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Session C3 : DAC & other Data Converter Module
C3-4

Systematic Construction of Resistor Ladder Network for *N*-ary DACs

Manato Hirai[1], Shuhei Yamamoto[1], Hirotaka Arai[1], Anna Kuwana[1], Hiroshi Tanimoto[2], Yuji Gendai[1], Haruo Kobayashi[1]

[1] Gunma University

[2] Kitami Institute of Technology,

Outline

- Research objective
- Current division with resistor ladder
- N-ary DAC configurations
  - Ternary DAC
  - Quaternary DAC
- Verification by SPICE simulations
- Conclusion and Future work

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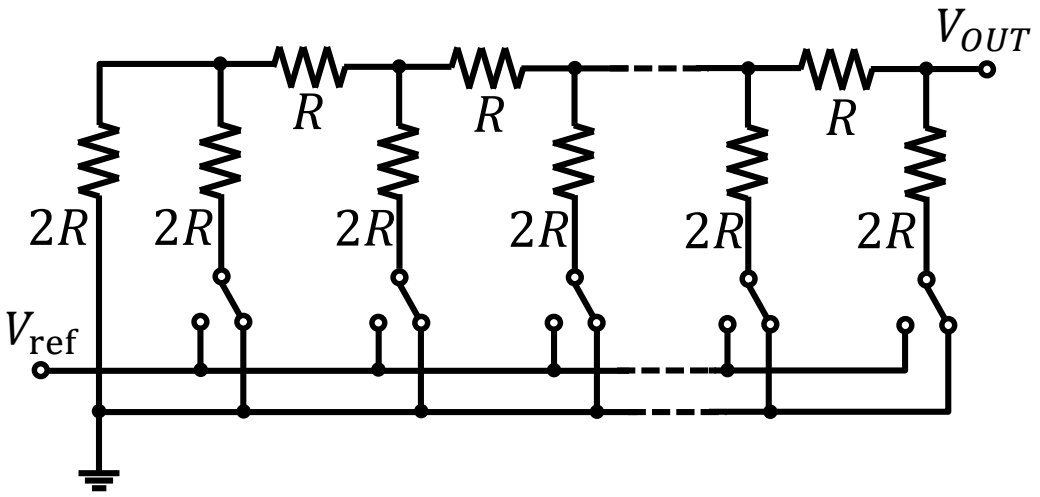
Research Objective

- Objective

  R-2R ladder

  – Binary weigted
  1-stage increment,
  1-bit increment



Voltage-mode R-2R DAC

Expanding

Derive N-ary DAC

- Generalized configuration of R-2R DAC
  – Ternary DAC
  – Quaternary DAC

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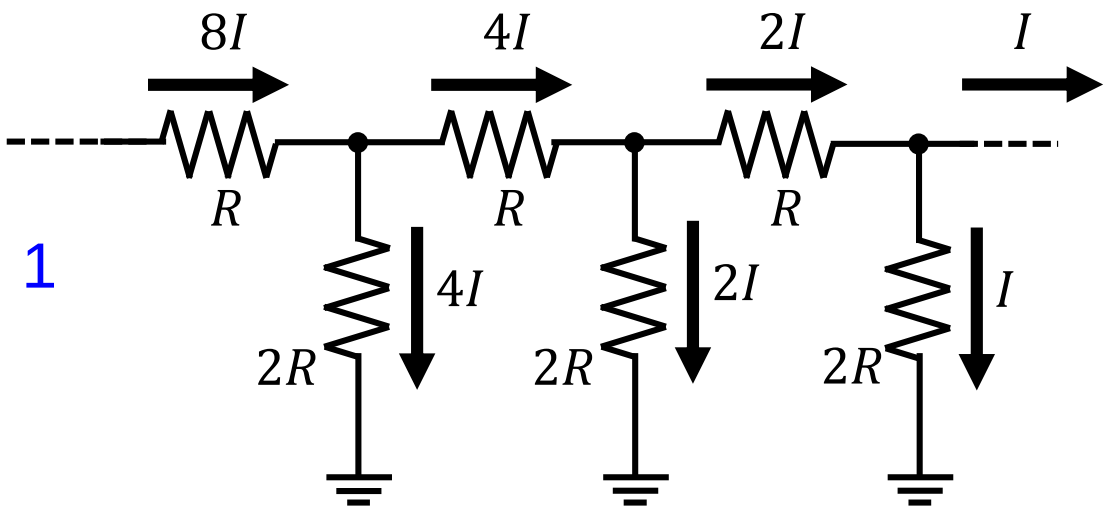
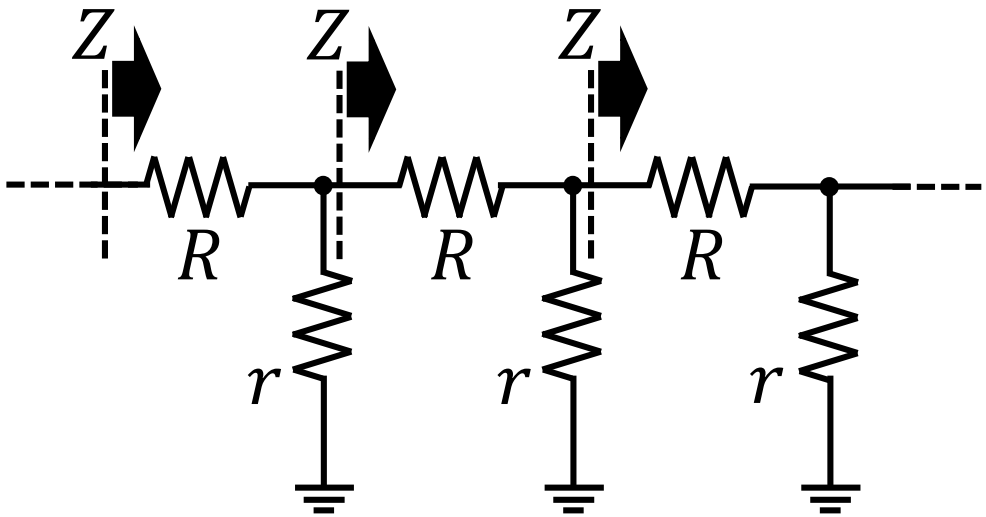
Current Division with Resistor Ladder

- R-2R ladder

→ Divide current into 1 : 1 at each node



Infinite R-2R ladder

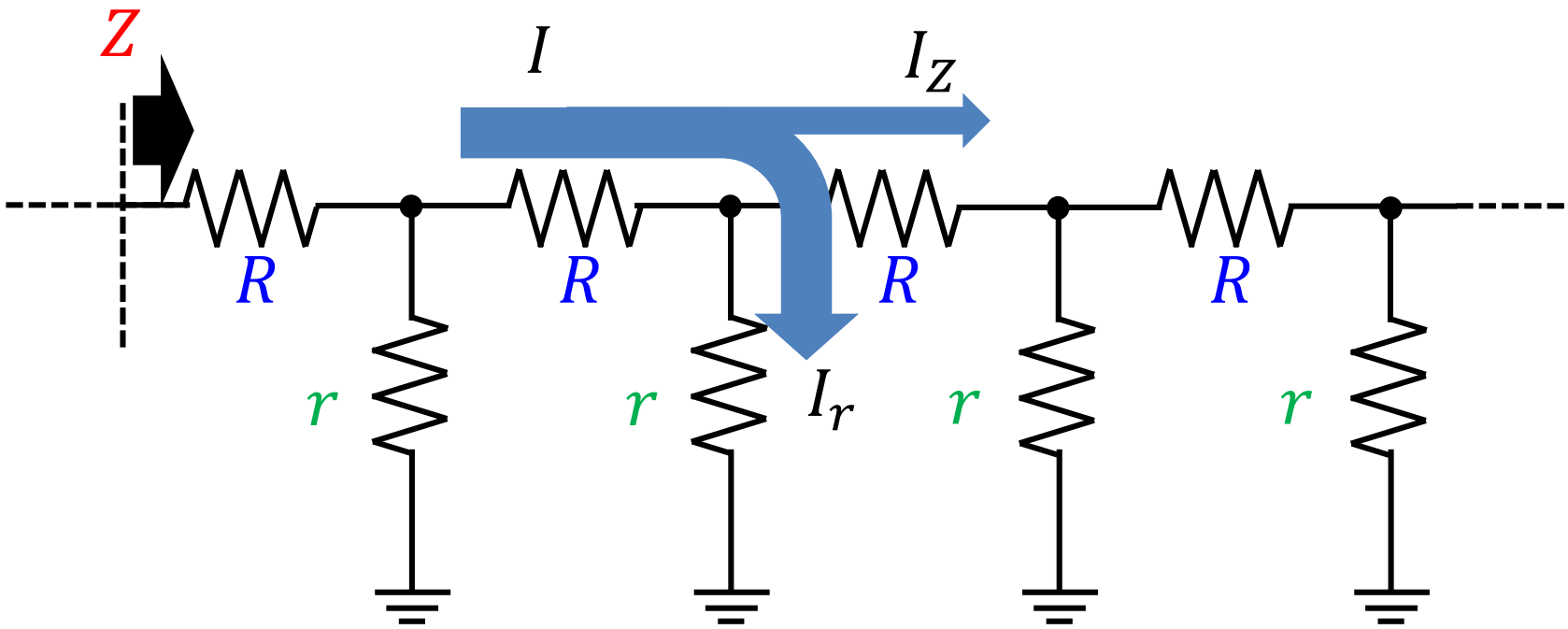


Infinite R-r resistor ladder

- R-r ladder Converges to

$$Z = \frac{R + \sqrt{R(R + 4r)}}{2}$$

Current Division by R-r Ladder

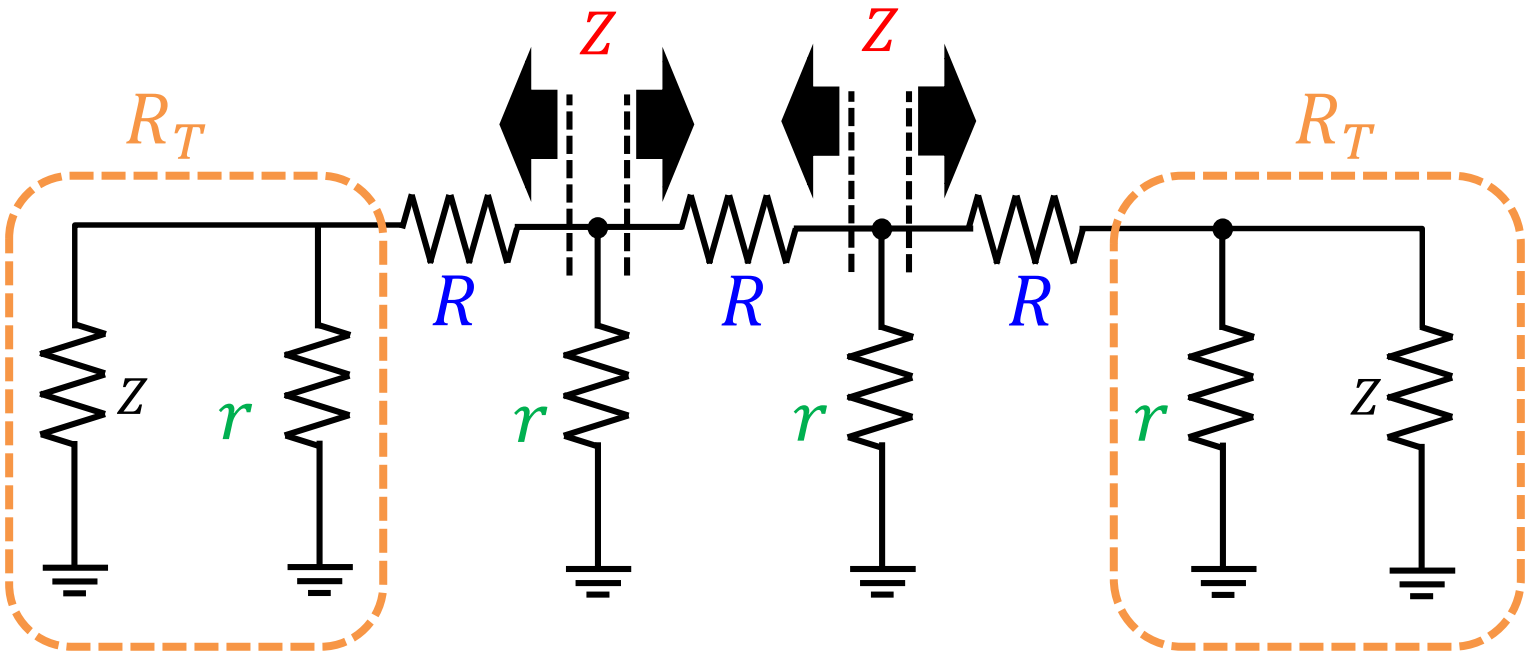


- $Z = \frac{R}{2} + \frac{\sqrt{R(R+4r)}}{2}$
- $I_r : I_Z = Z : r$
- Define $I_r : I_Z \equiv N - 1 : 1$

Ratio of R to r

$$\frac{R}{r} = \frac{(N-1)^2}{N}$$

Ladder Termination with R_T



- Terminate infinite ladder with R_T

$$R_T = Z - R = \frac{R}{N-1}$$

Resistance Ratio

$$R : r : R_T = (N-1)^2 : N : N-1$$

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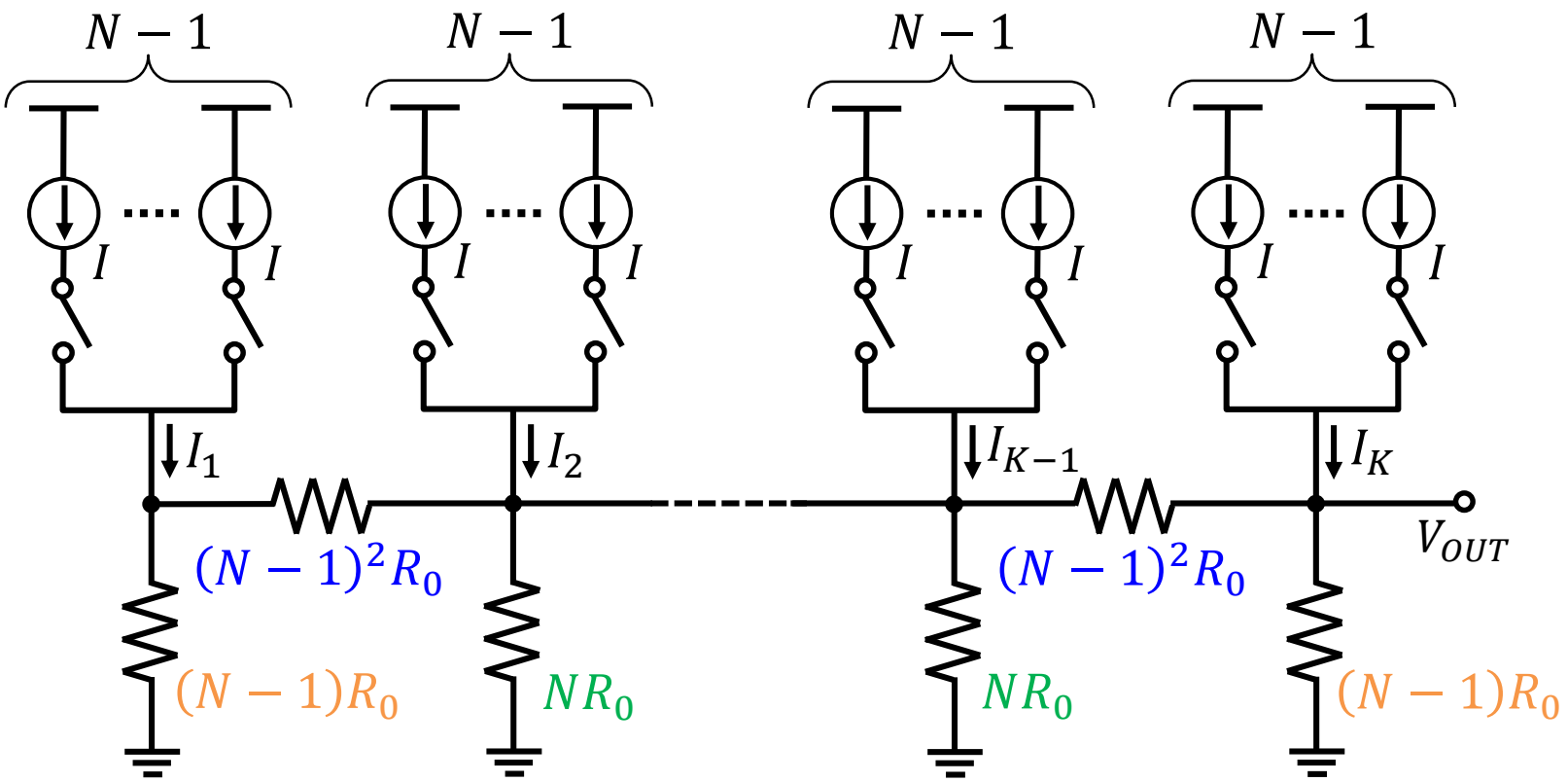
Configuration of *N*-ary DACs



- Stage number k
- Injected currents $I_1, \cdots, I_K$
- Normalizing resistance value R_0
- Current division ratio $\Rightarrow$ $N-1:1$

Theoretical output voltage

- Output voltage

$$V_{OUT}(I_1,\cdots,I_K,R_0,N,K)=R_0\frac{N(N-1)}{N+1}\sum_{k=1}^{K}\left(\frac{I_k}{N^{K-k}}\right)$$

- Maximum output voltage
  $\rightarrow I_k=(N-1)I$ for all k

$$V_{MAX}(I,R_0,N,K)=R_0 I\frac{N(N-1)^2}{N+1}\left(1-\frac{1}{N^K}\right)$$

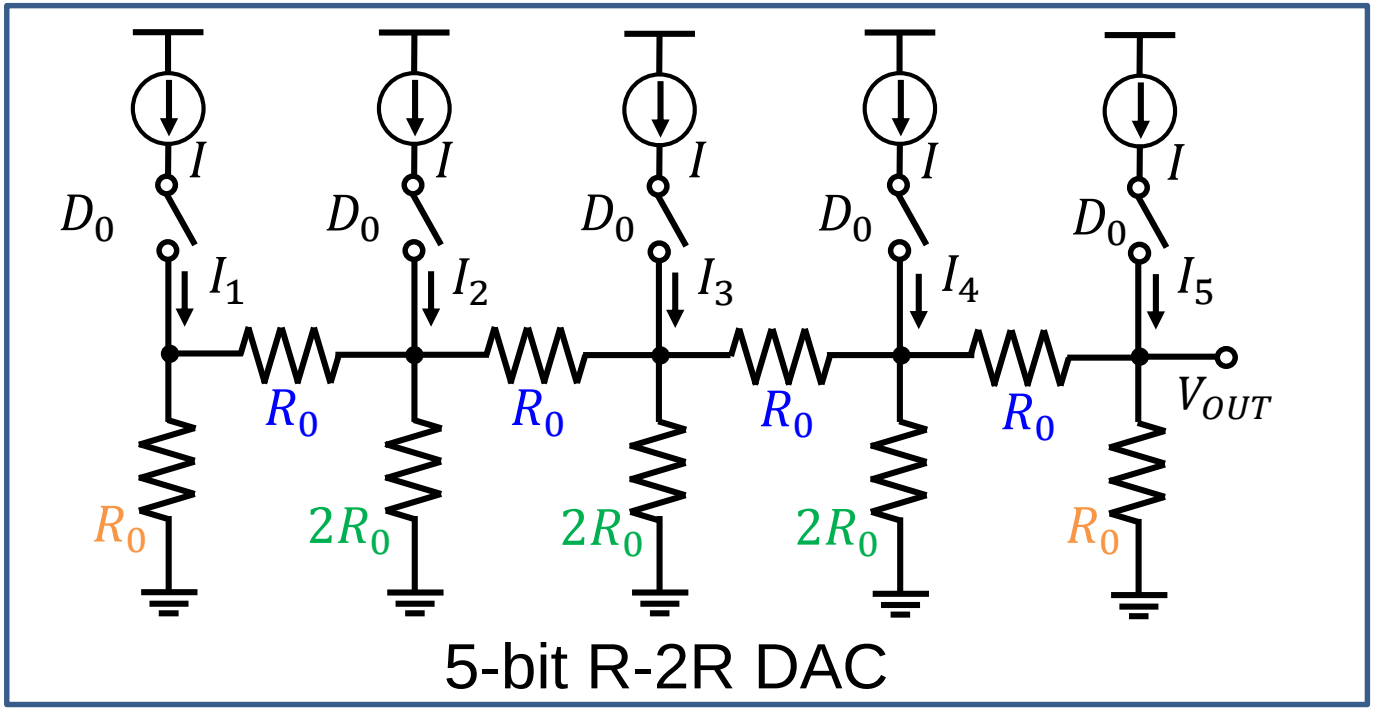
- Minimum voltage step
  $\rightarrow I_1=I$, for others $I_k=0$

$$V_{\min}(I,R_0,N,K)=R_0 I\frac{N-1}{(N+1)N^{K-2}}$$

K : Number of total stages
I_k : Injected currents $I_1,\cdots,I_K$
R_0 : Normalizing resistance value
$(N-1):1$: Current division ratio

$N = 2$, R-2R DAC

- $N = 2$, R-2R DAC
  - Number of total stages $K = 5 \rightarrow$ 5-bit

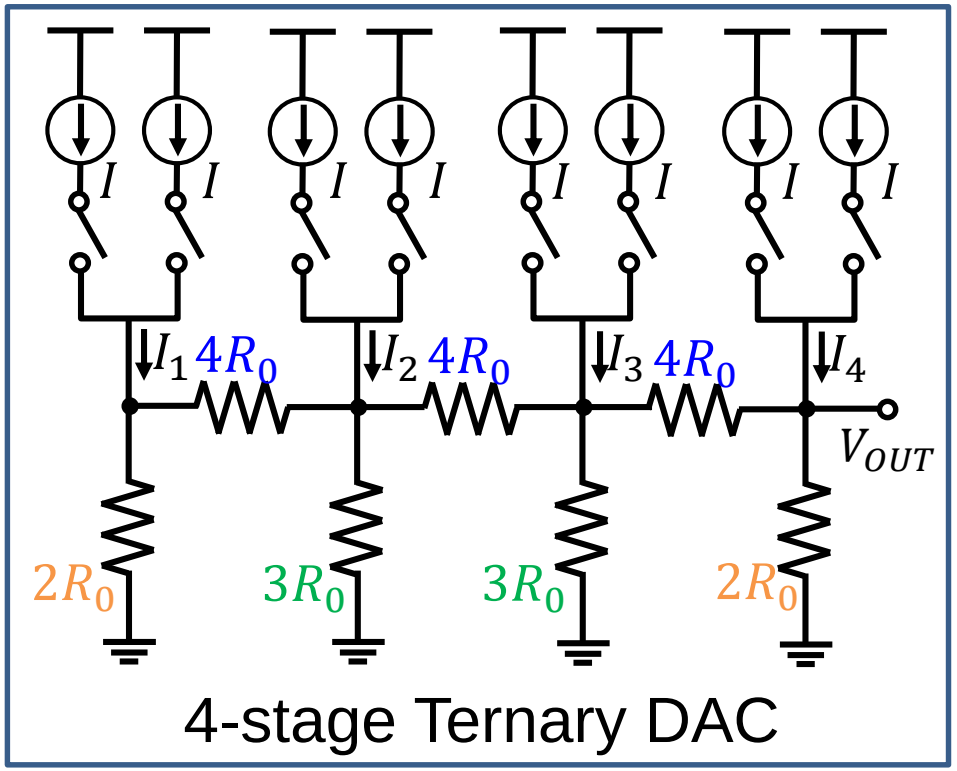


5-bit R-2R DAC

$$V_{OUT}(I_1, I_2, I_3, I_4, I_5, R_0) = R_0 I \cdot \frac{2}{3}\left(I_5 + \frac{1}{2^1} I_4 + \frac{1}{2^2} I_3 + \frac{1}{2^3} I_2 + \frac{1}{2^4} I_1\right)$$

$N = 3$, Ternary DAC

- Resistance ratio
  $R : r : R_T = 4R_0 : 3R_0 : 2R_0$
- Number of stages
  $K = 4$
- Number of minimum voltage steps
  $N^K - 1 = 3^4 - 1$
  $= 80$ steps



4-stage Ternary DAC

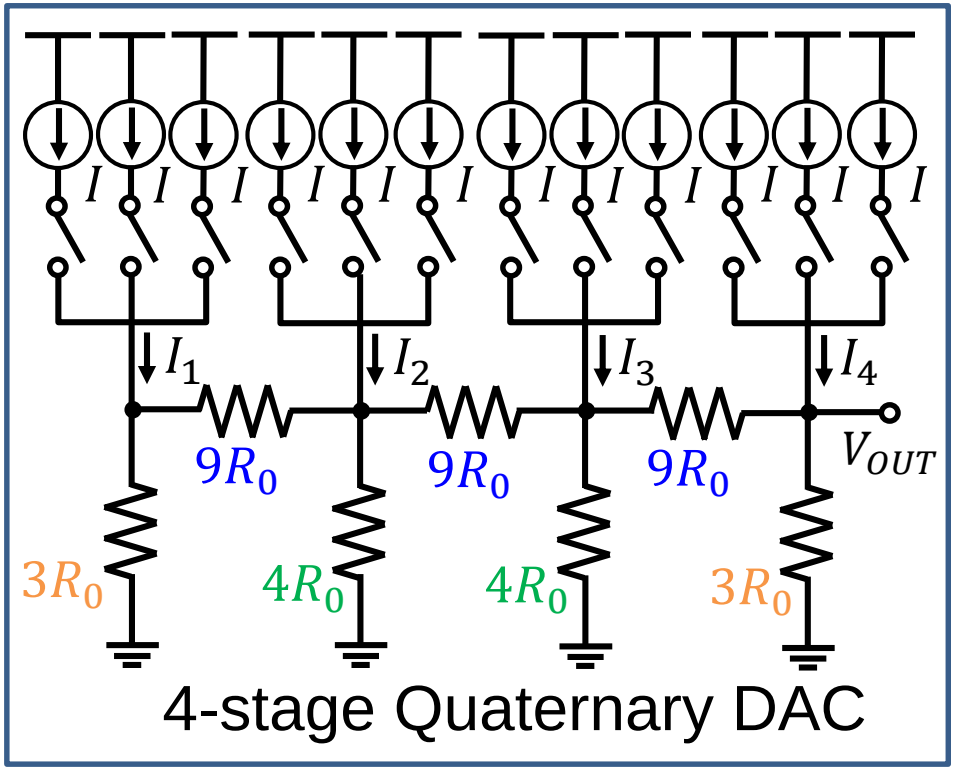
- Output voltage

$$V_{OUT}(I_1, I_2, I_3, I_4, R_0) = R_0 \cdot \frac{3}{2}\left(I_4 + \frac{1}{3^1} I_3 + \frac{1}{3^2} I_2 + \frac{1}{3^3} I_1\right)$$

Each I_k is ternary weighted.

$N = 4$, Quaternary DAC

- Resistance ratio
  $R : r : R_T = 9R_0 : 4R_0 : 3R_0$
- Number of stages
  $K = 4$
- Number of minimum voltage steps
  $N^K - 1 = 4^4 - 1$
  $= 255$ steps



4-stage Quaternary DAC

- Output voltage

$$V_{OUT}(I_1, I_2, I_3, I_4, R_0) = R_0 \cdot \frac{12}{5}\left(I_4 + \frac{1}{4^1} I_3 + \frac{1}{4^2} I_2 + \frac{1}{4^3} I_1\right)$$

Each I_k is quaternary weighted.

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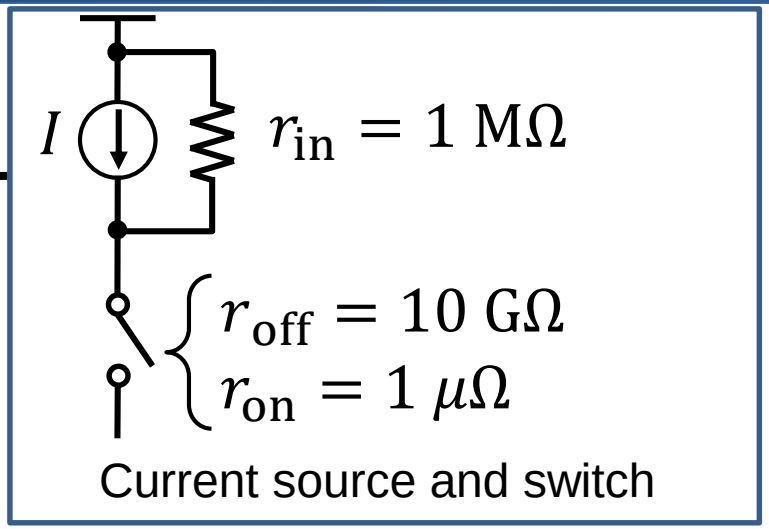
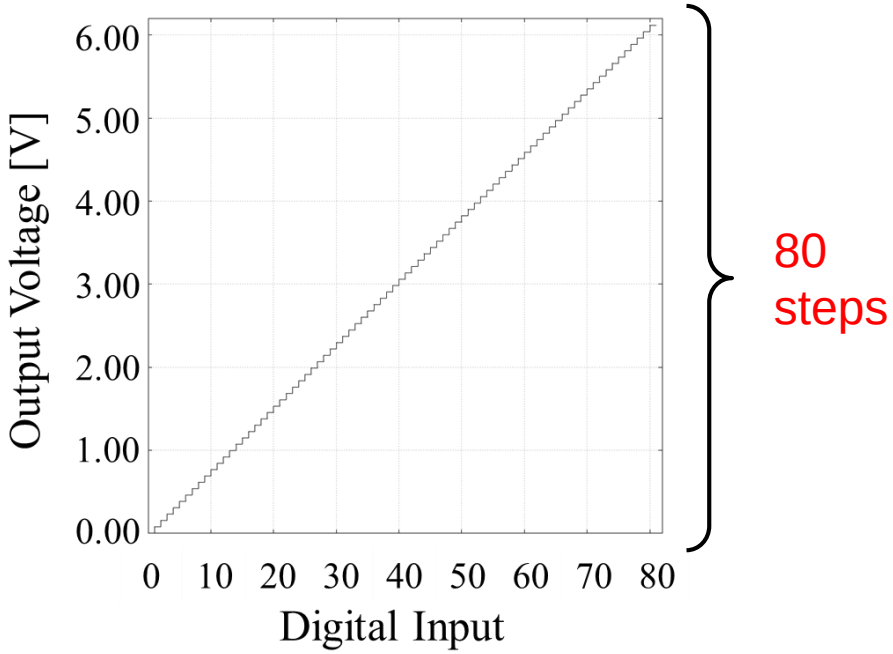
Simulation of Ternary DAC

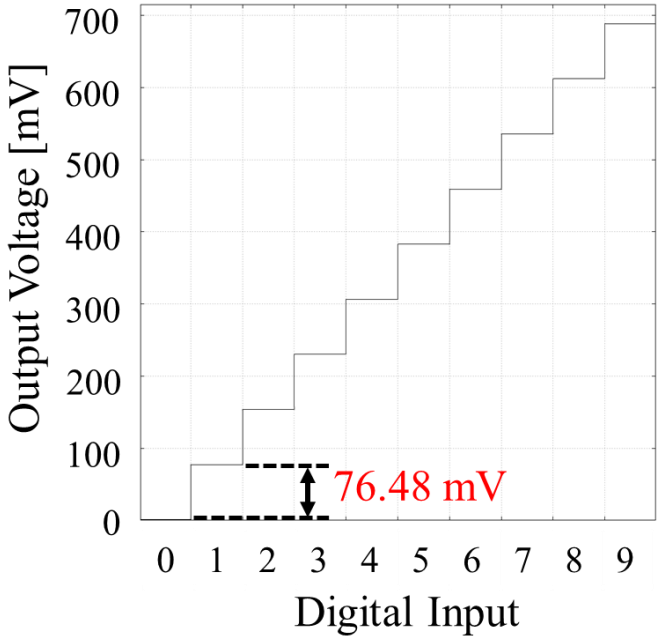
- Simulating input
  by switching current sources
- $R_0 = 100\ \Omega$, $I = 13.77\ \mathrm{mA}$
- Design value : $V_{MAX} = 6.12\ \mathrm{V}$, $V_{\min} = 76.5\ \mathrm{mV}$



Current source and switch



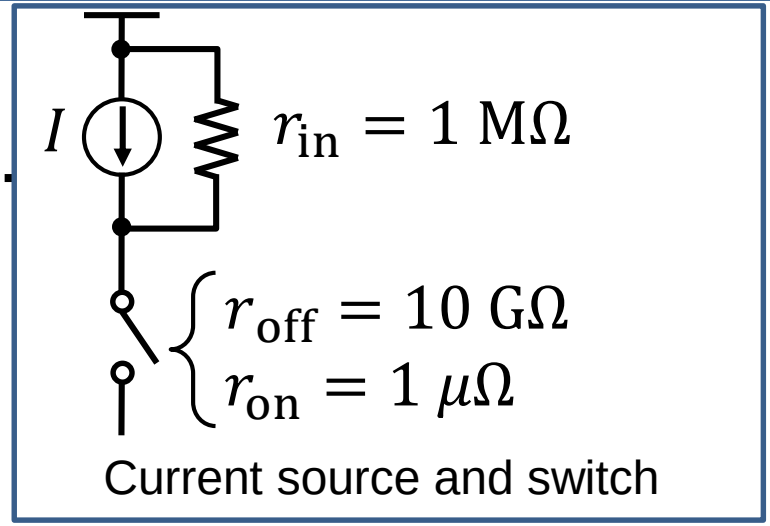
(a) Simulation result



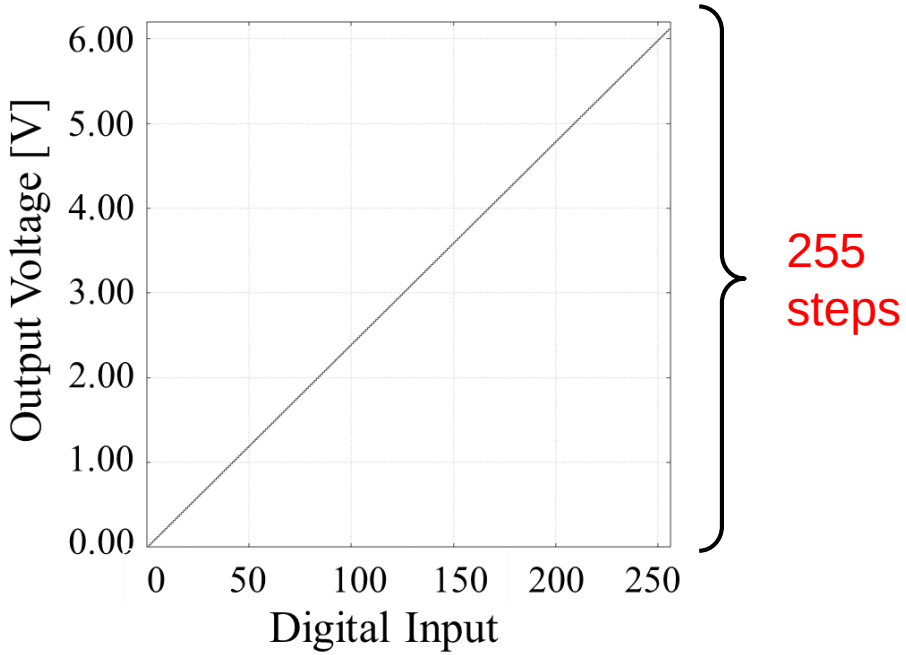
(b) Enlarged plot

Simulation of Quaternary DAC

- Simulating input by switching current sources
- $R_0 = 100\ \Omega$, $I = 6.40\ \mathrm{mA}$,
- Design value : $V_{MAX} = 6.12\ \mathrm{V}$, $V_{\mathrm{min}} = 24.0\ \mathrm{mV}$



Current source and switch



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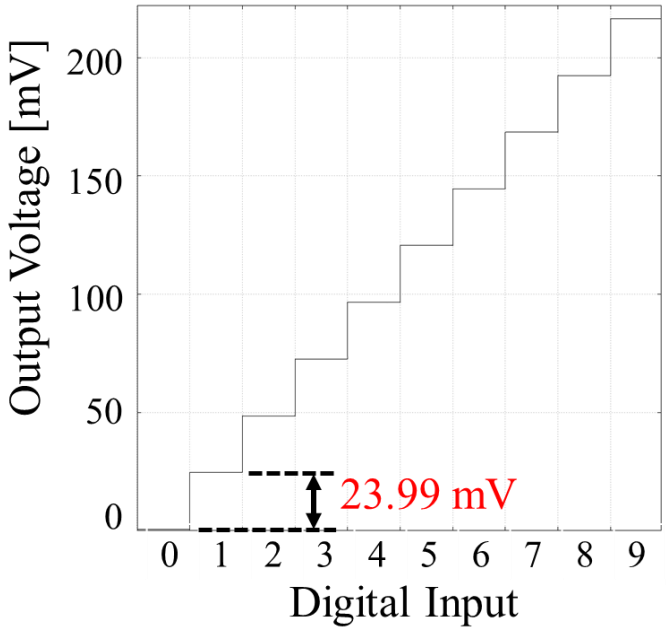

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Conclusion and Future work

- Our result
  - Generalize resistor ladder configurations including R-2R ladder

  - Proposal of N-ary DAC
- Future work
  - Devising effective usages of N-ary DAC
    - Less ladder stages, higher resolution
    - Voltage-mode configurations

Combined Resistance Value

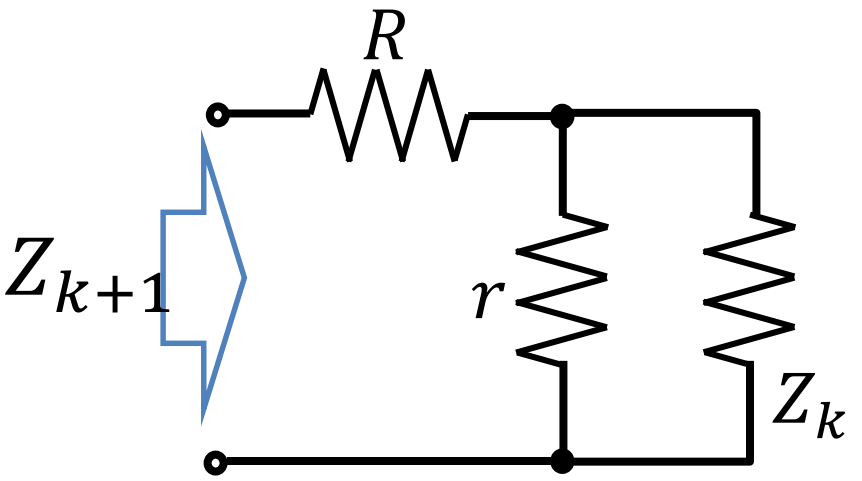
$$Z_k = \frac{\alpha\gamma^k - \beta}{\gamma^k - 1}$$

Here,

$$\alpha = \frac{1}{2}\left(R + \sqrt{R^2 + 4rR}\right),$$

$$\beta = \frac{1}{2}\left(R - \sqrt{R^2 + 4rR}\right),$$

$$\gamma = \frac{R + r - \beta}{R + r - \alpha}, 1 < \gamma$$



Convergence value:

$$Z_\infty = \frac{R}{2} + \frac{\sqrt{R(R + 4r)}}{2}$$