Optimization of High Reliability and Wide SOA 100V LDMOS Transistor with Low Specific On-Resistance

Anna Kuwana, Jun-ichi Matsuda and Haruo Kobayashi
(Gunma Univ., Japan)
Outline

1. Objective and Background
2. Conventional and Proposed LDMOS Transistor Structures
3. Simulation Results
   • Electric characteristics
     \[ I_{DS} - V_{DS}, R_{on,sp} \text{ vs. } B V_{DS}, \]
     \[ V_{DS, INT} \text{(Drain Voltage of the Intrinsic MOSFET)} \]
4. Discussion
   • Drain current expansion
   • Hot carrier endurance
   • Breakdown Location (ESD)
5. Summary

Simulation: 3D device simulator Advance/DESSERT developed by AdvanceSoft Corporation
1. Introduction

Background

• We proposed a 0.35 μm CMOS compatible dual REduced SURface Field (RESURF) 100 V LDMOS transistor with a two-step grounded field plate[1].

• For automotive applications to meet the requirements for
  ➢ wide SOA (Safe Operating Area)
  ➢ high hot carrier endurance
  ➢ low specific on-resistance
  ➢ low switching loss

1. Introduction

Cross-section of the Conventional LDMOS Transistor

Problems
- Low hot carrier endurance due to DAHC (drain avalanche hot carriers)
  ==> Caused by the high electric field in Region A
- Drain current expansion (CE) leading to a narrow SOA
  ==> Caused by the high electric field in Region B due to the Kirk effect
- Premature breakdown due to the high electric field in Region C under the drain
- High specific on-resistance due to low impurity concentration in the n-drift region (NDL)
- High switching loss due to the large Miller capacitance

1. Introduction

Cross-section of the Proposed LDMOS Transistor

- Two P-type buried Layers (Dual RESURF Structure)
  - PBL1: Enhances the RESURF effect in Region A, leading to high hot carrier endurance
  - PBL2:
    ① Causes a uniform electric field in the drift region
    ② Avoids premature breakdown in Region C

- Three N-type drift Layers
  - NDL1: The basic layer of the drift region
  - NDL2 and 3:
    ① Reduce specific on-resistance $R_{on,sp}$
    ② Suppress CE due to the low electric field in Region B

Cross-section of the Proposed LDMOS Transistor

- Two-Step Grounded Field Plate
  - FP1: Complements the RESURF effect in Region A
  - FP2: Complements the RESURF effect in the drift region excluding Region A
  - Reduces the Miller capacitance, leading to a low switching loss


A cross-section of the proposed device
(One cell size: 6.55 μm × 0.2 μm)
0.35 μm CMOS compatible process
Objective of this study

- This paper investigates how much production tolerances for the mask alignment of PBL1 (considered to have the greatest effect on characteristics).
- Simulation was carried out according to the following table.

### PBL1 net dose

<table>
<thead>
<tr>
<th>Condition</th>
<th>PBL1 net dose</th>
<th>∆PBL1 net dose</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td></td>
<td>-1.49×10^{13}</td>
</tr>
<tr>
<td>b</td>
<td></td>
<td>-7.50×10^{12}</td>
</tr>
<tr>
<td>c (standard)</td>
<td>* snip *</td>
<td>0.00</td>
</tr>
<tr>
<td>d</td>
<td></td>
<td>3.70×10^{12}</td>
</tr>
<tr>
<td>e</td>
<td></td>
<td>7.50×10^{12}</td>
</tr>
<tr>
<td>f</td>
<td></td>
<td>1.87×10^{13}</td>
</tr>
</tbody>
</table>

### PBL1 edge location

<table>
<thead>
<tr>
<th>Condition</th>
<th>PBL1 edge location</th>
<th>∆PBL1 edge location</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td></td>
<td>-600</td>
</tr>
<tr>
<td>b</td>
<td></td>
<td>-400</td>
</tr>
<tr>
<td>c</td>
<td>* snip *</td>
<td>-200</td>
</tr>
<tr>
<td>d (standard)</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>e</td>
<td></td>
<td>200</td>
</tr>
<tr>
<td>f</td>
<td></td>
<td>400</td>
</tr>
</tbody>
</table>

[cm^{-2}] [nm]
2. Simulation results

\[ I_{DS} - V_{DS} \] characteristics

Drain current \( I_{DS} \) vs. drain voltage \( V_{DS} \) characteristics at a gate voltage \( V_{GS} \) of 6 V

<table>
<thead>
<tr>
<th>SOA: Safe Operating Area</th>
<th>CE: Current Expansion</th>
</tr>
</thead>
</table>

(a) \( \Delta \)PBL1 net dose dependence.

\( V_{GS} = 6V \)

- \( \Delta \)PBL1 Dose (cm\(^{-2}\))
  - \(-1.49 \times 10^{13}\)
  - \(0\) (Standard)
  - \(+1.87 \times 10^{13}\)

(b) \( \Delta \)PBL1 edge location dependence.

\( V_{GS} = 6V \)

\( \Delta \)PBL1 Edge Location (nm)
- \(-600\)
- \(-400\)
- \(-200\)
- \(0\)
- \(+200\)

CE phenomena are...

- gradually suppressed with increasing the \( \Delta \)PBL1 dose.
- the \( \Delta \)PBL1 edge location.
- saturate for \( \Delta \)PBL1 dose > 0 cm\(^{-2}\).
- \( \Delta \)PBL1 edge location > 0 nm.
2. Simulation results

**BV\textsubscript{DS} and R\textsubscript{on,sp}**

\(\Delta\text{PBL1 dose dependences of BV}\textsubscript{DS} \text{ and } R\text{on,sp.} \)

at \(V\text{DS}=0.6\text{V}\) and \(V\text{GS}=5\text{V}\), the operation gate voltage.

(a) \(\Delta\text{PBL1 net dose dependence.}\)

When **PBL1 net dose \(\leq \text{standard } \pm 7.50 \times 10^{12} \text{ cm}^{-2}\)**


(b) \(\Delta\text{PBL1 edge location dependence.}\)

\(\text{Tolerance}\)

- suppressed CE
- keep the top-level \(BV\text{DS} \text{ and } R\text{on,sp}\)
2. Simulation results

**Dependence of the drain voltage of the intrinsic MOSFET**

- Decrease the PBL1 dose
  - the PBL1 edge location...
- $$\Rightarrow V_{DS,INT}$$ increase
- $$\Rightarrow$$ in linear mode, $$I_{DS}$$ increase
- $$\Rightarrow$$ CE phenomena easily occur

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(a) $\Delta$PBL1 net dose dependence.

(b) $\Delta$PBL1 edge location dependence.
3. Discussion

Current expansion

CE difference depending on the PBL1 net dose

Profiles of the electric field (linear mode)

CE suppressed with increasing the PBL1 dose.

Increasing the PBL1 dose.

==> \( I_{DS} \) decrease.

==> suppression of the Kirk effect

==> CE suppressed.
3. Discussion

Current expansion

CE difference depending on the PBL1 edge location

Profiles of the electric field (linear mode)

Increasing the PBL1 edge location.

=> $I_{DS}$ decrease.

=> suppression of the Kirk effect

=> CE suppressed.
Hot carrier endurance

Profiles of the electric field (saturation mode)

(a) $\Delta$PBL1 net dose dependence. The peak near the gate-side drift region edge decreases with increasing the $\Delta$PBL1 net dose.

(b) $\Delta$PBL1 edge location dependence. Thanks to enhanced RESURF effect, $\Rightarrow$ Higher hot carrier endurance.
ΔPBL1 dose dependences of $BV_{DS}$ and $R_{on,sp}$.

at $V_{DS}=0.6\text{V}$ and $V_{GS}=5\text{V}$, the operation gate voltage.

When $\text{PBL1 net dose} \leq \text{standard} \pm 7.50 \times 10^{12} \text{cm}^{-2}$

$\text{PBL1 edge location} \leq \text{standard} \pm 50 \text{nm}$

- suppressed CE
- keep the top-level $BV_{DS}$ and $R_{on,sp}$
3. Discussion

Hot carrier endurance

Profiles of the electric field (saturation mode)

(a) ∆PBL1 net dose dependence.

Lower tolerance limits?
- PBL1 net dose = standard $-7.50 \times 10^{12}$ cm$^{-2}$
  $\Rightarrow$ raises the peak by about 8 % from the standard
- PBL1 edge location = standard -50 nm
  $\Rightarrow$ raises the peak by about 5 % from the standard

$\Rightarrow$ Too small to further deteriorate hot carrier endurance.

(b) ∆PBL1 edge location dependence.
3. Discussion

The electric fields upon avalanche breakdown

High electric field regions cause avalanche breakdown.
3. Discussion

The hole current density upon avalanche breakdown

Location is far from the device

=> Breakdown A would not cause damage to the intrinsic MOSFET.
3. Discussion

The hole current density upon avalanche breakdown

Breakdown B might cause...

- damage to the intrinsic MOSFET.
- destruction due to filamentation in the drift region, leading to reduction of Electro Static Discharge (ESD) endurance.

==> however, adding ballast resistance to the drain would improve ESD endurance.

Standard (ΔPBL1=0nm)
$V_{DS}=133V$
$V_{GS}=0V$

Sample (ΔPBL1=+200nm)
$V_{DS}=120V$
$V_{GS}=0V$
Summary

• We have **optimized** the PBL1 net dose and the PBL1 edge location of the proposed dual RESURF 100 V LDMOS transistor for automotive applications.

• Although those parameters of PBL1 significantly affect electrical characteristics ($BV_{DS}$, $R_{on,sp}$, CE, and hot carrier endurance), we can obtain **top-level characteristics** of $BV_{DS}$ and $R_{on,sp}$ with keeping sufficiently suppressed CE and high hot carrier endurance **even in the wide range tolerances of the parameters for mass production**.

• In future, we will proceed to optimization of other parameters.
Acknowledgments

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