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Optimization of High Reliability and Wide SOA 100V LDMOS Transistor with Low Specific On-Resistance

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Outline

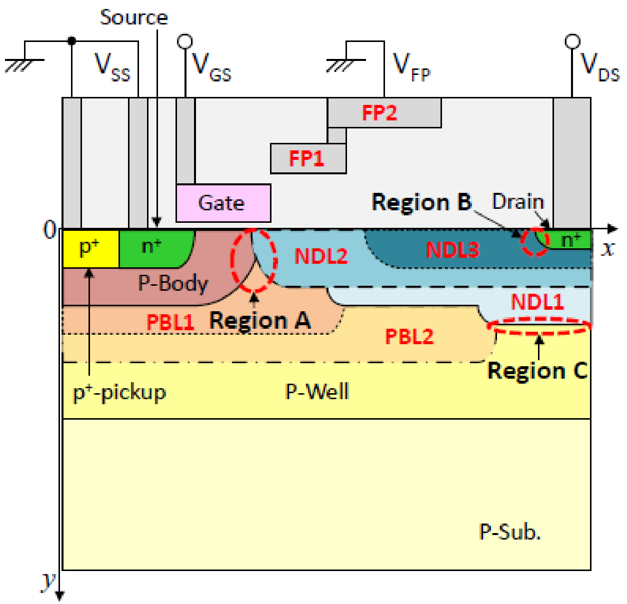
1. Objective and Background
2. Conventional and Proposed LDMOS Transistor Structures
3. Simulation Results
    - Electric characteristics
        - I_{DS}-V_{DS}, $R_{on,sp}$ vs. BV_{DS},
        - $V_{DS,INT}$(Drain Voltage of the Intrinsic MOSFET)
4. Discussion
    - Drain current expansion
    - Hot carrier endurance
    - Breakdown Location (ESD)
5. Summary

Simulation: 3D device simulator Advance/DESSERT developed by AdvanceSoft Corporation

Background

- We proposed a 0.35 μm CMOS compatible dual REduced SURface Field (RESURF) 100 V LDMOS transistor with a two-step grounded field plate[1].

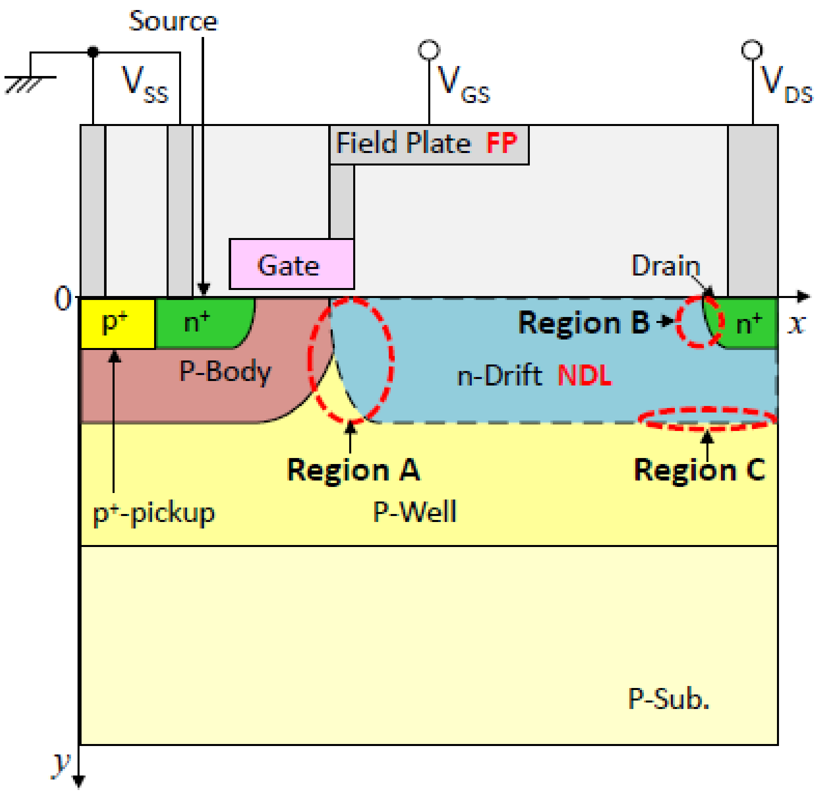
- For automotive applications to meet the requirements for
  - wide SOA (Safe Operating Area)
  - high hot carrier endurance
  - low specific on-resistance
  - low switching loss



A cross-section of the proposed device
(One cell size: 6.55 μm × 0.2 μm)
0.35 μm CMOS compatible process

[1] J. Matsuda, A. Kuwana, J. Kojima, N. Tsukiji, and H. Kobayashi, ICSICT, (2018).

Cross-section of the Conventional LDMOS Transistor



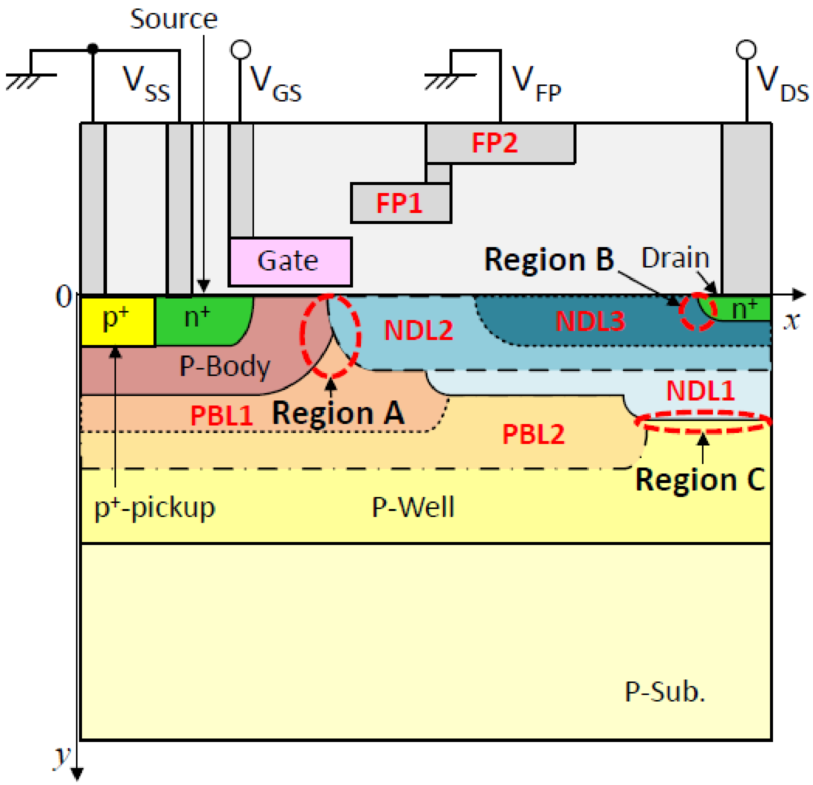
A cross-section of the conventional device
(One cell size: 6.55 µm × 0.2 µm)
0.35 µm CMOS compatible process

Problems

- Low hot carrier endurance
  due to DAHC(drain avalanche hot carriers)
  ==> Caused by the high electric field
  in Region A
- Drain current expansion (CE)
  leading to a narrow SOA
  ==> Caused by the high electric field
  in Region B due to the Kirk effect
- Premature breakdown due to the high electric field in Region C under the drain
- High specific on-resistance due to low impurityconcentration in the n-drift region (NDL)
- High switching loss
  due to the large Miller capacitance

[1] J. Matsuda, A. Kuwana, J. Kojima, N. Tsukiji, and H. Kobayashi, ICSICT, (2018).

Cross-section of the Proposed LDMOS Transistor



A cross-section of the proposed device
(One cell size: 6.55 µm × 0.2 µm)
0.35 µm CMOS compatible process

■Two P-type buried Layers
(Dual RESURF Structure)

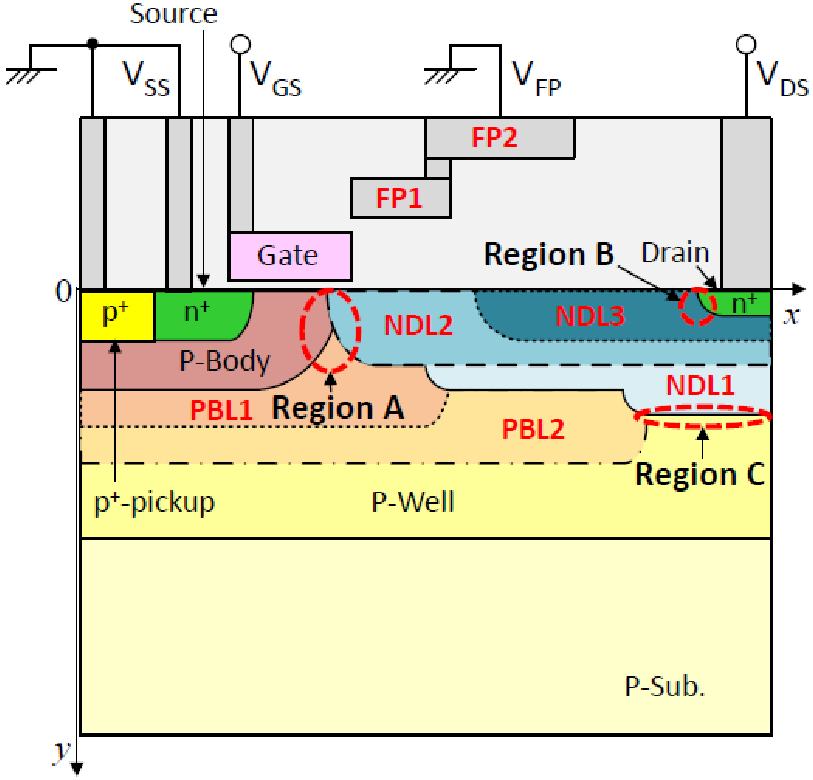
- PBL1: Enhances the RESURF effect in Region A, leading to high hot carrier endurance
- PBL2:
  ①Causes a uniform electric field in the drift region
  ②Avoids premature breakdown in Region C

■Three N-type drift Layers

- NDL1: The basic layer of the drift region
- NDL2 and 3:
  ①Reduce specific on-resistance $R_{on,sp}$
  ②Suppress CE due to the low electric field in Region B

[1] J. Matsuda, A. Kuwana, J. Kojima, N. Tsukiji, and H. Kobayashi, ICSICT, (2018).

Cross-section of the Proposed LDMOS Transistor



A cross-section of the proposed device
(One cell size: 6.55 μm × 0.2 μm)
0.35 μm CMOS compatible process

■Two-Step Grounded Field Plate

- FP1: Complements the RESURF effect in Region A
- FP2: Complements the RESURF effect in the drift region excluding Region A
- Reduces the Miller capacitance, leading to a low switching loss

[1] J. Matsuda, A. Kuwana, J. Kojima, N. Tsukiji, and H. Kobayashi, ICSICT, (2018).

Objective of this study

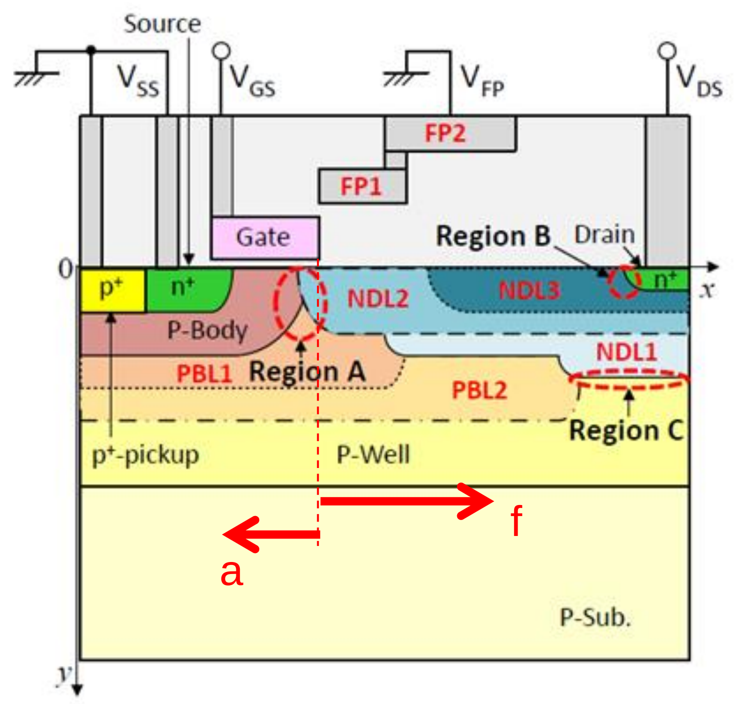
- This paper investigates how much production tolerances for the mask alignment of PBL1 (considered to have the greatest effect on characteristics)
- Simulation was carried out according to the following table.

[cm^{-2}]

Condition	PBL1 net dose	ΔPBL1 net dose
a		-1.49×10^{13}
b		-7.50×10^{12}
c (standard)	* snip *	0.00
d		3.70×10^{12}
e		7.50×10^{12}
f		1.87×10^{13}

[nm]

Condition	PBL1 edge location	ΔPBL1 edge location
a		-600
b		-400
c	* snip *	-200
d (standard)		0
e		200
f		400

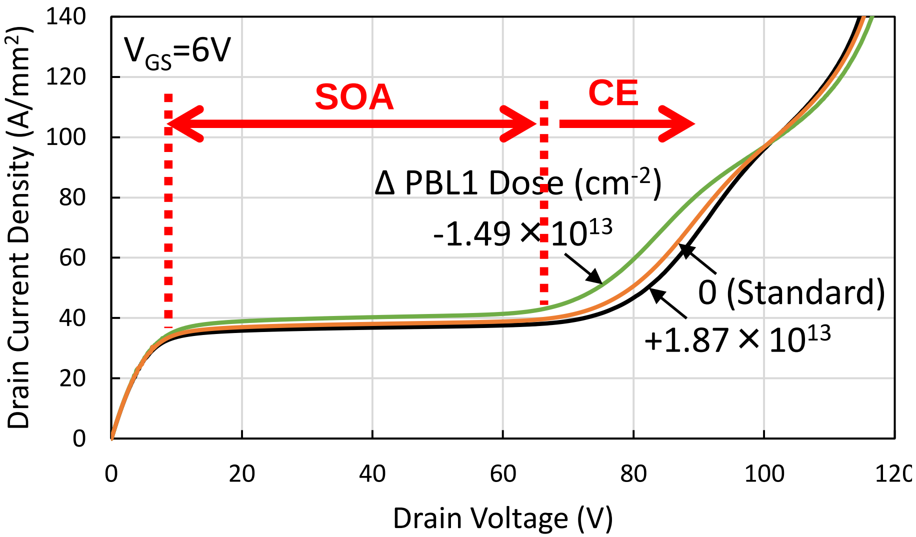


I_{DS}-V_{DS} characteristics

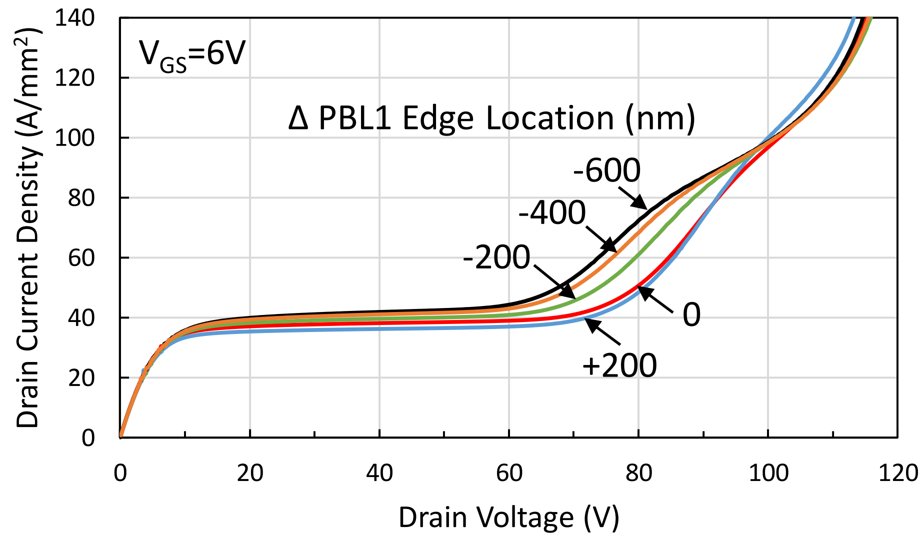
Drain current I_{DS} vs. drain voltage V_{DS} characteristics at a gate voltage V_{GS} of 6 V

SOA:
Safe Operating Area 

CE:
Current Expansion 



(a) ΔPBL1 net dose dependence.



(b) ΔPBL1 edge location dependence.

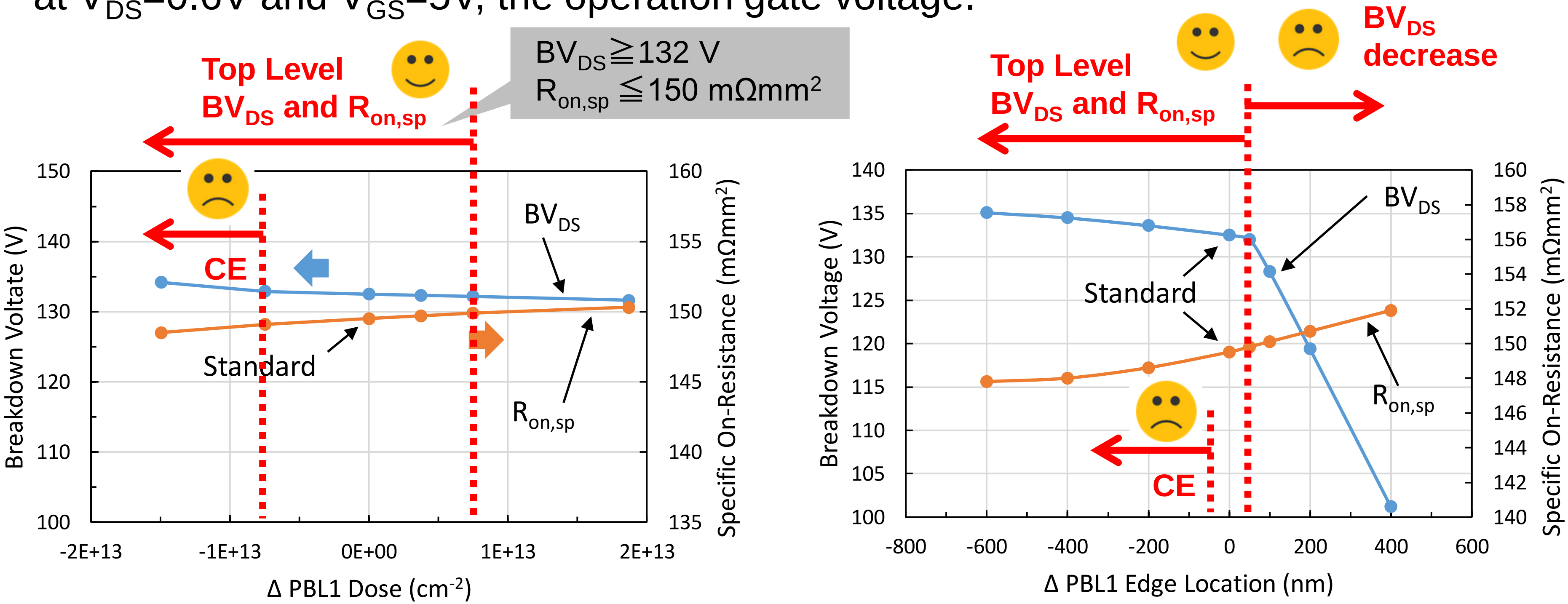
CE phenomena are...

- gradually suppressed with increasing the PBL1 dose.
  the PBL1 edge location.
- saturate for ΔPBL1 dose > 0 cm^{-2}.
  ΔPBL1 edge location> 0 nm.

BV_{DS} and $R_{on,sp}$

ΔPBL1 dose dependences of BV_{DS} and $R_{on,sp}$.

at V_{DS}=0.6V and V_{GS}=5V, the operation gate voltage.



(a) ΔPBL1 net dose dependence.

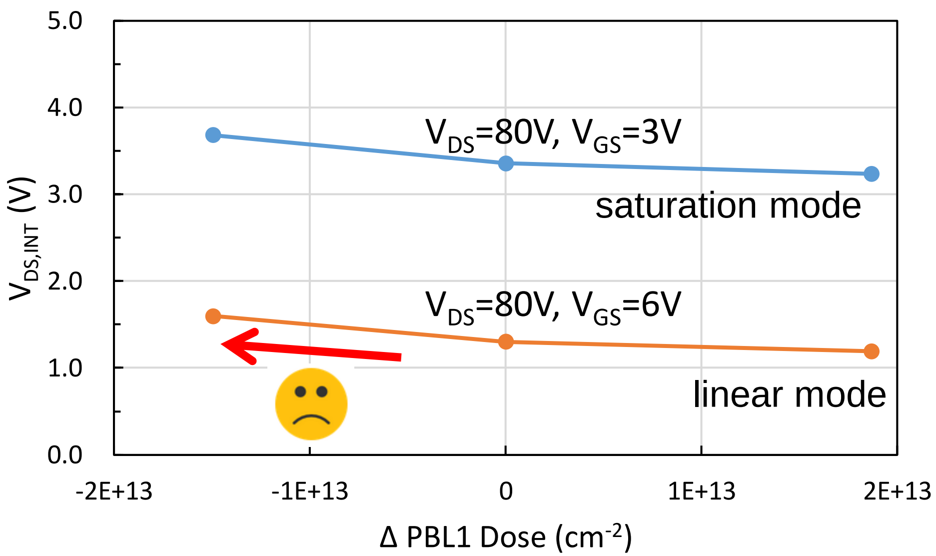
(b) ΔPBL1 edge location dependence.

When **PBL1 net dose ≦standard ±7.50×10¹² cm⁻²**
PBL1 edge location ≦standard ±50 nm
} **Tolerance**

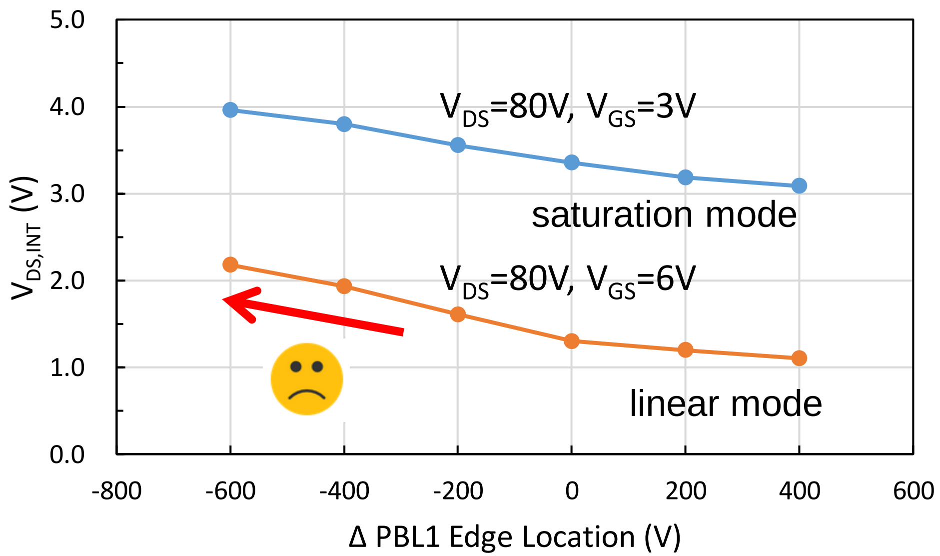
- suppressed CE
- keep the top-level BV_{DS} and $R_{on,sp}$

$V_{DS,INT}$

Dependence of the drain voltage of the intrinsic MOSFET



(a) ΔPBL1 net dose dependence.

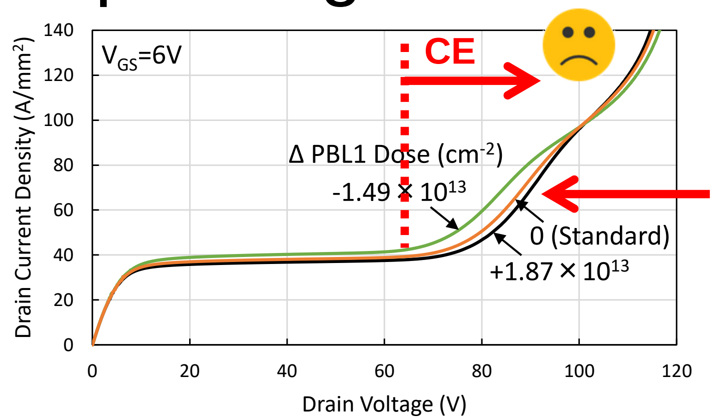


(b) ΔPBL1 edge location dependence.

- Decrease the PBL1 dose
  the PBL1 edge location...
- ==> $V_{DS,INT}$ increase
- ==> in linear mode, I_{DS} increase
- ==> CE phenomena easily occur

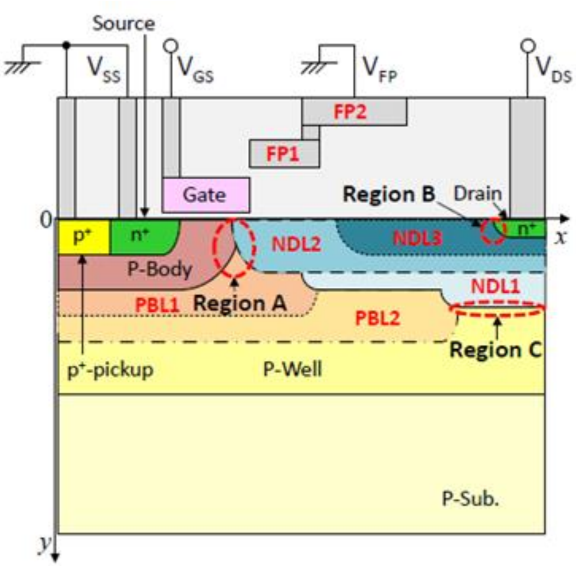
Current expansion

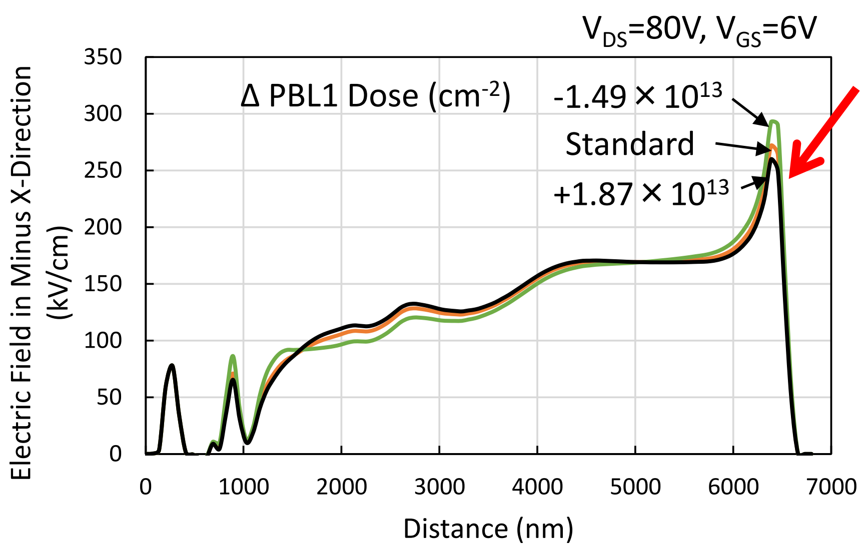
CE difference depending on the PBL1 net dose



CE suppressed with increasing the PBL1 dose.

Profiles of the electric field (linear mode)

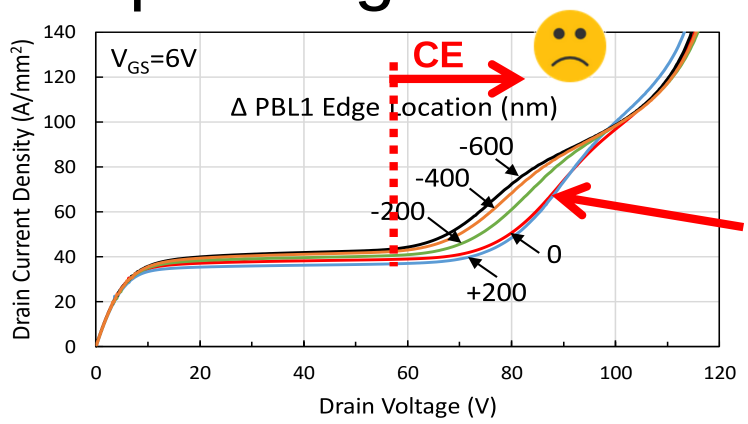




Increasing the PBL1 dose.
==> I_{DS} decrease.
==> suppression of the Kirk effect
==> CE suppressed.

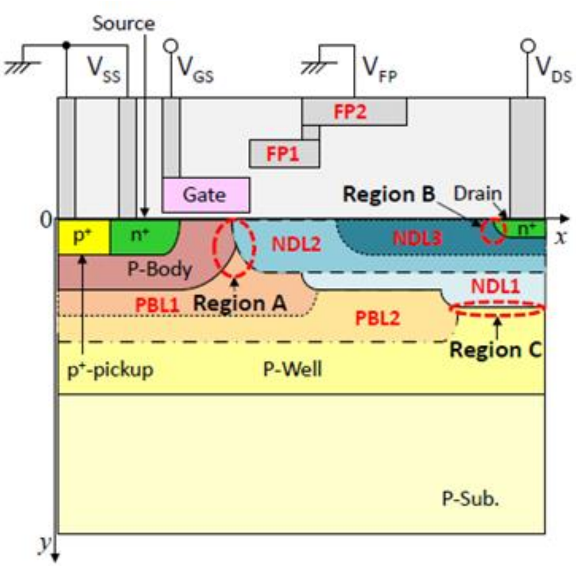
Current expansion

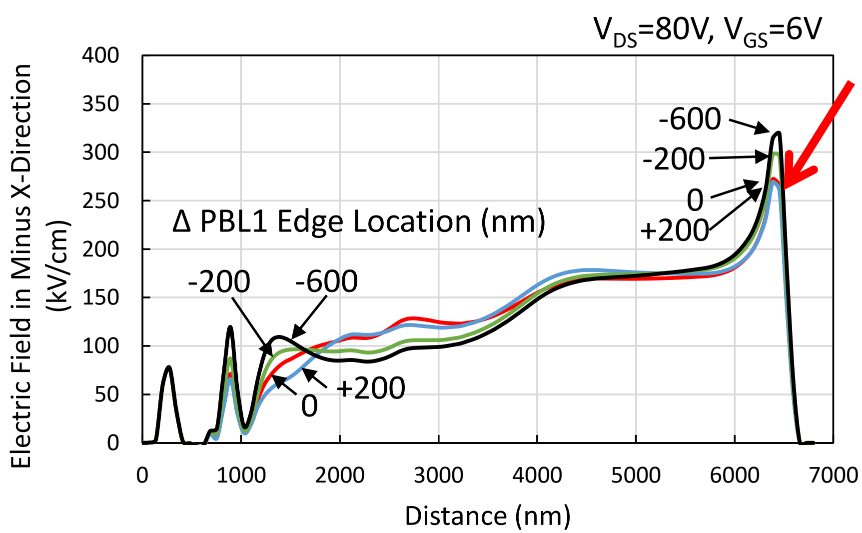
CE difference depending on the PBL1 edge location



CE suppressed with increasing the PBL1 edge location

Profiles of the electric field (linear mode)

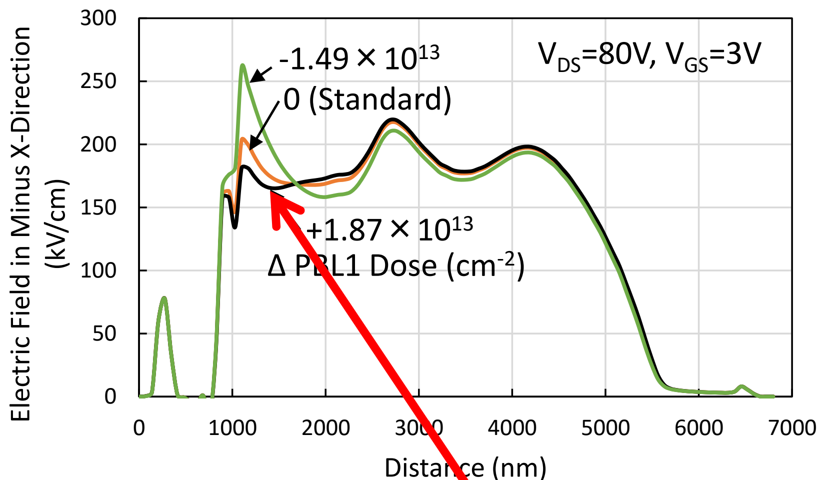




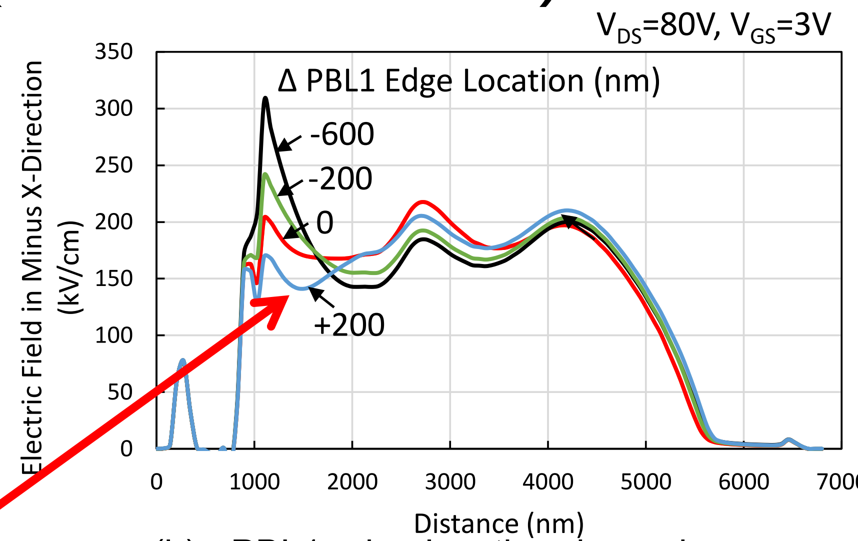
Increasing the PBL1 edge location.
==> I_{DS} decrease.
==> suppression of the Kirk effect
==> CE suppressed.

Hot carrier endurance

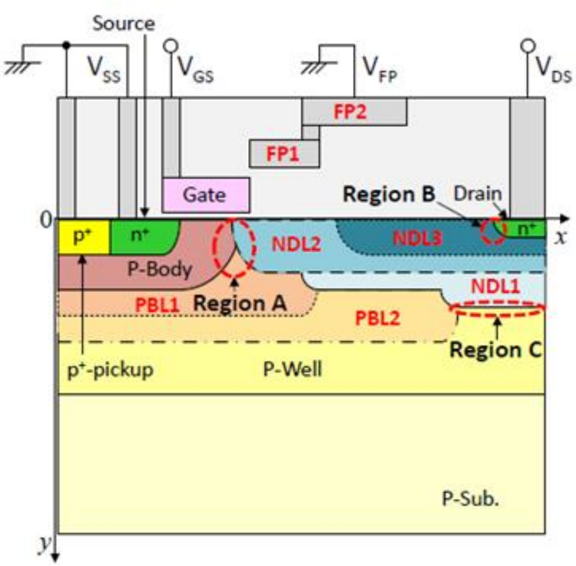
Profiles of the electric field (saturation mode)



(a) ΔPBL1 net dose dependence.



(b) ΔPBL1 edge location dependence.



The peak near the gate-side drift region edge decreases with increasing the ΔPBL1 net dose

the ΔPBL1 edge location

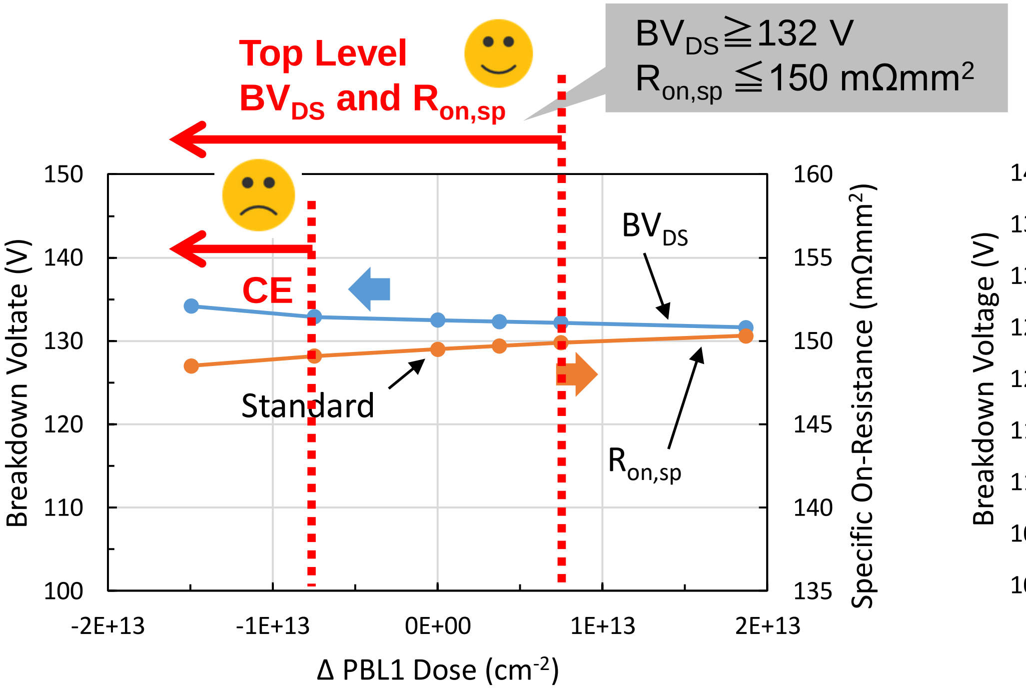
Thanks to enhanced RESURF effect

==> Higher hot carrier endurance. 🙂

BV_{DS} and $R_{on,sp}$

ΔPBL1 dose dependences of BV_{DS} and $R_{on,sp}$.

at V_{DS}=0.6V and V_{GS}=5V, the operation gate voltage.



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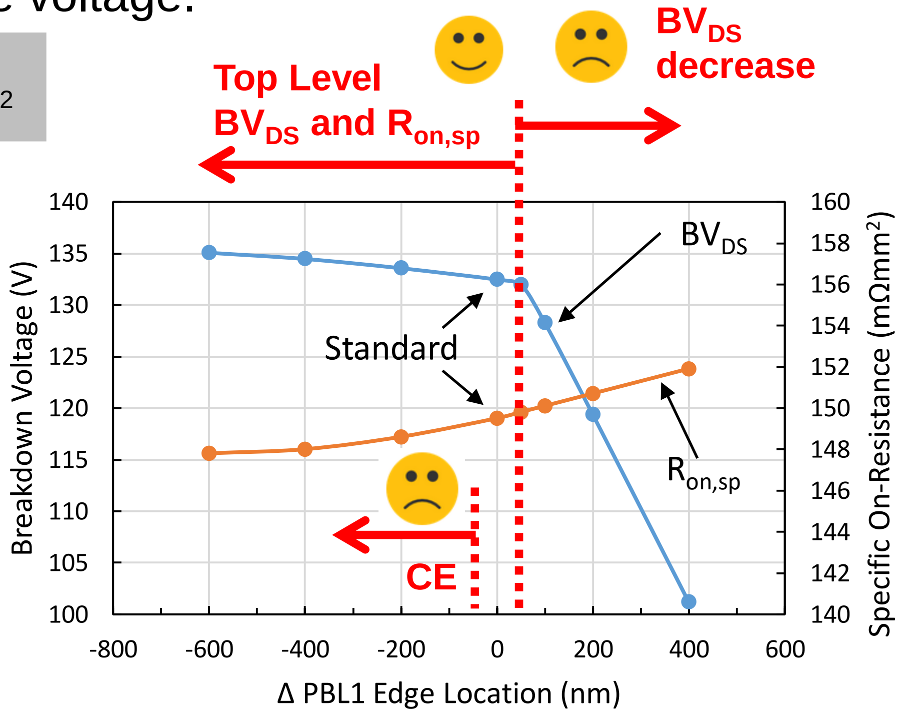


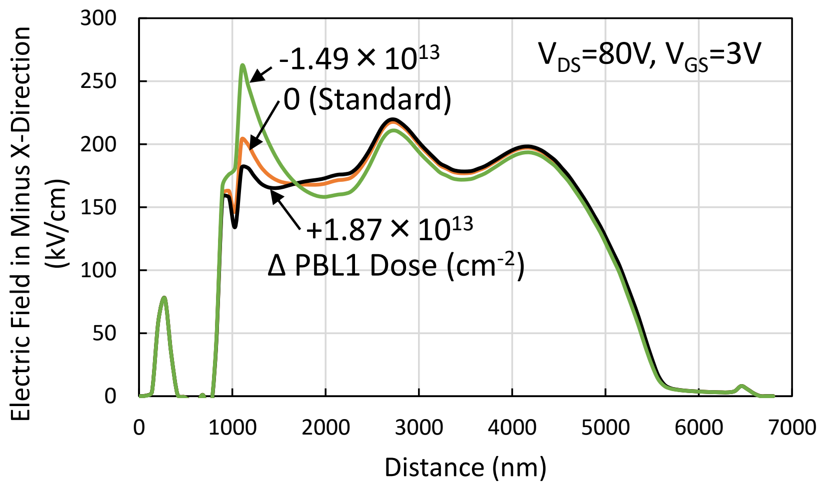
(b) ΔPBL1 edge location dependence.

When **PBL1 net dose ≦standard ±7.50×10^{12} cm^{-2}**
PBL1 edge location ≦standard ±50 nm
} **Tolerance**

- suppressed CE
- keep the top-level BV_{DS} and $R_{on,sp}$

Hot carrier endurance

Profiles of the electric field (saturation mode)



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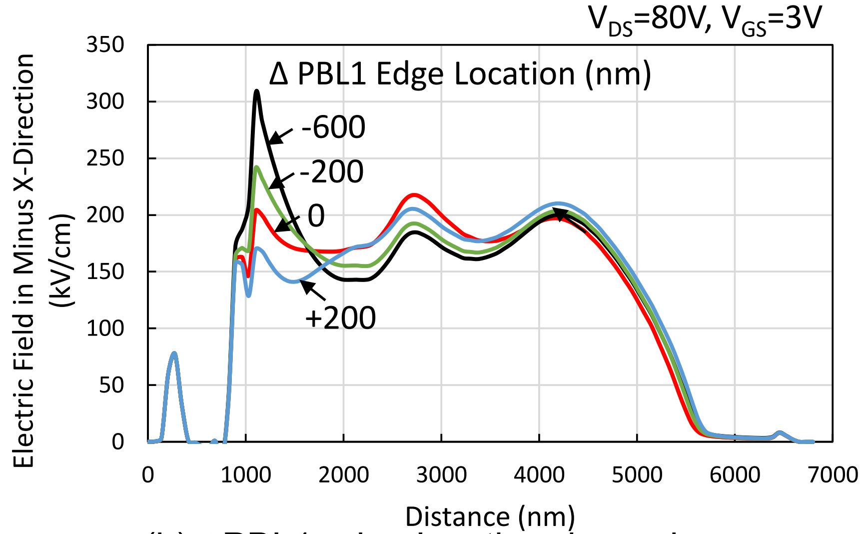
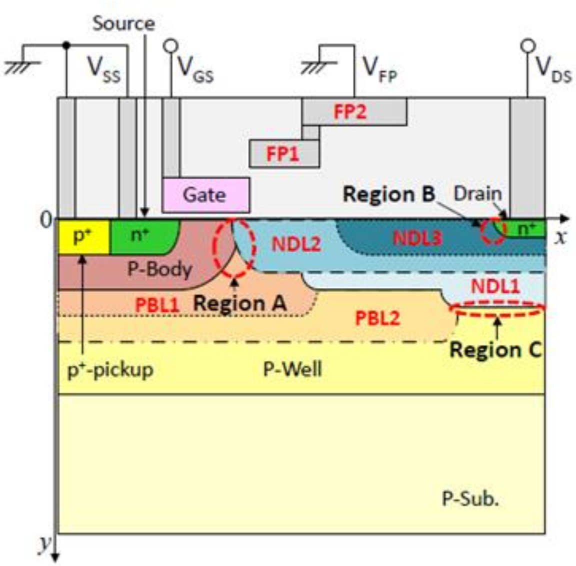


(b) ΔPBL1 edge location dependence.



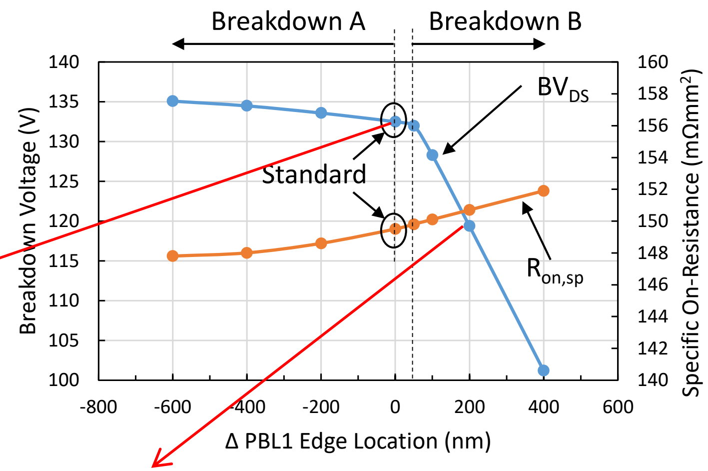
Lower tolerance limits?

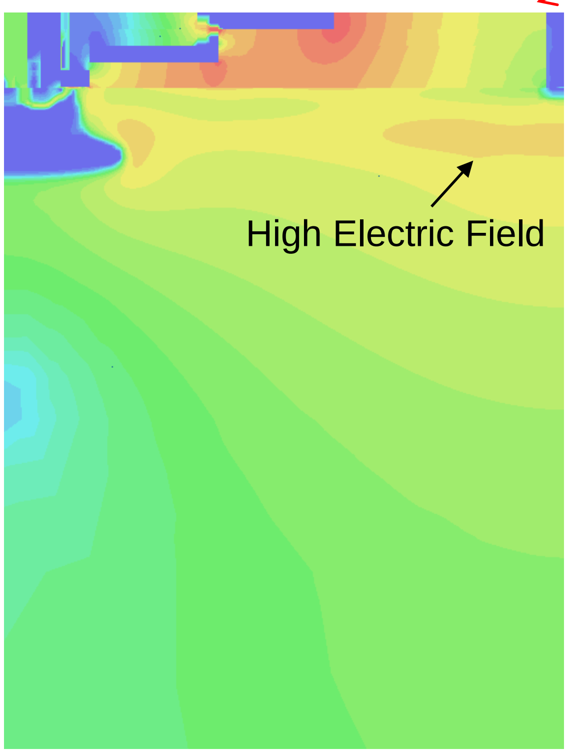
- PBL1 net dose = standard -7.50×10^{12} cm^{-2}
  ==> raises the peak by about 8 % from the standard
- PBL1 edge location = standard -50 nm
  ==> raises the peak by about 5 % from the standard

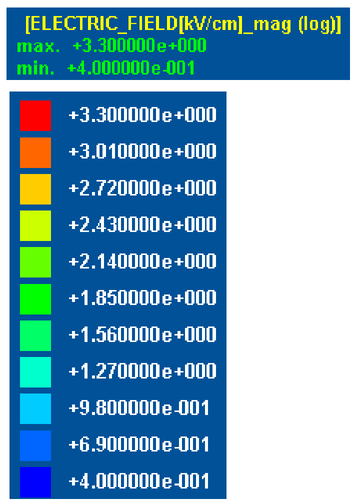
==> Too small to further deteriorate hot carrier endurance.

The electric fields upon avalanche breakdown

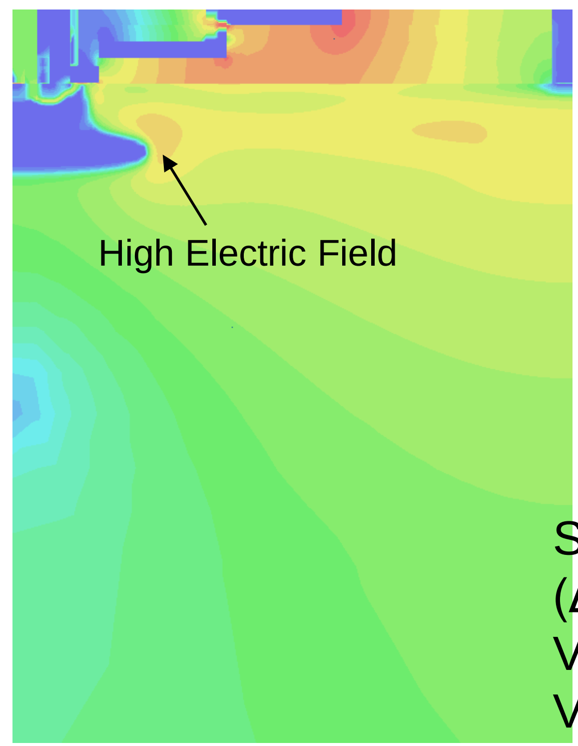
High electric field regions cause avalanche breakdown.

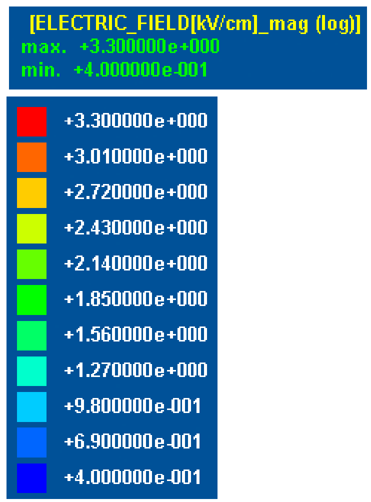






Standard
(ΔPBL1=0nm)
V_{DS}=133V
V_{GS}=0V



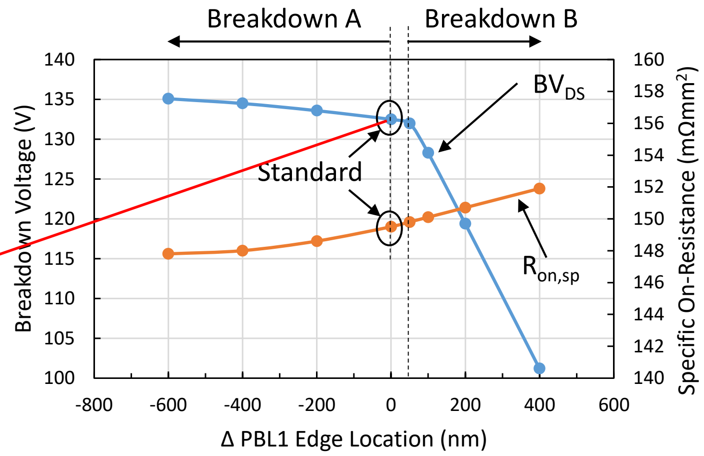


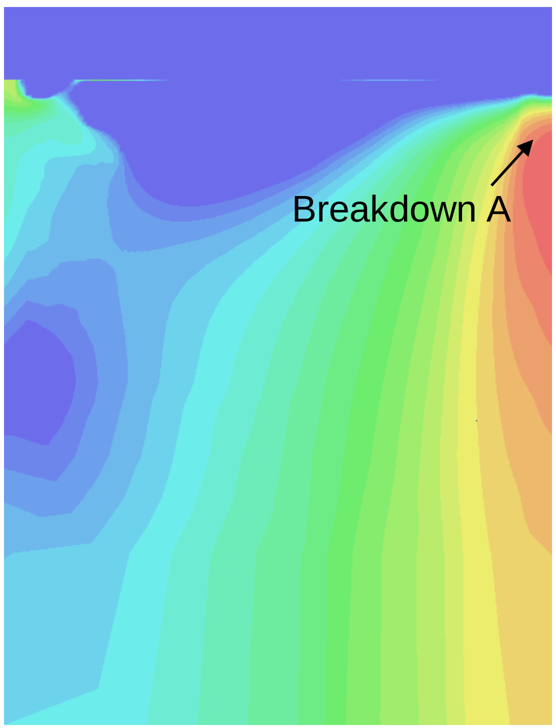
Sample
(ΔPBL1=+200nm)
V_{DS}=120V
V_{GS}=0V

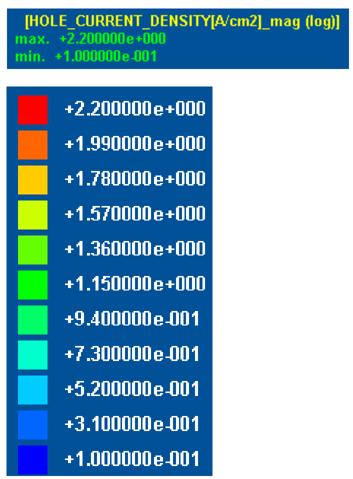
The hole current density upon avalanche breakdown

Location is far from the device

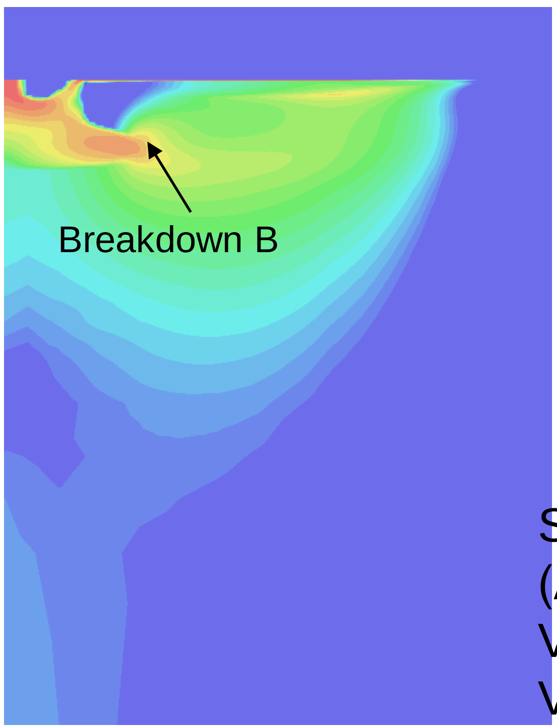
==> Breakdown A would not cause damage to the intrinsic MOSFET.

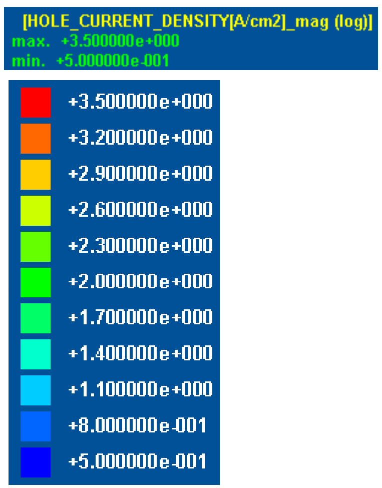






Standard
(ΔPBL1=0nm)
V_{DS}=133V
V_{GS}=0V



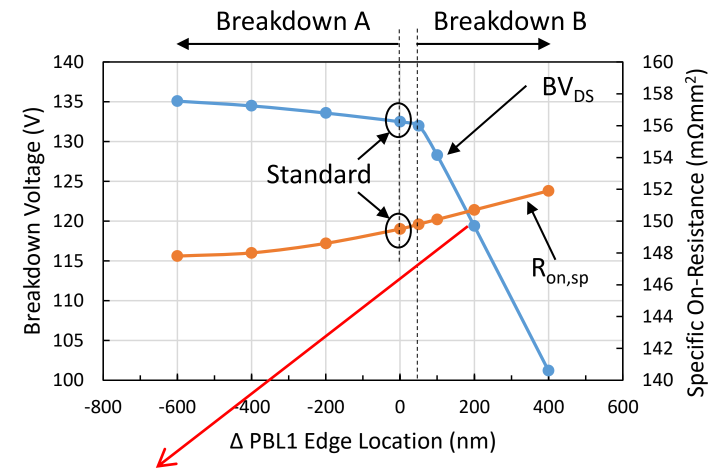


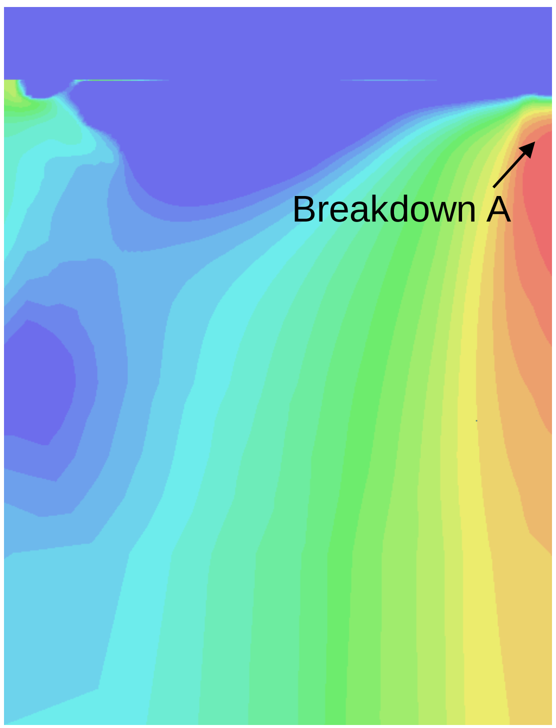
Sample
(ΔPBL1=+200nm)
V_{DS}=120V
V_{GS}=0V

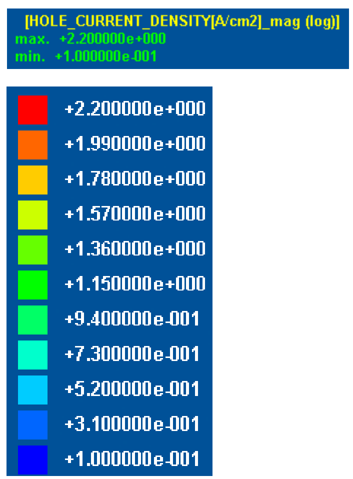
The hole current density upon avalanche breakdown

Breakdown B might cause...

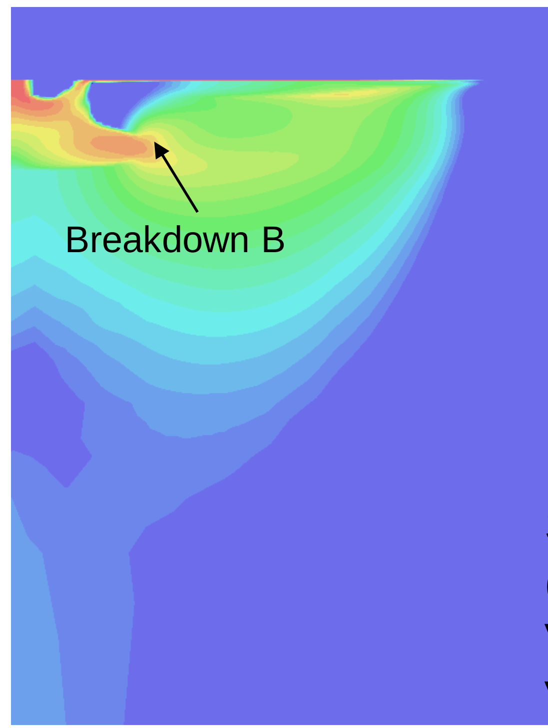
- damage to the intrinsic MOSFET.
- destruction due to filamentation in the drift region, leading to reduction of Electro Static Discharge (ESD) endurance.
  ==> however, adding ballast resistance to the drain would improve ESD endurance.

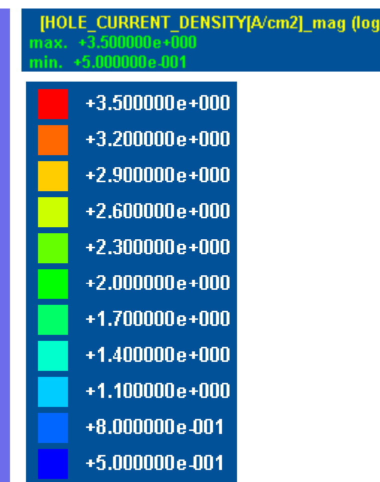






Standard
(ΔPBL1=0nm)
V_{DS}=133V
V_{GS}=0V



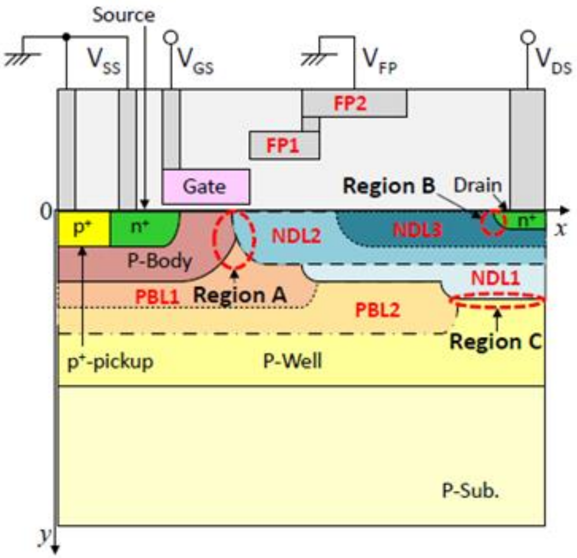


Sample
(ΔPBL1=+200nm)
V_{DS}=120V
V_{GS}=0V

Summary

- We have optimized the PBL1 net dose and the PBL1 edge location of the proposed dual RESURF 100 V LDMOS transistor for automotive applications.
- Although those parameters of PBL1 significantly affect electrical characteristics (BV_{DS}, $R_{on,sp}$, CE, and hot carrier endurance), we can obtain top-level characteristics of BV_{DS} and $R_{on,sp}$ with keeping sufficiently suppressed CE and high hot carrier endurance even in the wide range tolerances of the parameters for mass production.

- In future, we will proceed to optimization of other parameters.



Acknowledgments

- We would like to express sincere thanks to AdvanceSoft Corporation for providing us some licenses of using a 3D TCAD simulator. The development of this simulator is assisted by Japan Science and Technology Agency, National Research and Development Agency using A-STEP program.