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Time Domain Signal Processing Techniques and Their Applications

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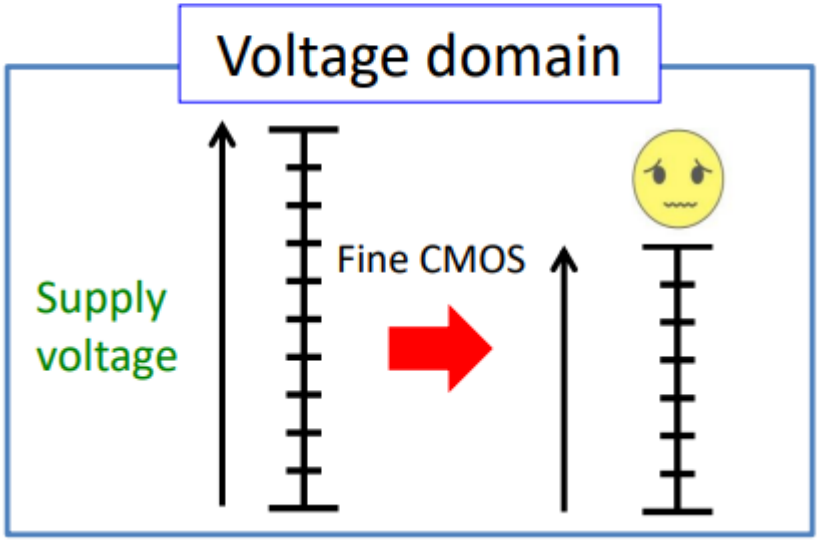
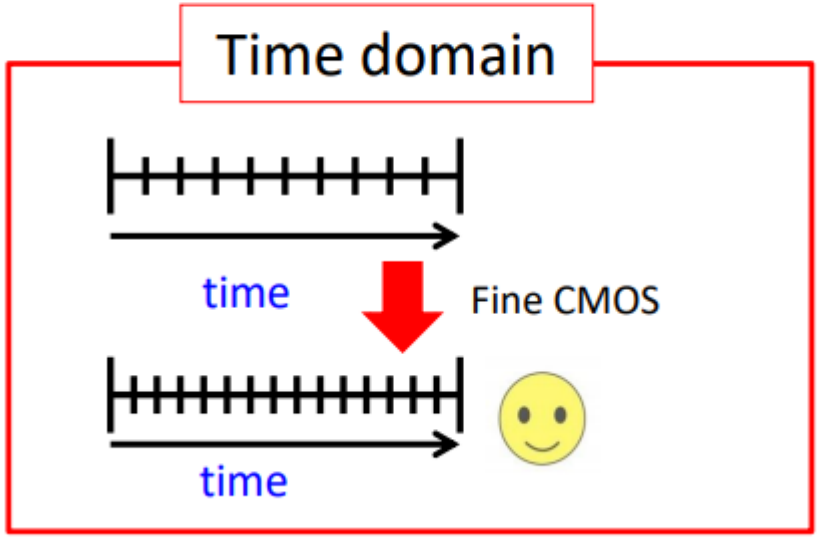
Research Background

Advanced CMOS VLSI

- Low power-supply voltages
- Fast switching speeds





Much attention is being paid to

Time domain analog signal processing

In nano-CMOS technology era.

Features of Time Domain Processing (1)

- Dynamic range of time domain signal processing can be very wide.

Time continues indefinitely

Time flies like an arrow

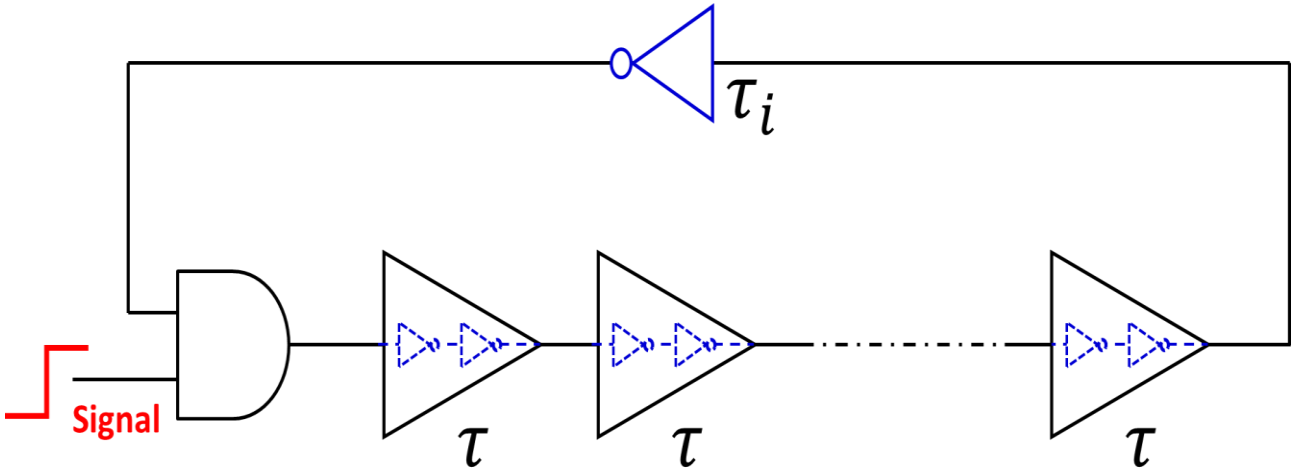
Features of Time Domain Processing (2)

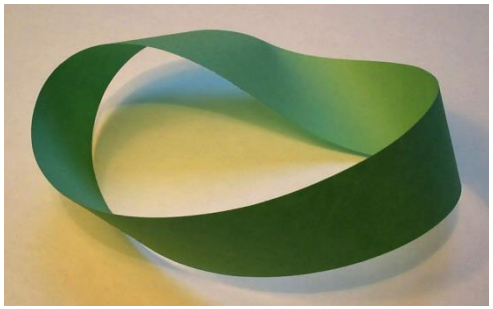
- Synchronization among clocks

  Similar to gears

Features of Time Domain Processing (3)

- Ring oscillator





Möbius strip

Myth and Truth for Time Signal

- Time hold circuit

Myth : Time cannot be held.

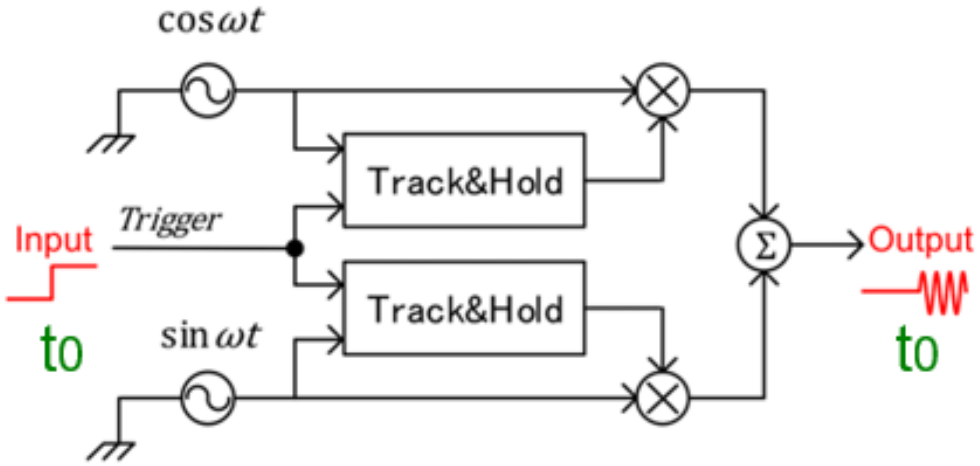
Truth: It can be held.

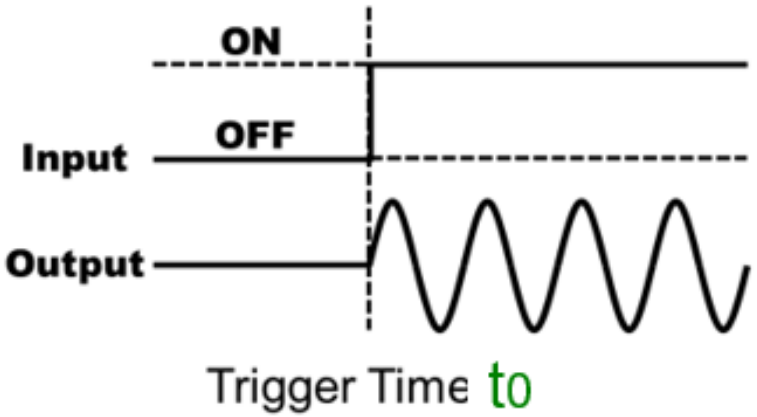
- Time amplifier circuit

Myth : Time cannot be amplified.

Truth: It can be amplified.

Trigger Circuit

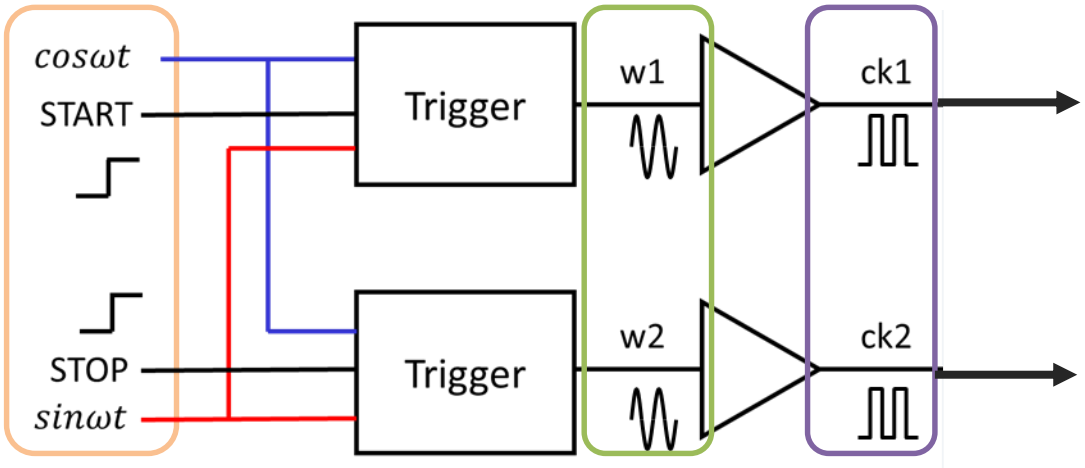


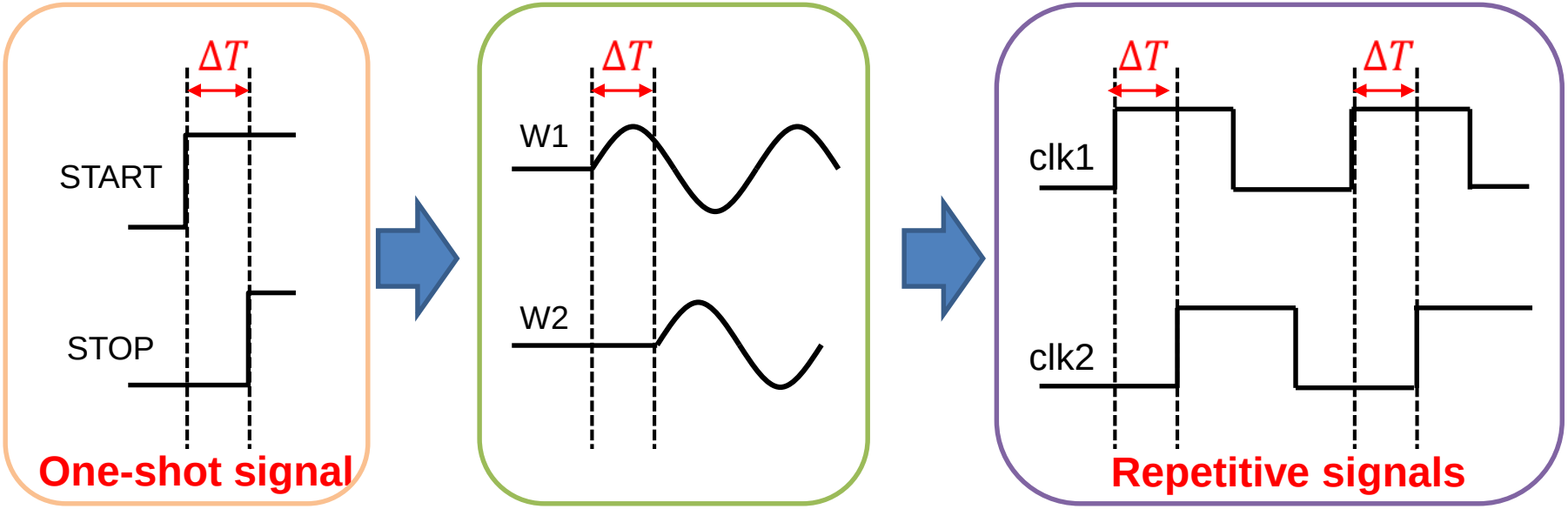


- Output starts to oscillate at rising timing edge of input

[1] M. Nelson (Tektronics)
"A New Technique for Low-Jitter Measurements Using Equivalent-Time Sampling Oscilloscope"
Automatic RF Techniques Group 56th Measurement (Dec. 2000)

Time difference can be held !





Equivalent-Time Sampling

In a sampling oscilloscope,
a repetitive high-frequency waveform can be sampled with low-frequency sampling clock and reconstructed.

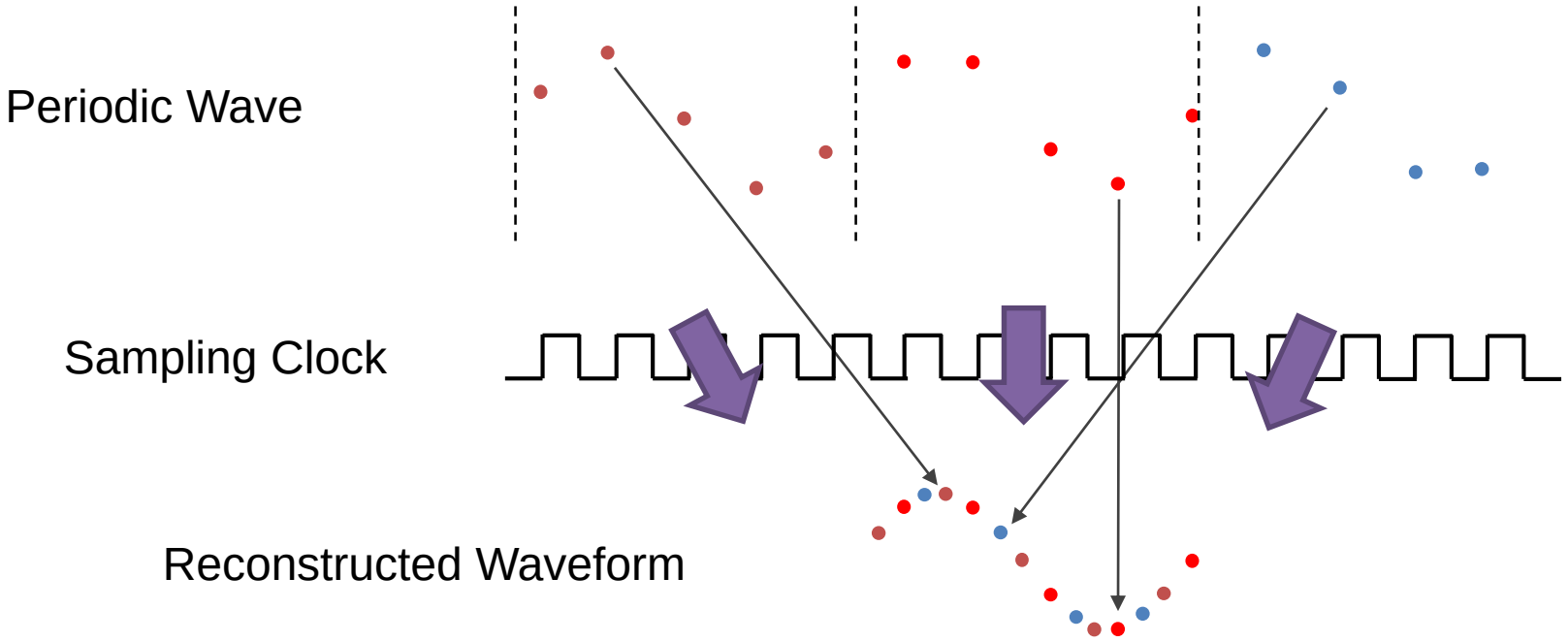
3 time-bases

① Coherent Sampling
for periodic waveform

② Sequential Sampling
for repetitive waveform, w/o pre-trigger function

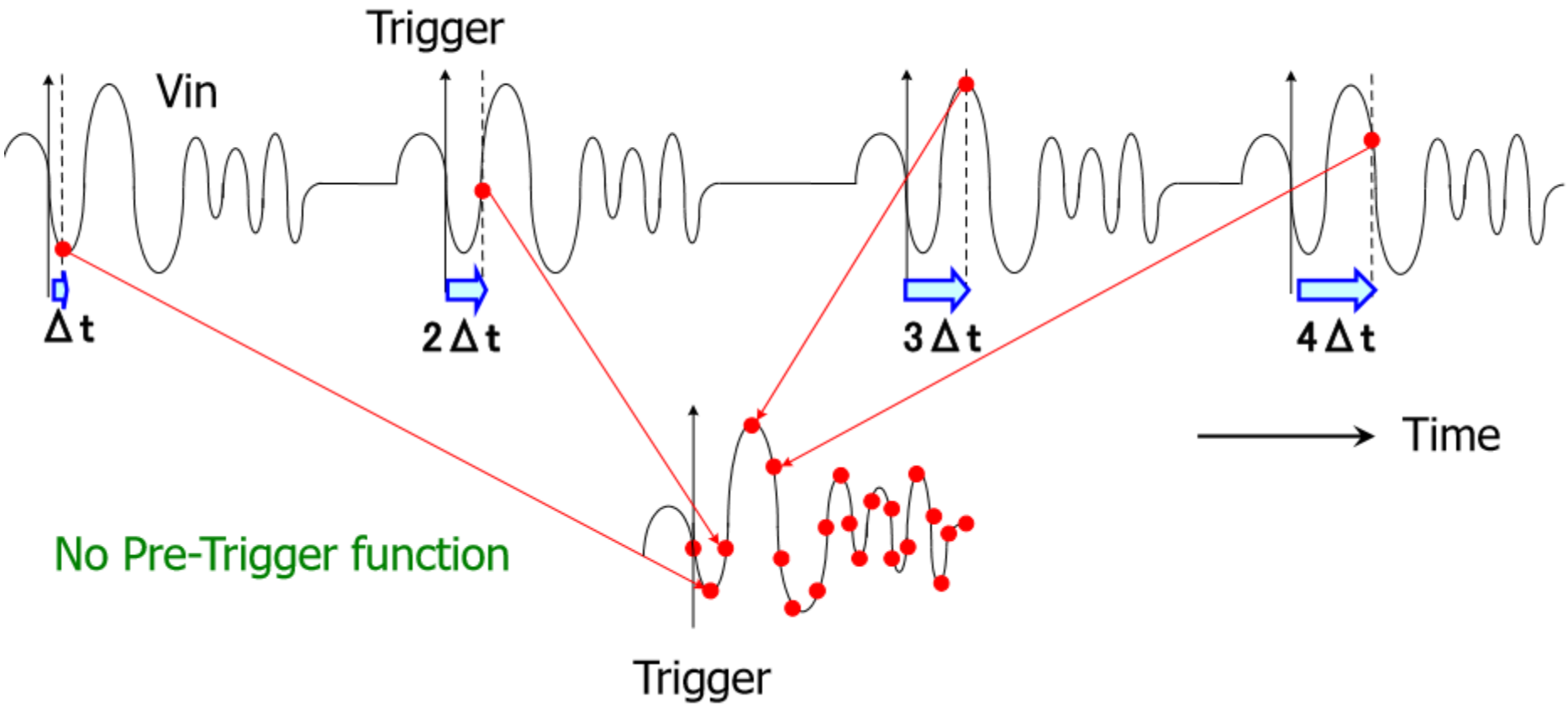
③ Random Sampling
for repetitive waveform, w/ pre-trigger function

Coherent Sampling

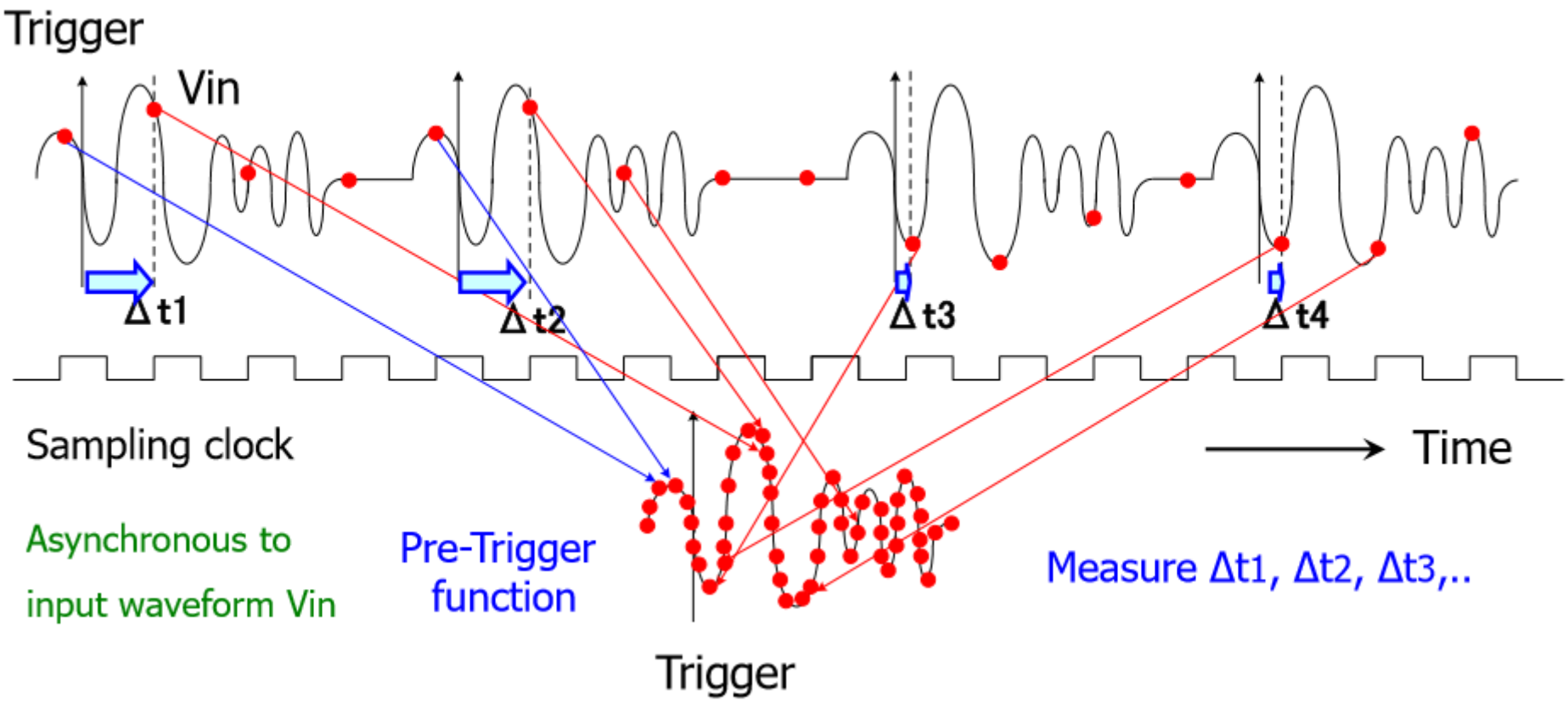


Finer time resolution than sampling clock period

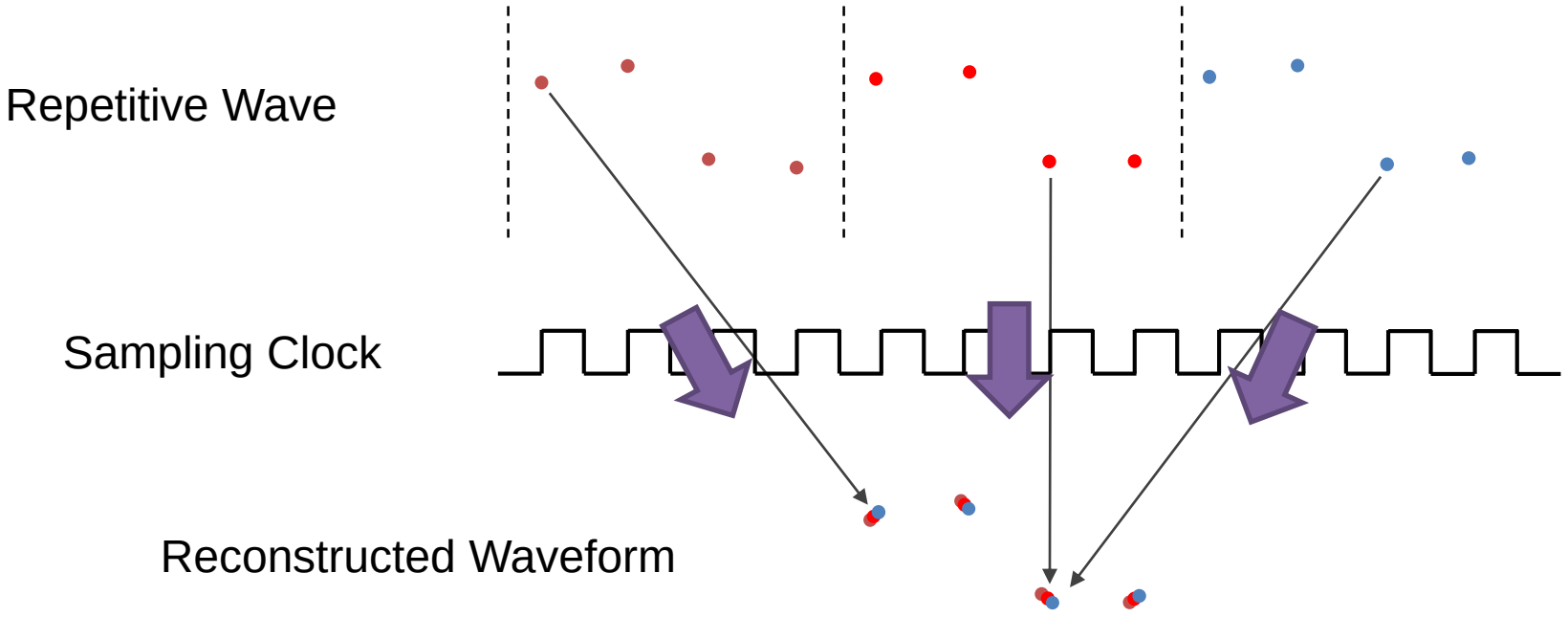
Sequential Sampling



Random Sampling



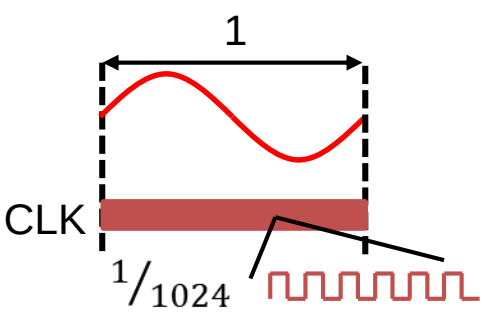
Waveform Missing Phenomena

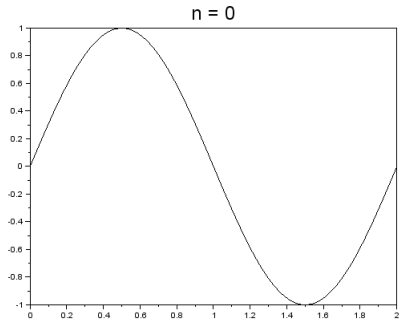


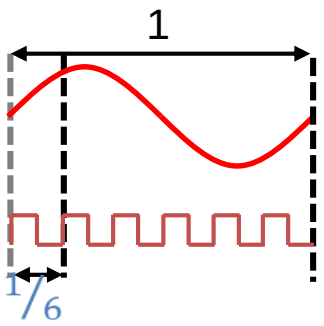
Toothless waveform appears

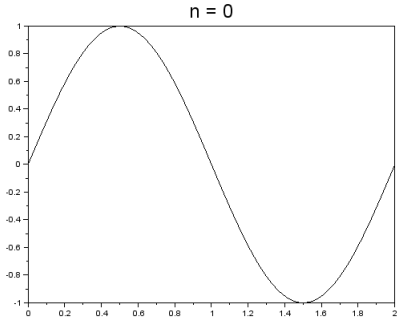
Waveform Missing Conditions

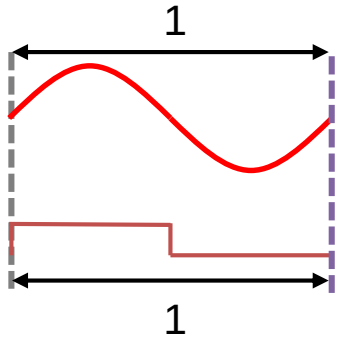
$f_{CLK} \gg f_{sin}$ $\quad f_{CLK} \approx \frac{1}{\alpha} f_{sin} \left(\alpha = 1, \frac{1}{2}, \frac{1}{3}, \frac{2}{3}, \cdots, \frac{1}{6}, \cdots\right)$ $\quad f_{CLK} \approx f_{sin}$

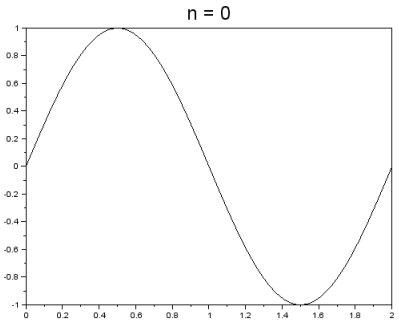






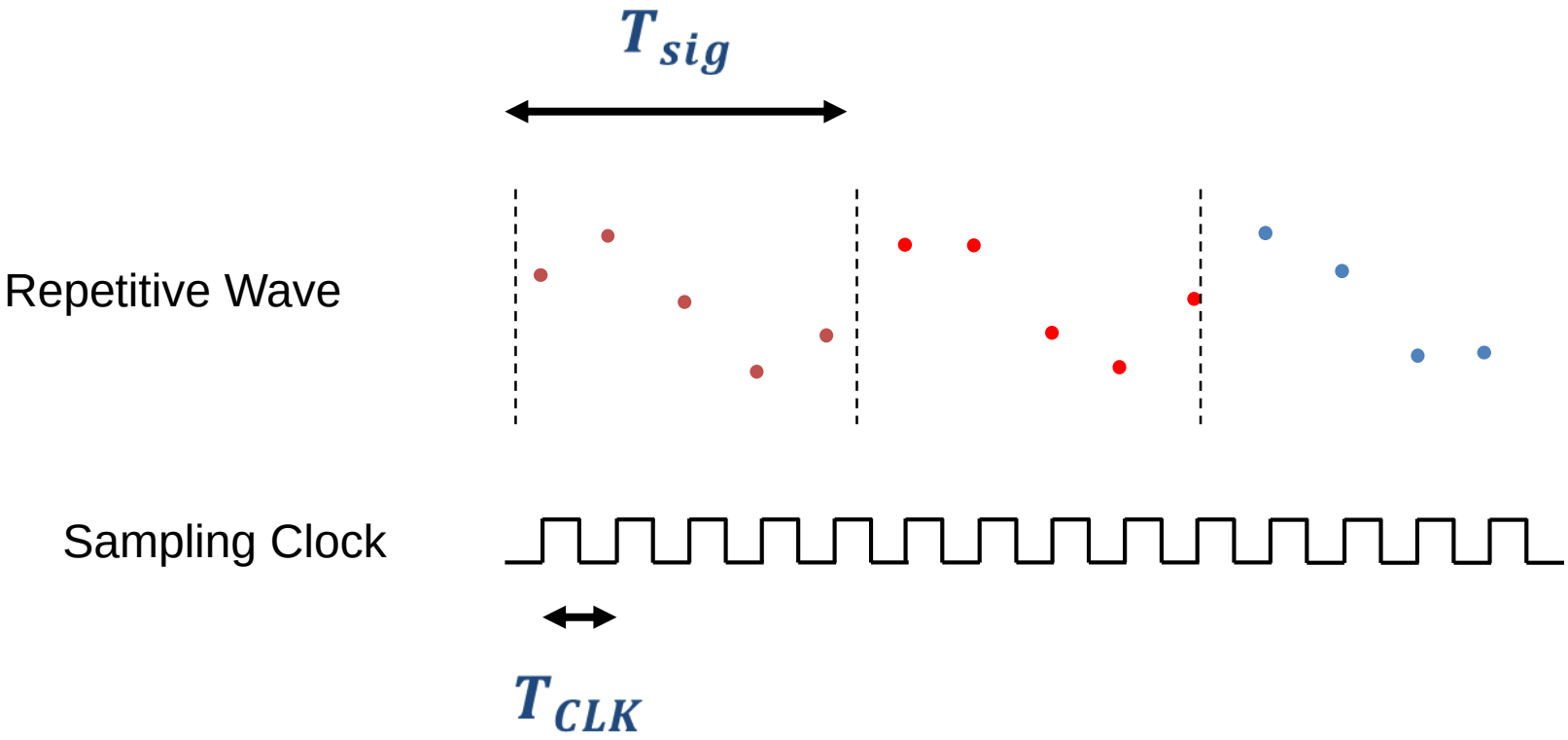






Sampling points move little ➡ Requires long time

Waveform Sampling Condition



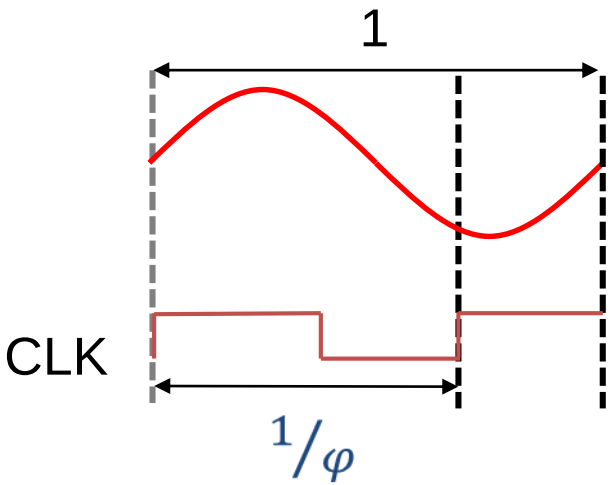
$$T_{CLK} = \ ? \ \times T_{sig}$$

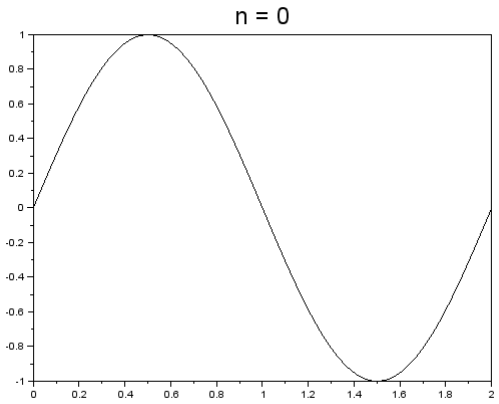
[1] Y. Sasaki, Y. Zhao, A. Kuwana, H. Kobayashi,
"Highly Efficient Waveform Acquisition Condition in Equivalent-Time Sampling System“
27th IEEE Asian Test Symposium, Hefei, Anhui, China (Oct. 2018)

Our Proposed Optimal Condition

$$f_{CLK} = \varphi \times f_{sig}$$

φ : Golden ratio (= 1.6180339887…)

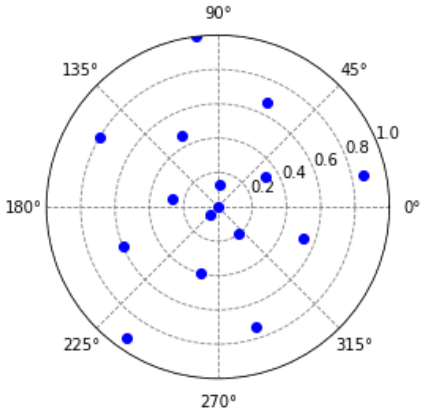


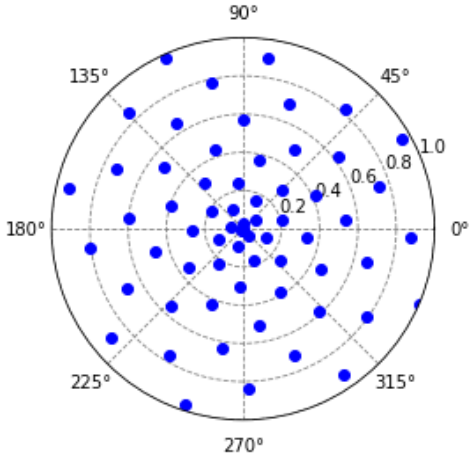


Sampling points disperse uniformly through measurement

Time versus Phase with Optimal Sampling

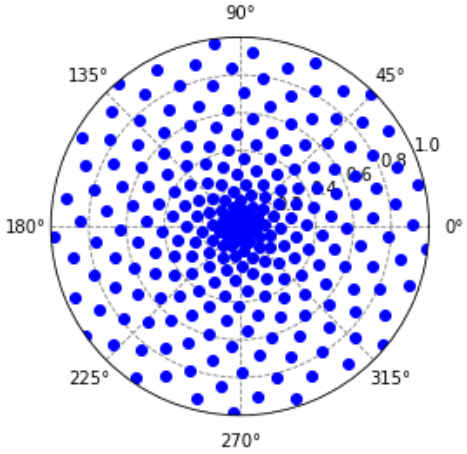
16 pt.

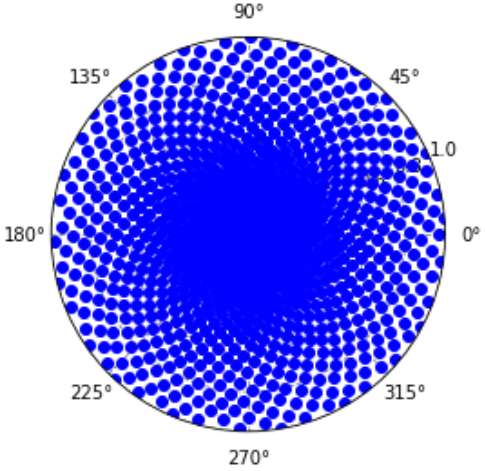




64 pt.

256 pt.



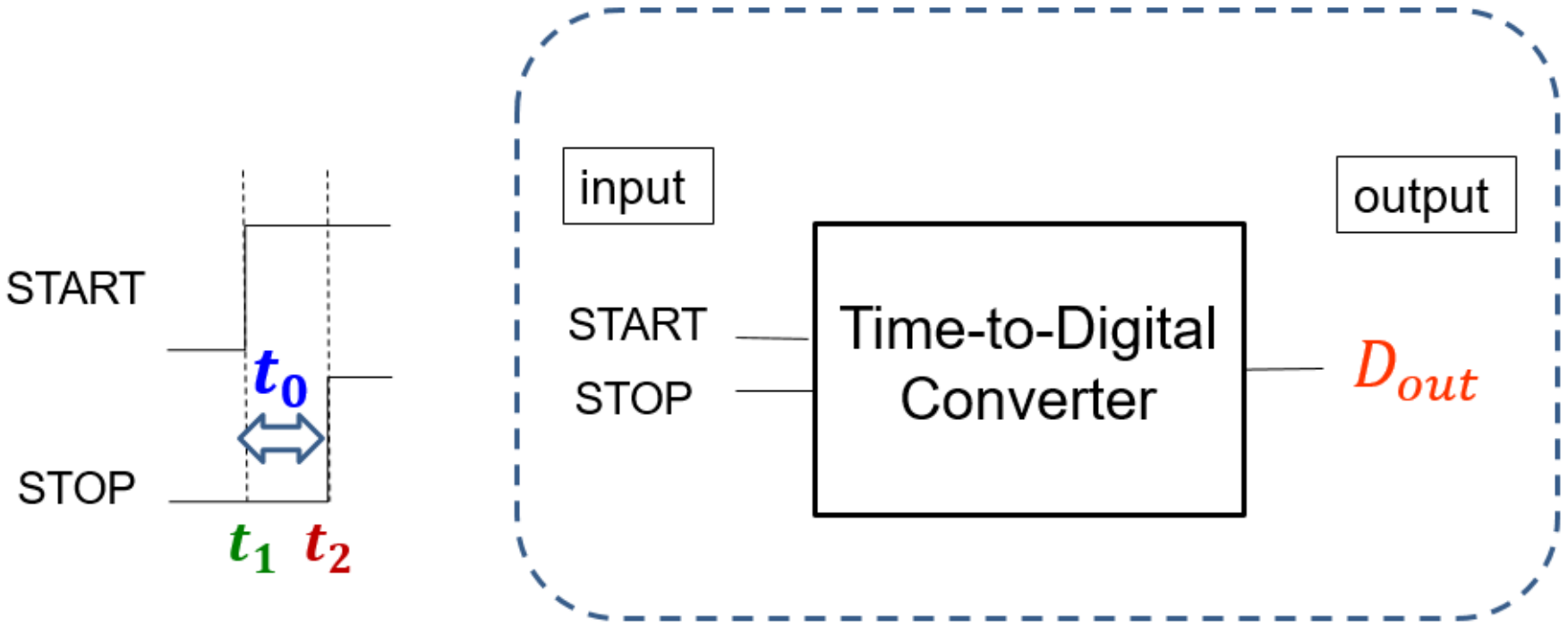


1024 pt.

Radius: Normalized time progress Phase: Input sinewave phase

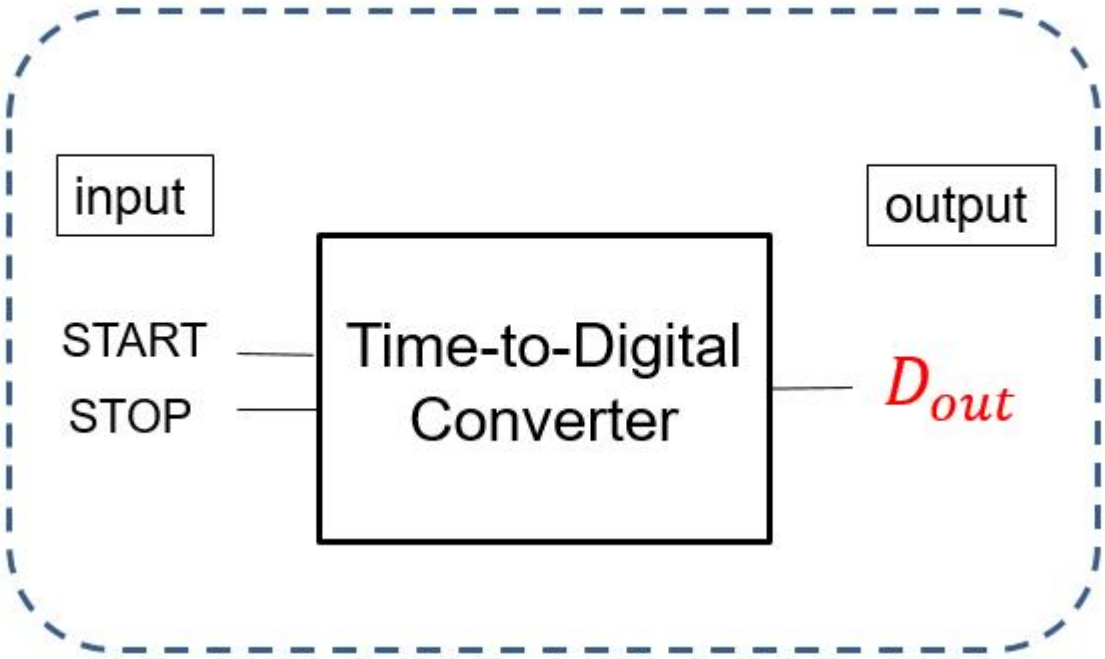
Dots are filled uniformly in Gaussian plane.

Time-to-Digital Converter

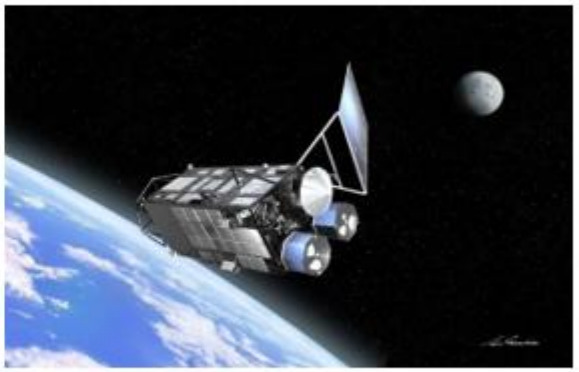


- Time-to-digital converter (TDC) measures **timing difference t_0** between t_1 , t_2 as a **digital value D_{out}**

TDC Application Examples



Inter-vehicular distance measurement

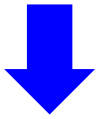


Satellite distance measurement

Target TDC Architectures

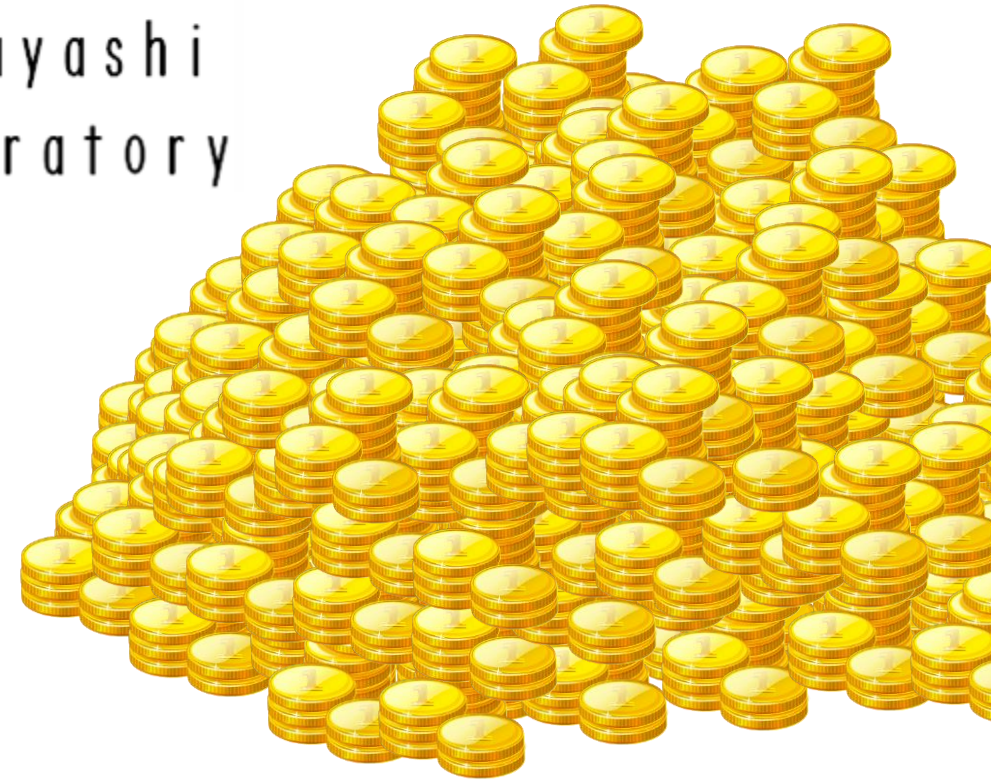
TDC architectures have been inspired by ADC architectures

Flash TDC	⟺	Flash ADC
SAR TDC	⟺	SAR ADC
Integral-type TDC	⟺	Integral-type ADC
ΔΣ TDC	⟺	ΔΣ ADC



Slow but very fine time resolution

Conclusion: Time is GOLD !!

Kobayashi Laboratory

Varieties of time domain signal processing techniques