

並列配置された低ゲイン増幅器による 閉ループ利得の補償



t160d031@gunma-u.ac.jp <u>荻原 岳,</u>桑名 杏奈,小林 春夫 (群馬大学)

1.Reserch Background



2. Investigated Circuit



Circuit Assumption

- **Resistance values of R1 .. Rn are fixed.**
- Resistance values of R'1 .. R'n are adjusted

according to the desired amplification factor.

All operational amplifiers have almost the same gain without offsets.

Operation Explanation

(1) Amplifies the inverting input potential

of the previous stage operational amplifier.

2 Outputs at each stage are de-multiplexed, converted to digital and added by DSP.

3.Simulation Results

Simulation Result 1

Simulation Result 2

Errors for Low Open Loop Gain





Number of stages



4.Conclusions

Conventional Amplifier

- Low gain operational amplifier \rightarrow Inaccurate output ullet
- High gain operational amplifier \rightarrow Sufficient accuracy



Parallel Low-Gain Amplifiers

Low gain operational amplifier \rightarrow Approximate to ideal value \bullet

5.Future Works

- **Experiments using actual circuits**
- Effect of changing load resistance
- **Theoretical analysis**

for parallel low-gain amplifiers

6.Reference



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Middle gain operational amplifier \rightarrow Higher precision gain lacksquare



[1] Texas Instruments, Handbook of Operational Amplifier Applications (Rev. B), SBOA092B, Bruce Carter, Thomas R. Brown, October 2001.