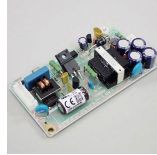
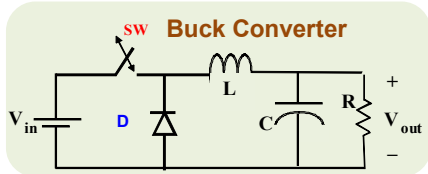


1. Research Objective

Solving problems:

- Output voltage overshoot
- Output voltage ripple



2. Research Background

- Conventional method of overshoot reduction : a feedback loop [1]
- Ripple reduction: spread spectrum of pulse width modulation (PWM)[2]
- Proposed overshoot reduction technique: a parallel RLC network

3. Proposed Design of Buck Converter

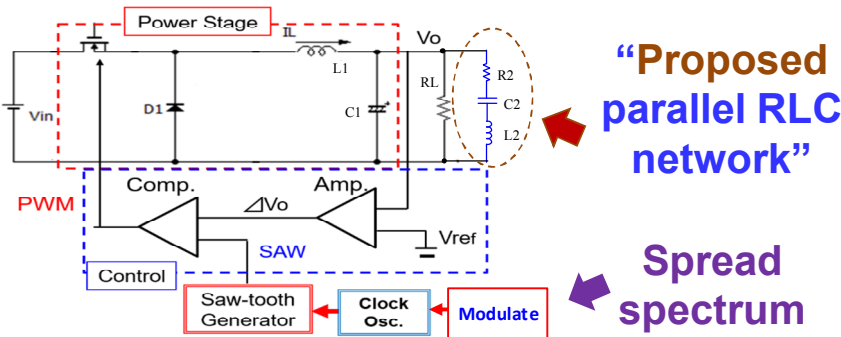


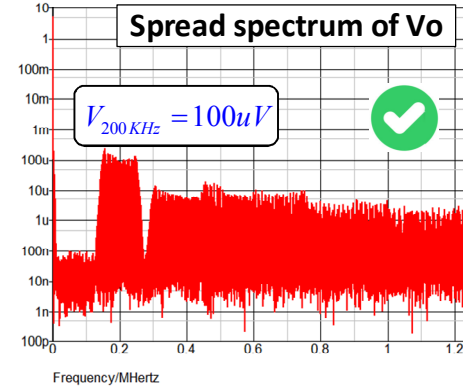
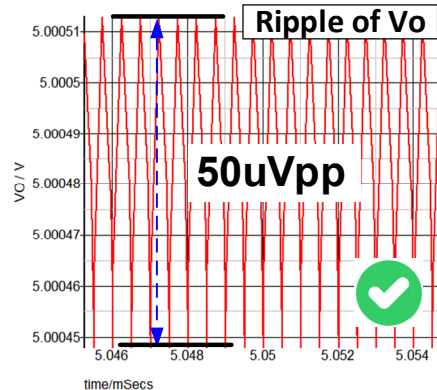
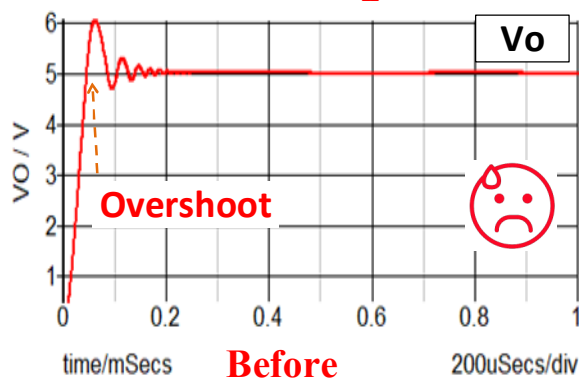
Table.1: Operation parameters

Input Voltage (Vin)	12V
Output Voltage (Vo)	5.0V
Output Current (Io)	1A
Clock Frequency (Fck)	200kHz

4. Simulation Results

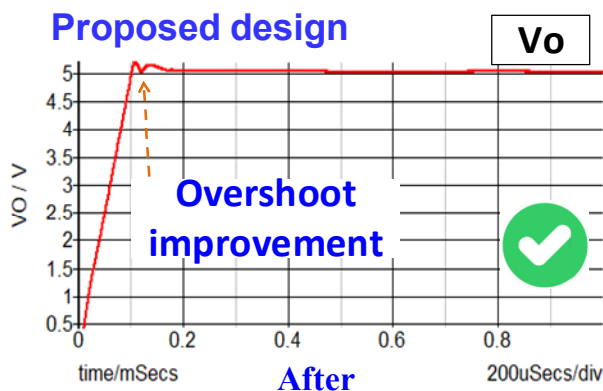
- Overshoot reduction: 1Vpp → 0.1Vpp
- Small ripple: 50μVpp → Low spectrum: 100μV

Conventional design



with parallel RLC

Proposed design



5. Summary

- Voltage overshoot is improved by a parallel RLC (< 0.1Vpp).
- Ripple is kept very small (50μVpp) based on spread spectrum of PWM.
- Ripple spectrum are very low (100μV).

References

- [1] H. Kobayashi, T. Nabeshima (Editors), Handbook of Power Management Circuits, Pan Stanford Publisher (2016).
- [2] Minh Tri Tran, N. Miki, Y. Sun, Y. Kobori, H. Kobayashi, "EMI Reduction and Output Ripple Improvement of Switching DC-DC Converters with Linear Swept Frequency Modulation", IEEE 14th International Conference on Solid-State and Integrated Circuit Technology, (Qingdao, China) Nov. 2018.