3B-06

High Resolution Time-to-Digital Converter Using Integral Architecture and Vernier Oscillators

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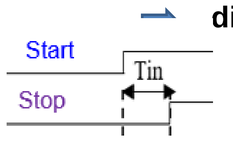
1.Research Objective

Research for time-to-digital converter architectures with Vernier oscillators

- **Time Measurement between Start and Stop rising edges → digital output *Dout***



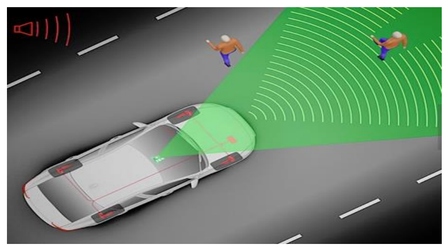
- **Inspired by integration-type ADC**
- **Two oscillators with different frequencies**

  Fine time resolution $T1 - T2$

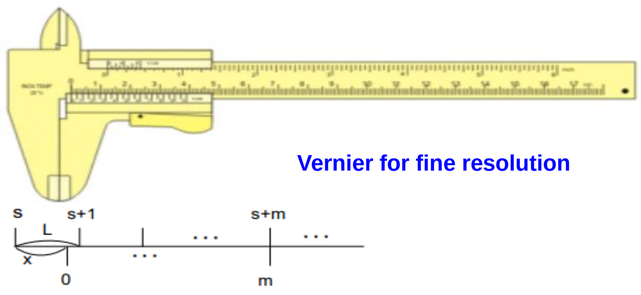
  $T1 = 1/f1$, $T2 = 1/f2$
- **Simple circuit**
- **Good linearity without calibration**

2.TDC＆Vernier Application Examples

Radar distance measurement



Vehicle distance measurement



Vernier for fine resolution

Tram arrival time

Taking the scale of the minor scale

$$L' = \frac{n-1}{n}L \qquad \cdots(1)$$

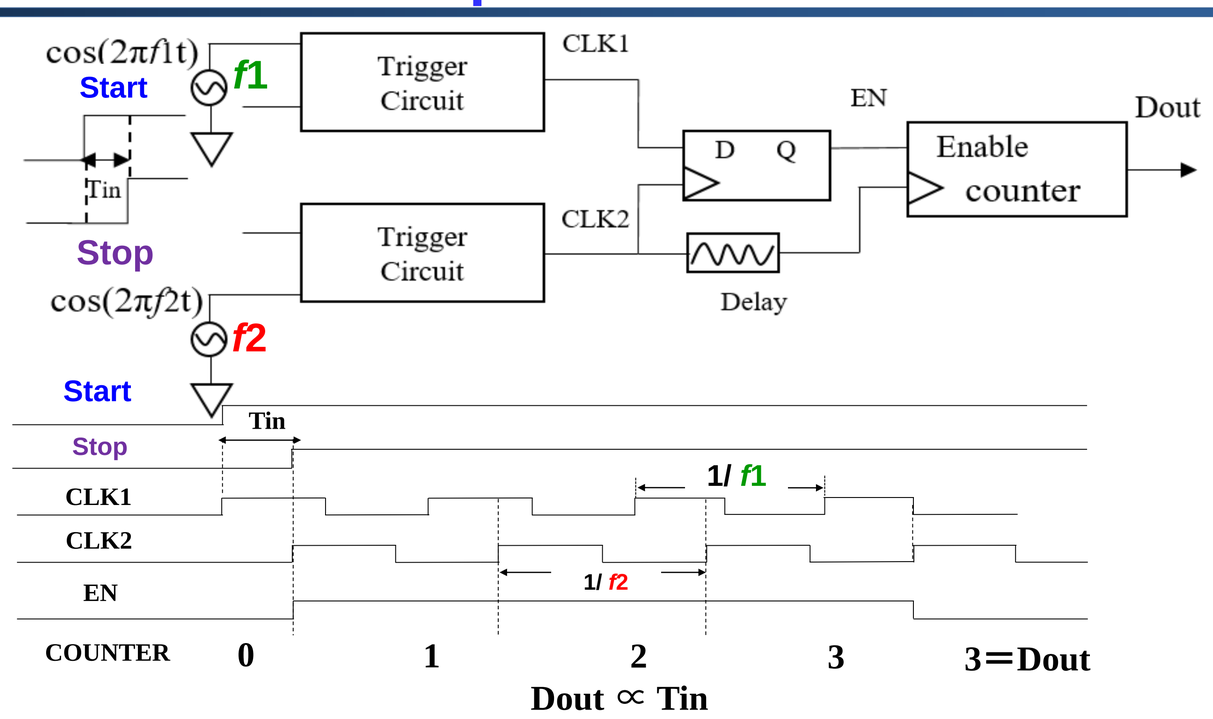
As shown in the figure

$$((s+m)-s)L = x + mL' \qquad \cdots(2)$$

$$mL = x + m\frac{n-1}{n}L$$

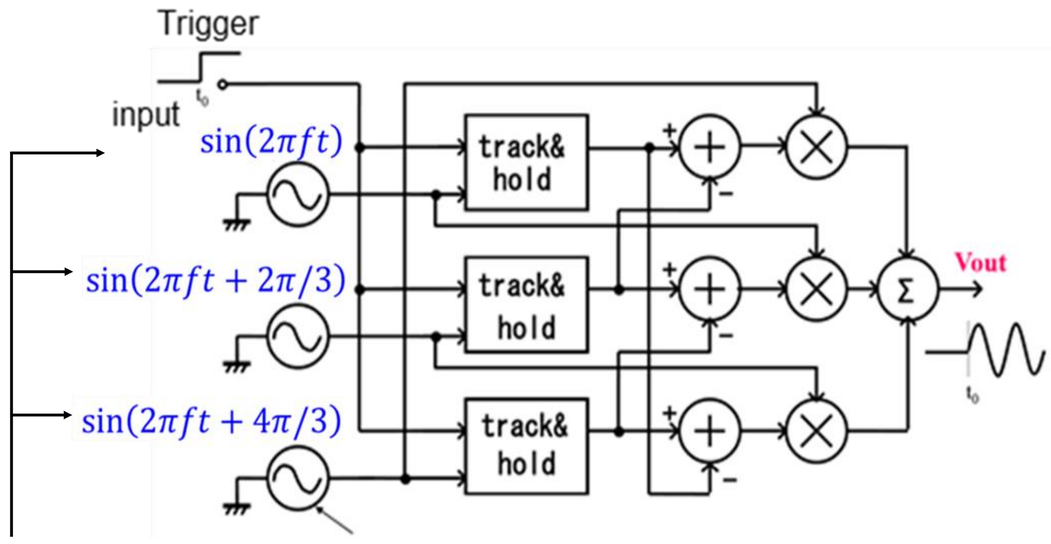
$$x = \frac{L}{n}m \qquad \cdots(3)$$

3.Proposed Circuit

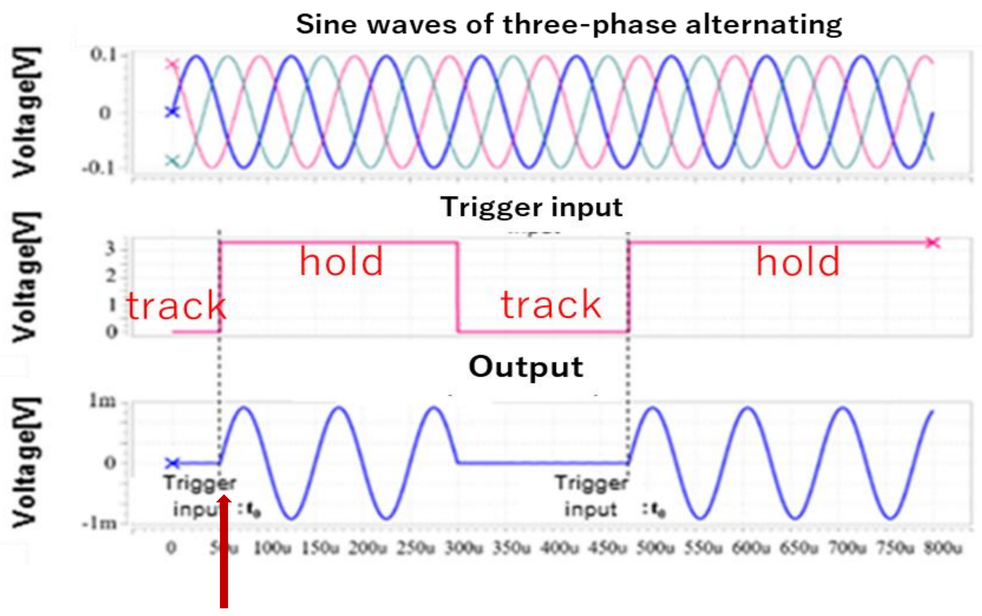


Dout ∝ Tin

4.Trigger Circuit＆Simulation Results

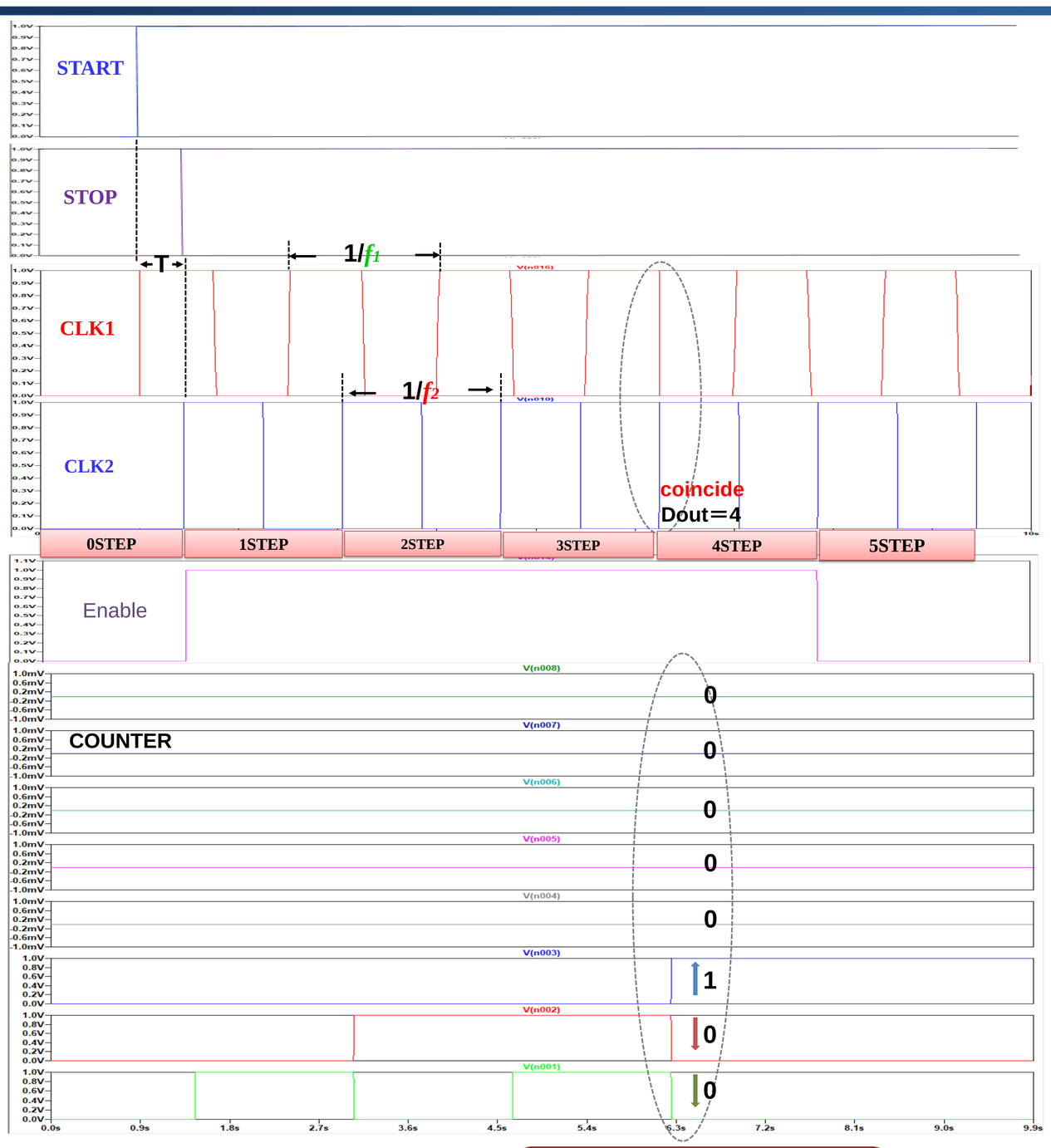


Enter three sine waves



Output starts to oscillate at the rising time edge of trigger input

5.Simulation Results



Counter output results is 00000100

Binary number → Octal number

00000100＝4

Dout × ｜1/*f1*-1/*f2*｜＝T

Period difference＝0.1 ps × 4 ＝0.4 ps

6.Conclusion

- **New time-to-digital converter architecture**
  - **Accurate fine time resolution of 1/*f1* – 1/*f2***
  - **Good overall linearity without calibration**
  - **Long measurement time**
  - **Operation is confirmed with simulation**

ありがとうございます。

Thank you