3B-07

ΔΣAD Converter Linearity Test Algorithm using FFT Method

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1. Research Objective

High resolution, low speed ΔΣ ADC

- Sensor interface key components
- Mass production test

Our Studies

✓ Linearity test takes a long time..

High reliability requirements

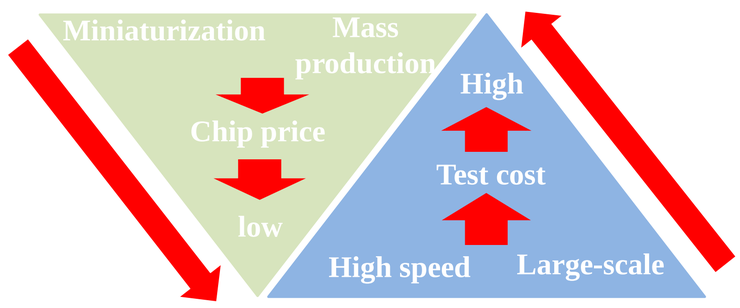
✓ Perform its linearity test in a short time

✓ Develop its algorithm

2. Research Background

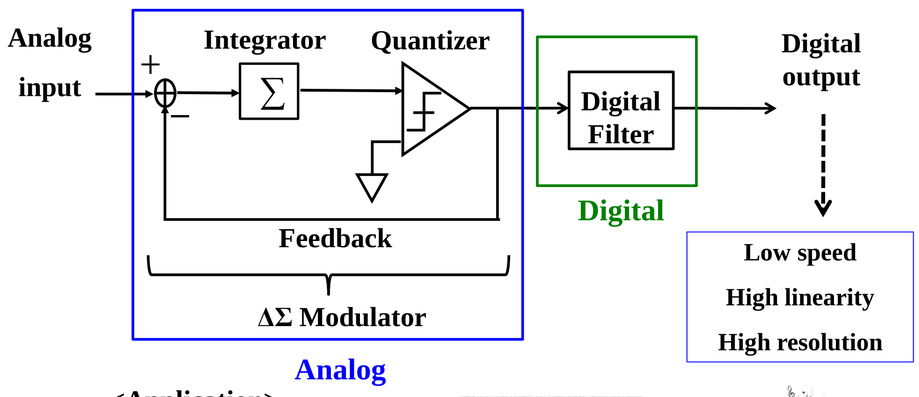
IOT（Internet of things）

Testing of IOT devices ➡ important.



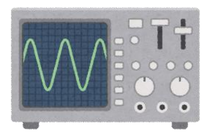
Mass production shipment of IOT devices requires high quality & low cost testing.

ΔΣ ADC

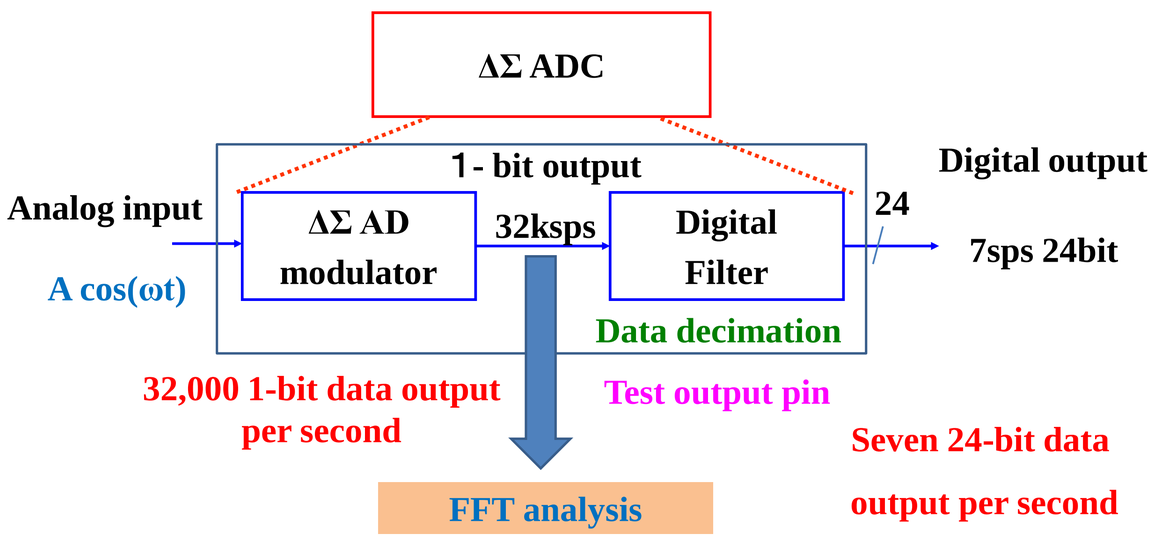


<Application>

- Measurement
- Audio system

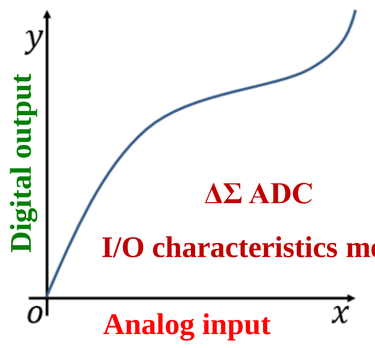


3. Proposed Test Method



4. Calculation of Polynomial Coefficients

$$y = a_0 + a_1x + a_2x^2 + \cdots + a_nx^n$$



ΔΣ ADC

I/O characteristics model

Cosine input : $x(t) = A_0\cos\omega t$

Output characteristic model : $y(t) = a_1x(t) + a_3x(t)^3$

3td order model for simplicity :

$$y(t) = a_1x(t) + a_3x(t)^3$$

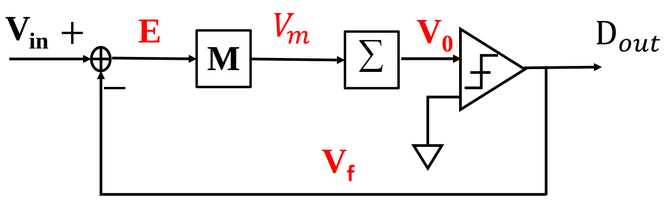
$$y(t) = (a_1A_0 + \frac{3}{4}a_3{A_0}^3)cos\omega_0t$$ Fundamental

$$+\frac{1}{4}a_3{A_0}^3cos3\omega_0t$$ 3rd harmonics

5. Modulator 3th-order Nonlinearity Model

3th-order nonlinearity model

$$V_m = \mathrm{E} - k * \mathrm{E}^3 \ (\mathrm{k}>0)$$



$$\mathrm{E(n)} = \mathrm{V_{in}(n)} - \mathrm{V_f(n)}$$

$$\mathrm{V_m(n)} = \mathrm{E(n)} - k * \mathrm{E(n)^3} \ (\mathrm{k} > 0)$$

$$\mathrm{V_o(n)} = \mathrm{V_o(n-1)} + \mathrm{V_m(n)}$$

If $\mathrm{V_o(n)} \geq 0;$

$$\mathrm{D_{out}(n+1)} = 1;\ \mathrm{V_f(n+1)} = 1$$

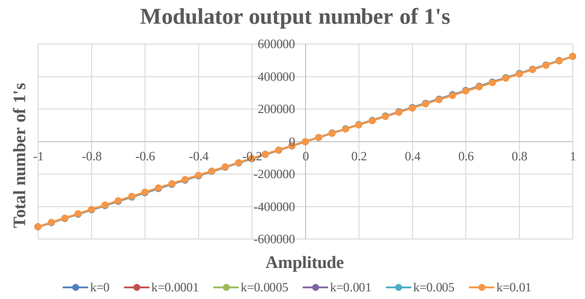
Else $\mathrm{D_{out}(n+1)} = 0;\ \mathrm{V_f(n+1)} = -1$

6-1. Simulation Verification

20-bit first-order LP case

DC Input Simulation Configuration:

- **The number of data** : $N=2^{20}$
- V_{in} : **DC= -1.0 ～ +1.0**
- **K=0.0001, 0.0005, 0.001**
  0.005, 0.01



Estimated coefficient values in polynomial model of ΔΣAD modulator
DC input/input characteristics

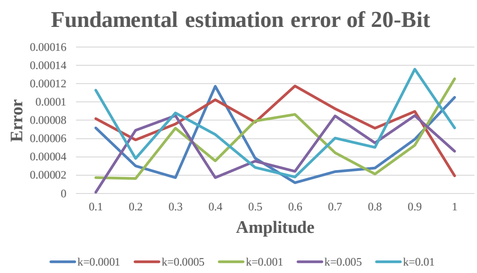
k	a_3	a_2	a_1	c
0.0001	104.84	0.16206	524180	-0.032331
0.0005	524.48	0.16206	523760	-0.032331
0.001	1050.5	0.16206	523240	-0.032331
0.005	5282.5	0.16206	519000	-0.032331
0.01	10643	0.16206	513610	-0.032331

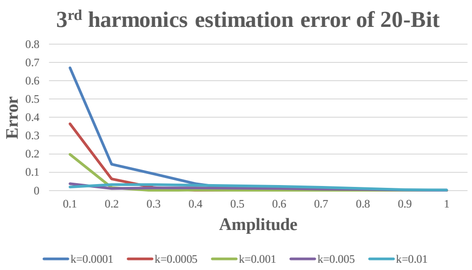
6-2. Simulation Results

20-bit first-order Low-Pass case

Cosine Input Simulation Configuration:

- **The number of data** : $N = 2^{20}$
- V_{in} : $A_0\cos(\omega t)$ $(A = 0.1 \sim 1)$
- **K = 0.0001, 0.0005, 0.001,**
  0.005, 0.01





7. Conclusion

- **High resolution, low speed ΔΣ ADC linearity short time test algorithm**
- ✓**Modeling by polynomial of modulator input / output characteristics**
- ✓**FFT of modulator 1-bit output stream for cosine input**
- ✓**Estimate polynomial coefficients from fundamental and harmonic powers**
- **Verified by simulation with a simple model**
- **Also verified by experiment, which will be reported.**