4B-03

General Configuration of Non-Binary DAC Using Resistor Ladder Network

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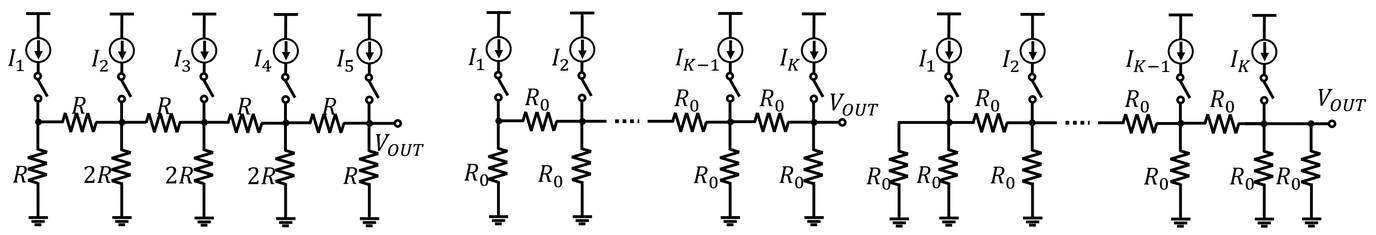
1. Objective

- Resistor ladder network is used
  - Configurations of DACs
  - Internal circuit of ADCs
  - Analog spatial filters

Developing a theory about DACs with resistor ladder

2. Background

- DAC configurations with resistor ladders
  - R-2R DAC
  - Fibonacci DAC as internal circuit of SAR ADCs



5-bit R-2R DAC

(a) Odd terms (b) Even terms

R-R Fibonacci number weighted DACs

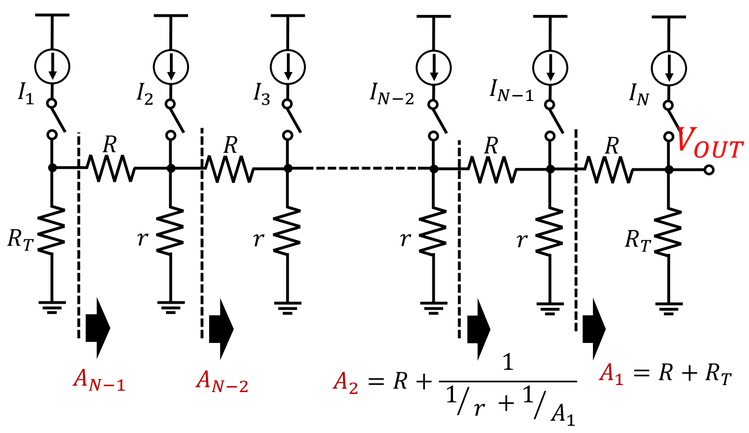
Developing unified design theory from these similar configurations of DACs

3. Circuit Analysis

- Definition of combined resistances A_n

$A_1 = R + R_T$

$A_n = R + \dfrac{1}{1/r + 1/A_{n-1}}$

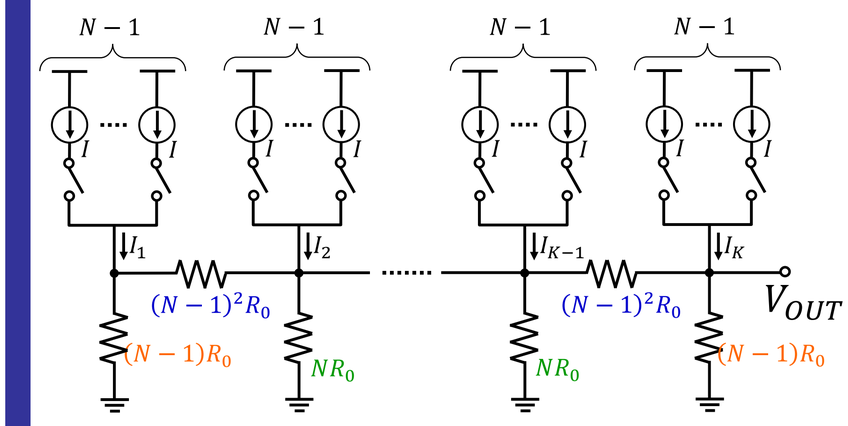


$$V_{OUT}(I_1, I_2, \cdots, I_N, R, r, R_T) = R_T \cdot \left(I_N \cdot \frac{A_{N-1}}{A_{N-1} + R_T} + I_{N-1} \cdot \frac{r||A_{N-2}}{r||A_{N-2} + A_1} + \frac{r}{A_1 + r} \right) \cdot \left(I_{N-2} \cdot \frac{r||A_{N-3}}{r||A_{N-3} + A_2} + \frac{r}{A_2 + r} \right) \cdot \left(\cdots \cdot \left(I_2 \cdot \frac{r||A_1}{r||A_1 + A_{N-2}} + \frac{r}{A_{N-2} + r} \cdot \left(I_1 \cdot \frac{R_T}{A_{N-1} + R_T} \right) \right) \cdots \right) \right)$$

Current division ratios from the left node to the right node

Current division ratio at each node / Output voltage determined by A_n and r

4. Proposal of *N*-ary DAC

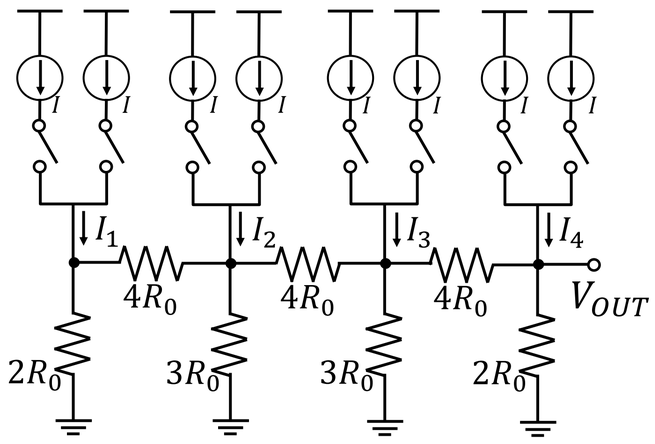


Parameters
- Provided currents $I_1, \cdots, I_K$
- Normalized resistance value R_0
- Current division ratio $N-1:1$
- Number of ladder's stages K

- Resistance ratio
  $R : r : R_T = (N-1)^2 : N : N-1$
- Output voltage
  $V_{OUT}(I_1, \cdots, I_K, R_0, N, K) = R_0 \dfrac{N(N-1)}{N+1} \sum_{k=1}^{K} \left(\dfrac{I_k}{N^{K-k}} \right)$
- Output Voltage steps : N^K
- Maximum output voltage
  $\rightarrow I_k = (N-1)I$ for all k
  $V_{MAX}(I, R_0, N, K) = R_0 I \dfrac{N(N-1)^2}{N+1} \left(1 - \dfrac{1}{N^K} \right)$
- Minimum voltage step
  $\rightarrow I_1 = I$, for others $I_k = 0$
  $V_{\min}(I, R_0, N, K) = R_0 I \dfrac{N-1}{(N+1)N^{K-2}}$

5. Examples of *N*-ary DAC

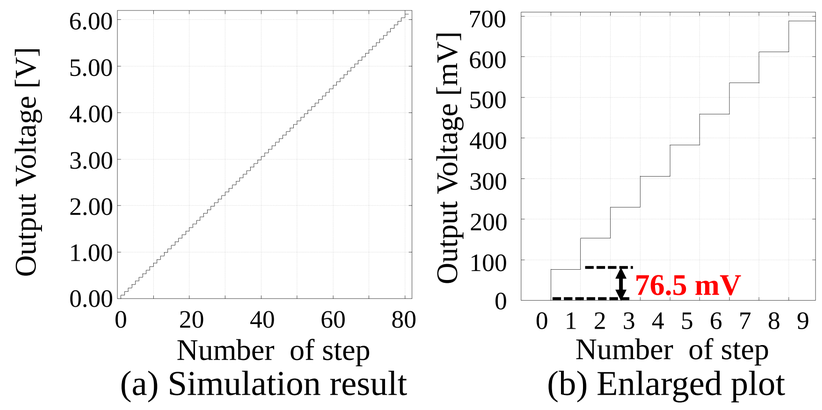
- **Ternary DAC** $N = 3$ $\quad R : r : R_T = 4R_0 : 3R_0 : 2R_0$



- Output voltage

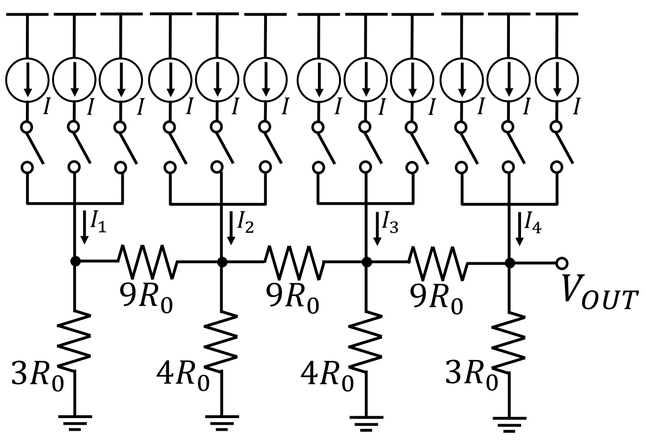
$$V_{OUT}(I_1, I_2, I_3, I_4, R_0) = R_0 \cdot \frac{3}{2} \left(I_4 + \frac{1}{3^1} I_3 + \frac{1}{3^2} I_2 + \frac{1}{3^3} I_1 \right)$$

- Simulation conditions
  - simulating ramp wave code input by switching current sources
  - $R_0 = 100\ \Omega$, $I = 13.77$ mA
- Design value : $V_{MAX} = 6.12$ V, $V_{\min} = 76.5$ mV



(a) Simulation result (b) Enlarged plot

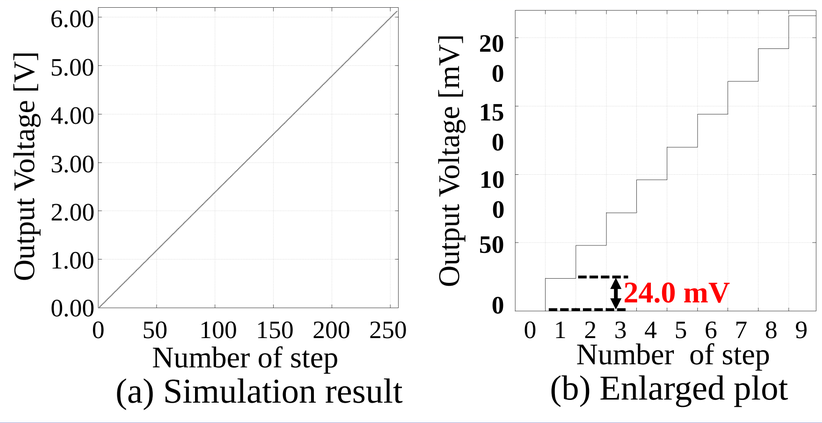
- **Quaternary DAC** $N = 4$
  $R : r : R_T = 9R_0 : 4R_0 : 3R_0$



- Output voltage

$$V_{OUT}(I_1, I_2, I_3, I_4, R_0) = R_0 \cdot \frac{12}{5} \left(I_4 + \frac{1}{4^1} I_3 + \frac{1}{4^2} I_2 + \frac{1}{4^3} I_1 \right)$$

- Simulation conditions
  - simulating ramp wave code input by switching current sources
  - $R_0 = 100\ \Omega$, $I = 6.40$ mA
- Design value : $V_{MAX} = 6.12$ V, $V_{\min} = 24.0$ mV



(a) Simulation result (b) Enlarged plot

6.Conclusion

- **Delivered the output voltage of R-r-R_T ladder circuit**
- **Proposed *N*-ary DAC configurations**
  - Ternary DAC
  - Quaternary DAC

<Future work>

- Usages of *N*-ary DACs
  - Middle bits of segmented DACs
  - For an internal circuit of pipelined ADCs / SAR ADCs

Reference

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