Analysis, Testing and Calibration of Charge Distribution SAR ADC Architecture with Split Capacitor

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Outline

- Research Background
- Split Capacitor Calculation
- Split Capacitor Parasitic Capacitance Problem
  - In case of parasitic capacitance in left side
  - In case of parasitic capacitance in right side
  - How to find parasitic capacitance value
- Capacitor Mismatch Effects to SAR ADC Non-Linearity
- Testing and Calibration
- Conclusion

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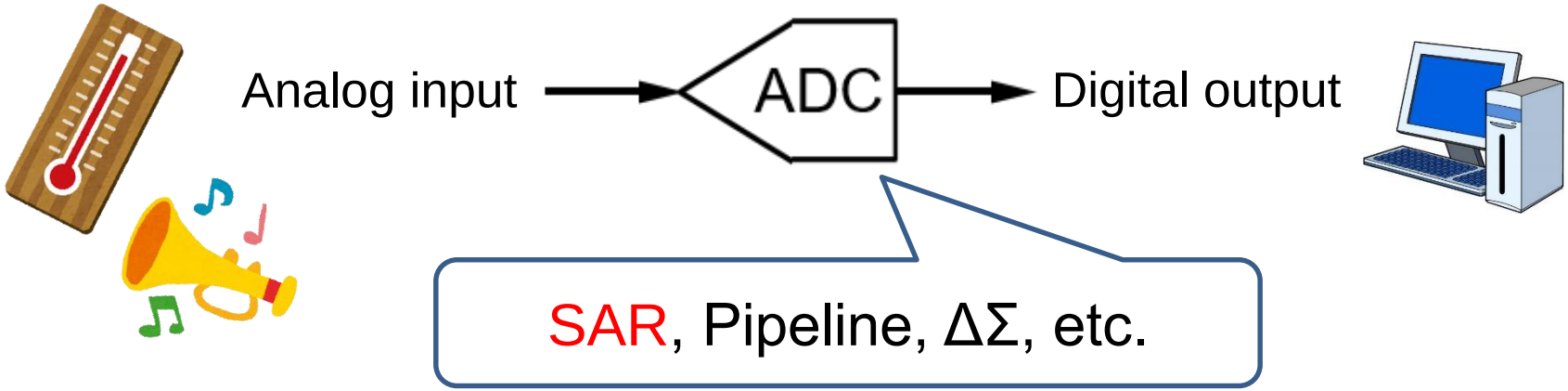
Research Background

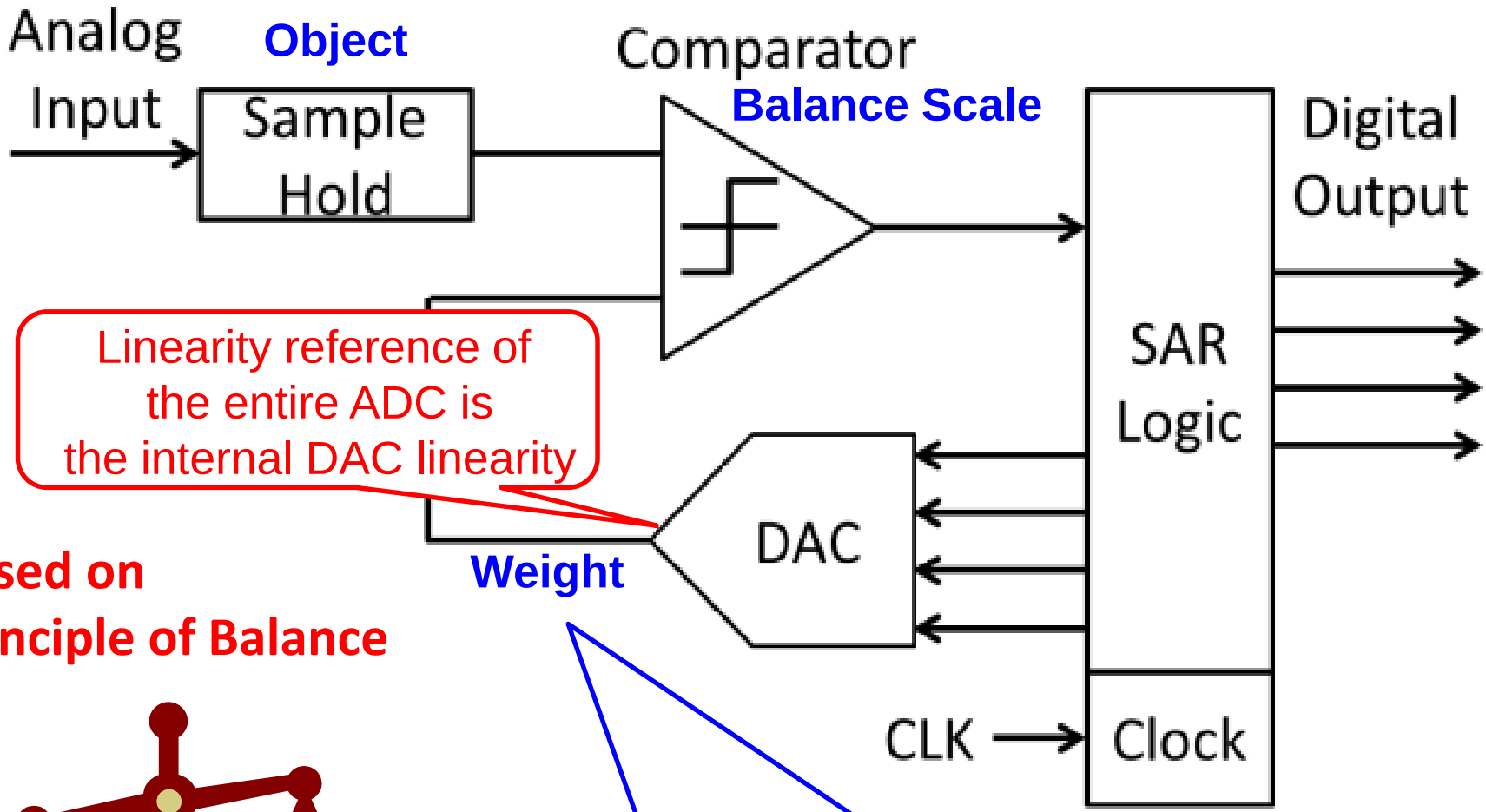
Natural signals are analog e.g. sound, light, temperature, pressure, etc.

Signals computer can handle are digital e.g. 0 or 1

Requires analog-to-digital converter (ADC)



SAR ADC Configuration



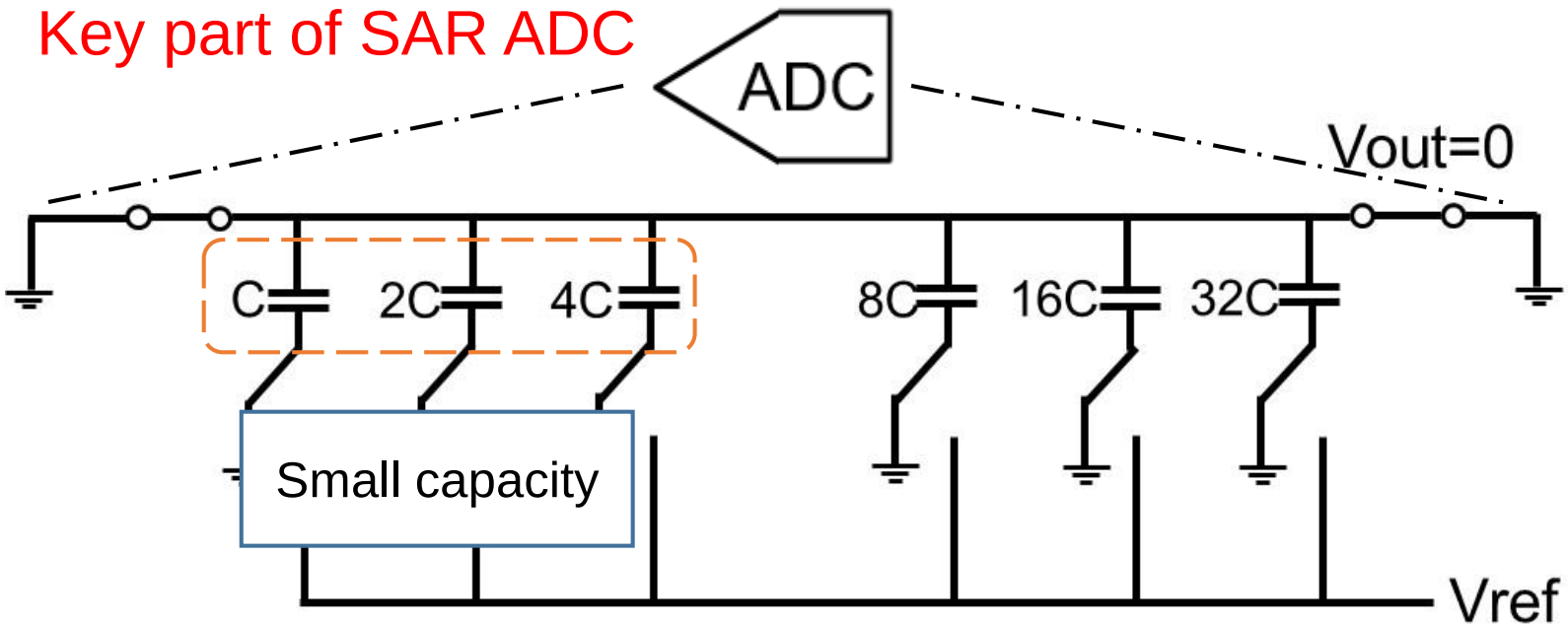
Linearity reference of the entire ADC is the internal DAC linearity

Based on Principle of Balance

Generally use binary weight
(1 , 2 , 4 , 8 , 16 , 32, 64 …)

Problem with Conventional SAR ADC

Key part of SAR ADC



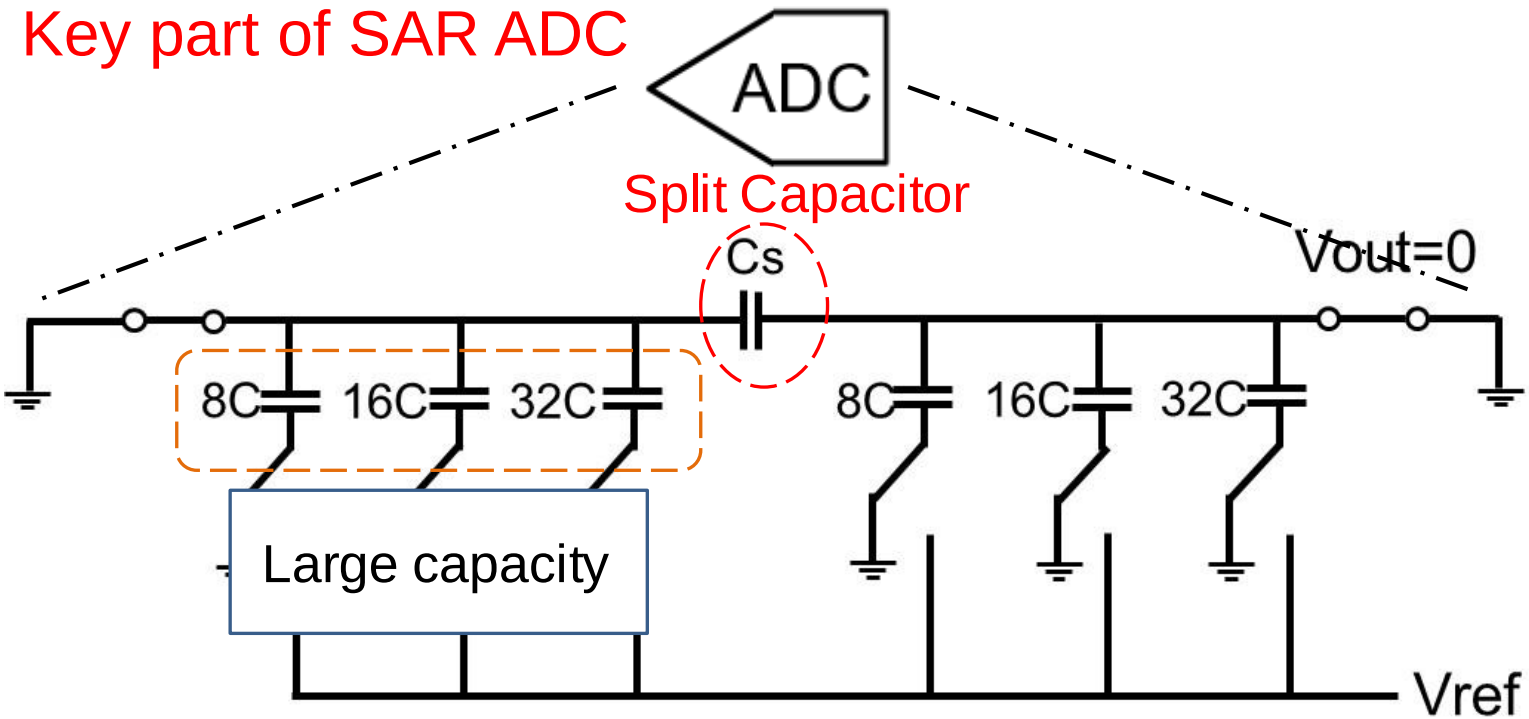
Achieves high accuracy with
a minute capacitance

Capacitance ratio with other capacitances in t circuit → Large
e.g. C≪32C

Difficult to manufacture!

SAR ADC：
Successive-Approximation-Register
Analog-to-Digital Converter

Improvement using Split Capacitor



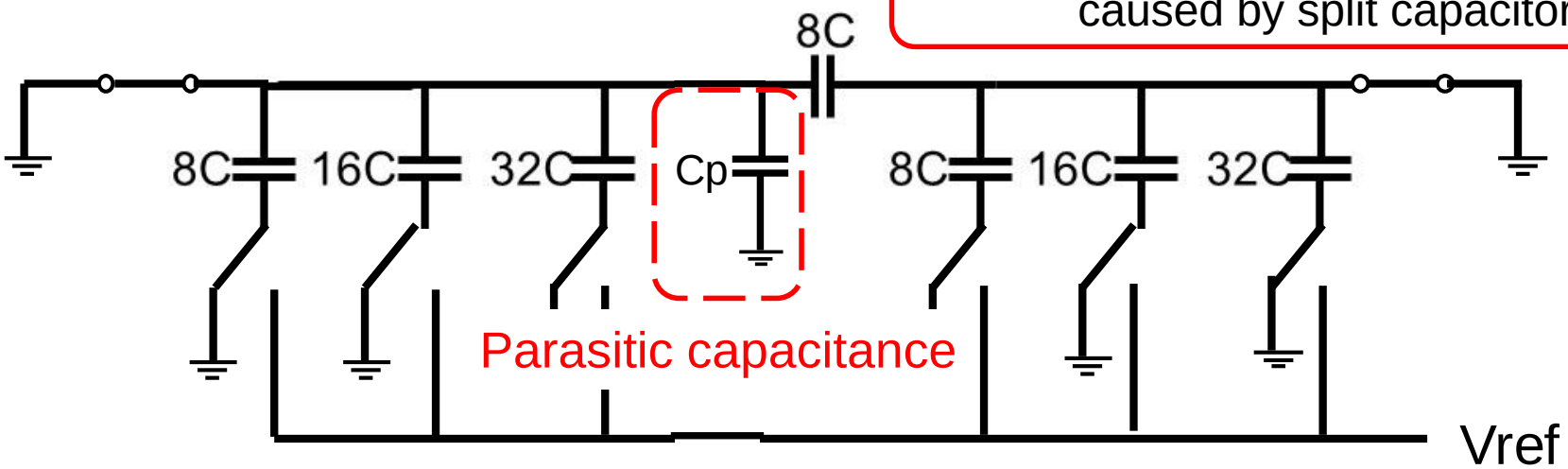
Reduce capacitance ratio

Obtain high-precision output without using a minute capacitance

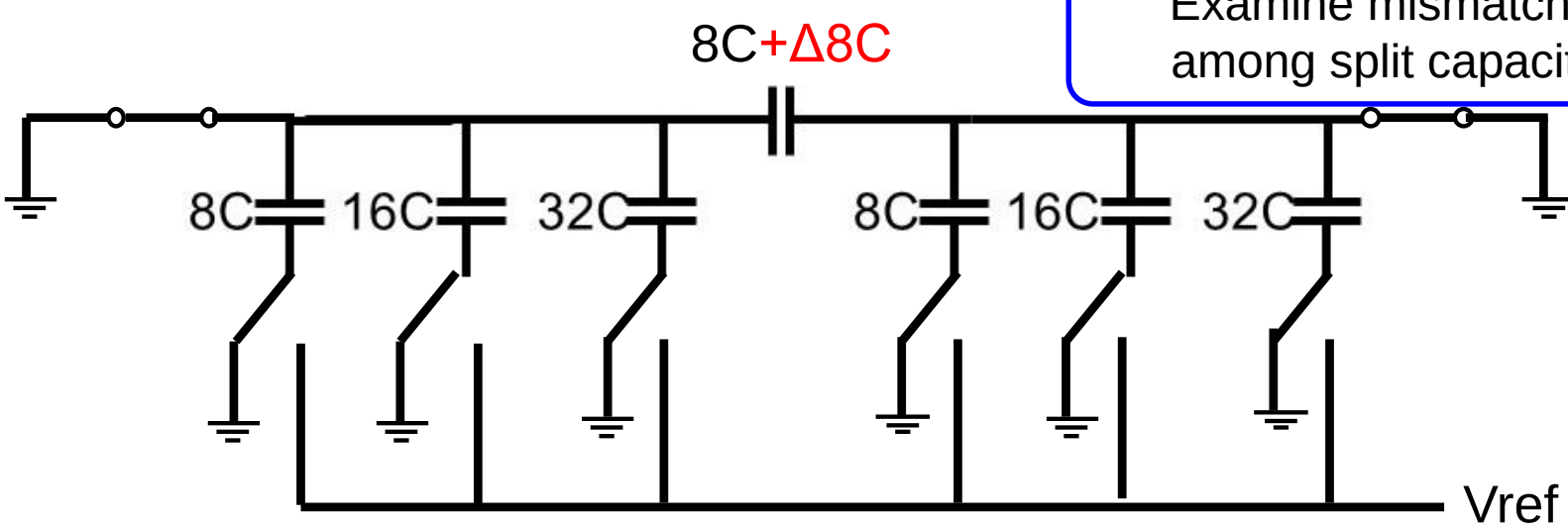
Using Split Capacitor

Research Goal

Examine parasitic capacitance effect caused by split capacitor



Examine mismatches among split capacitor



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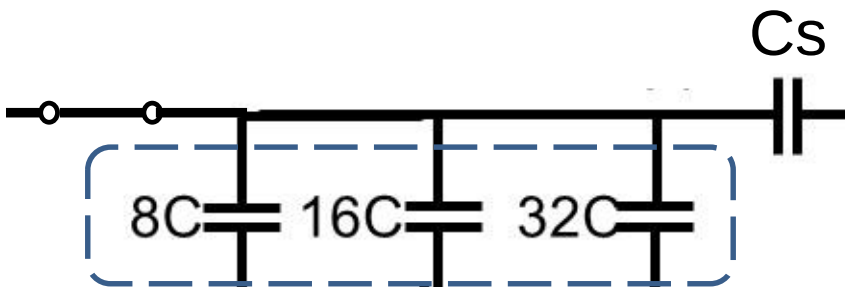
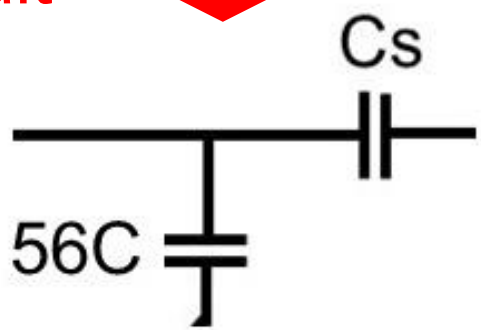
Combined Capacitance



Parallel ➡ 8C+16C+32C=56C

Equivalent circuit



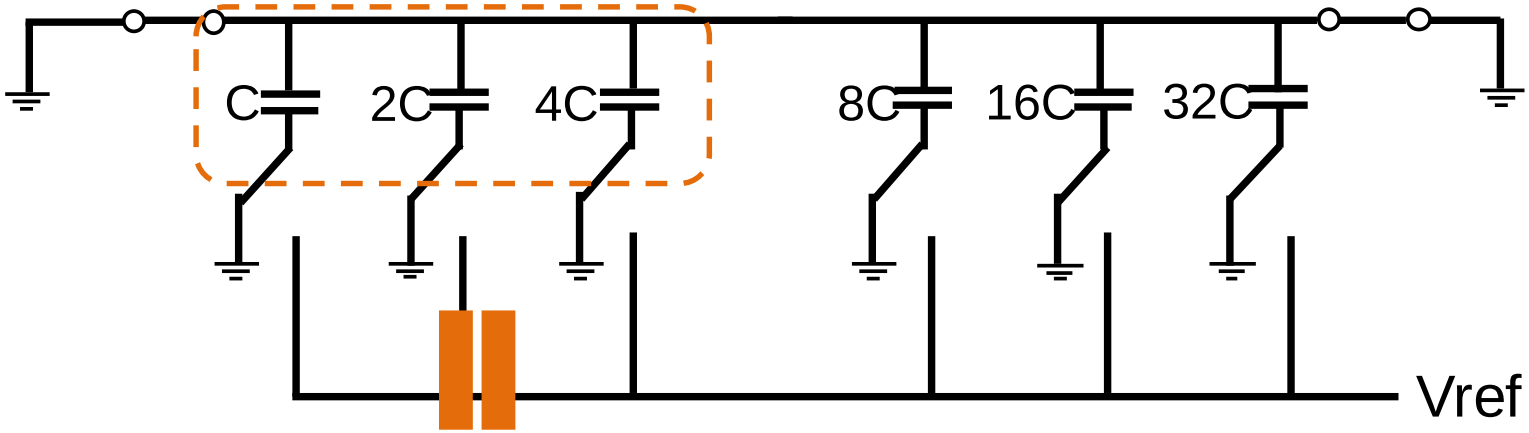
Combined capacitance

Series ➡

$$\frac{1}{\frac{1}{56C}+\frac{1}{C_s}}=\boxed{\frac{56CC_S}{56C+C_S}}$$

Split Capacitor Calculation

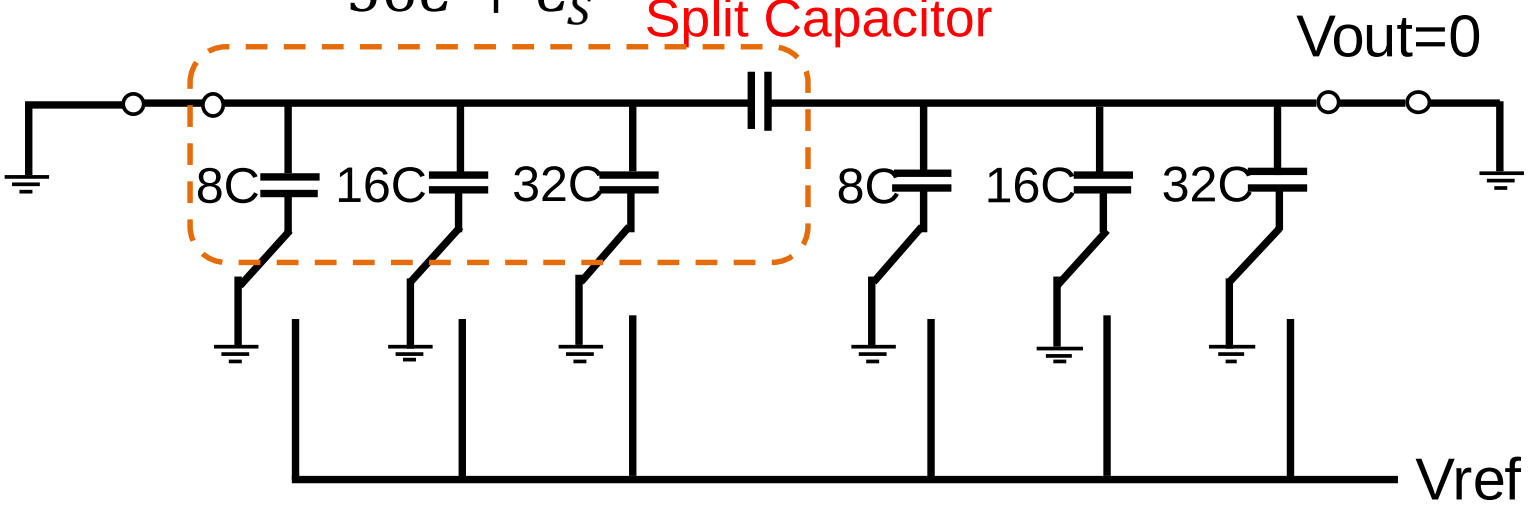
C+2C+4C=7C



$$\frac{56CC_S}{56C + C_S}$$

Split Capacitor

Cs=8C



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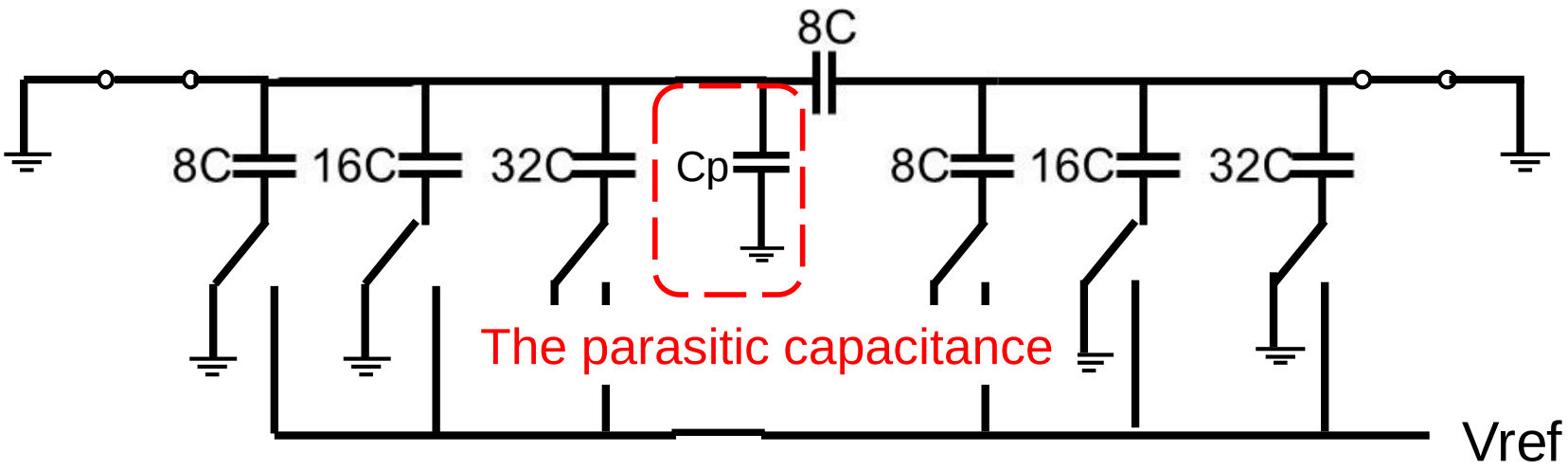
Parasitic Capacitance Problem



Advantage — Alleviate problem of capacitance ratio

Disadvantage — Affect overall ADC linearity

Derivation of general formula
Obtain parasitic capacitance value

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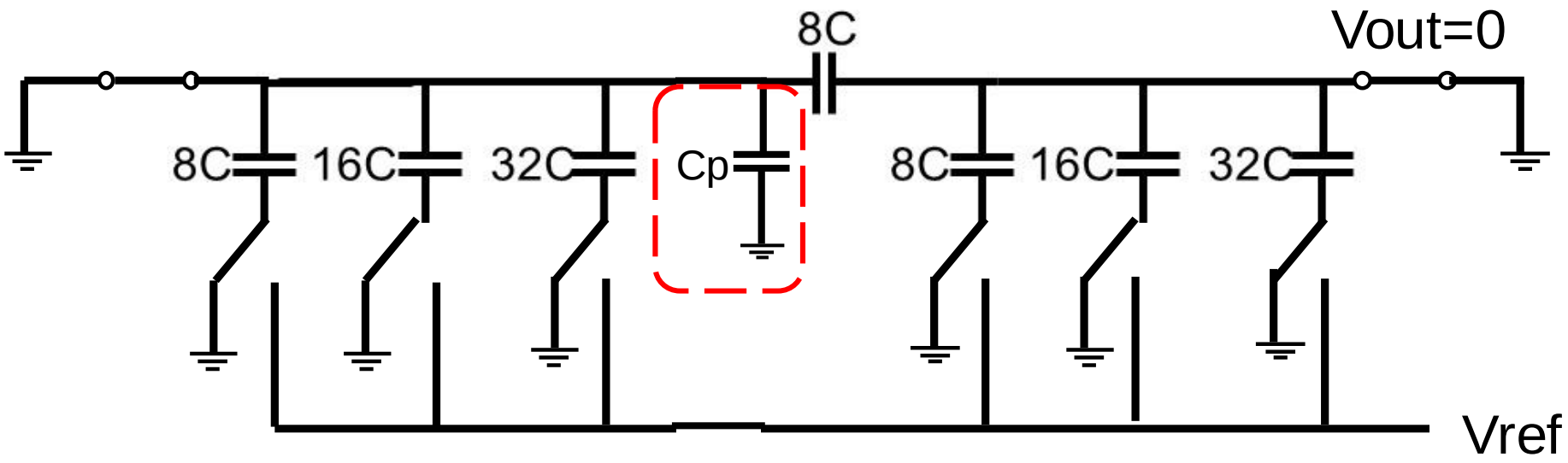
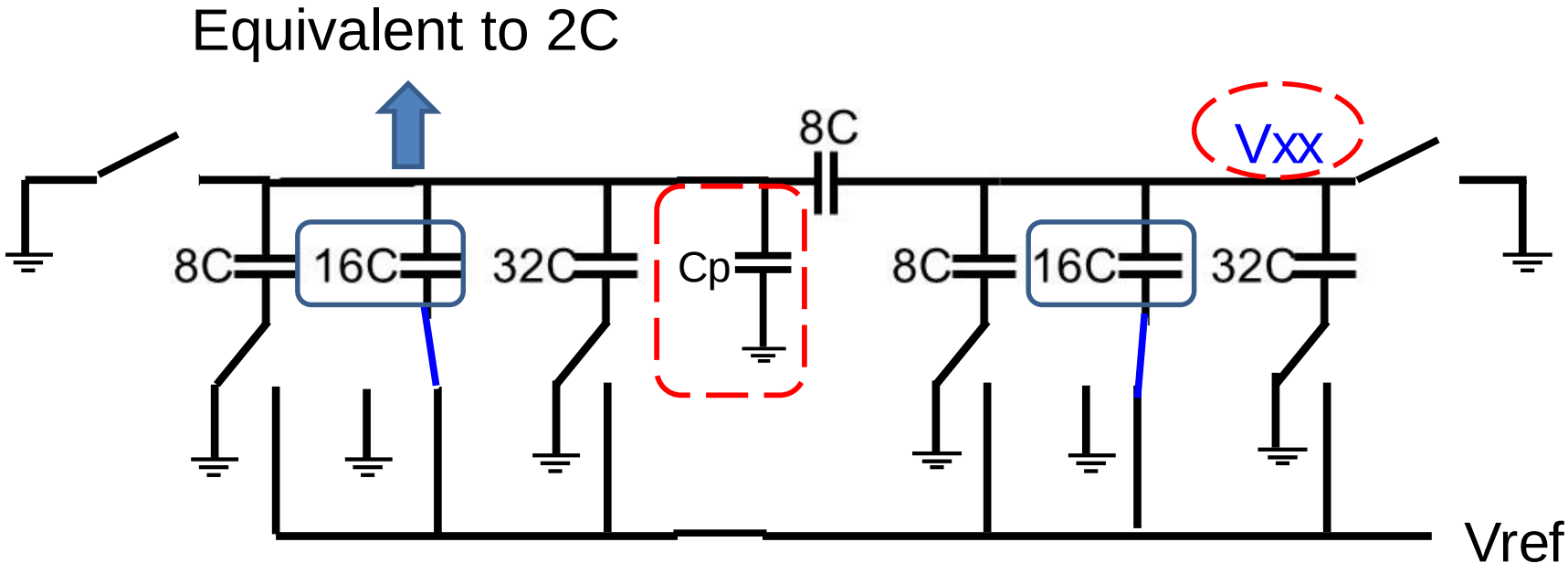
Initialization

Set charge amount to each capacitance to 0

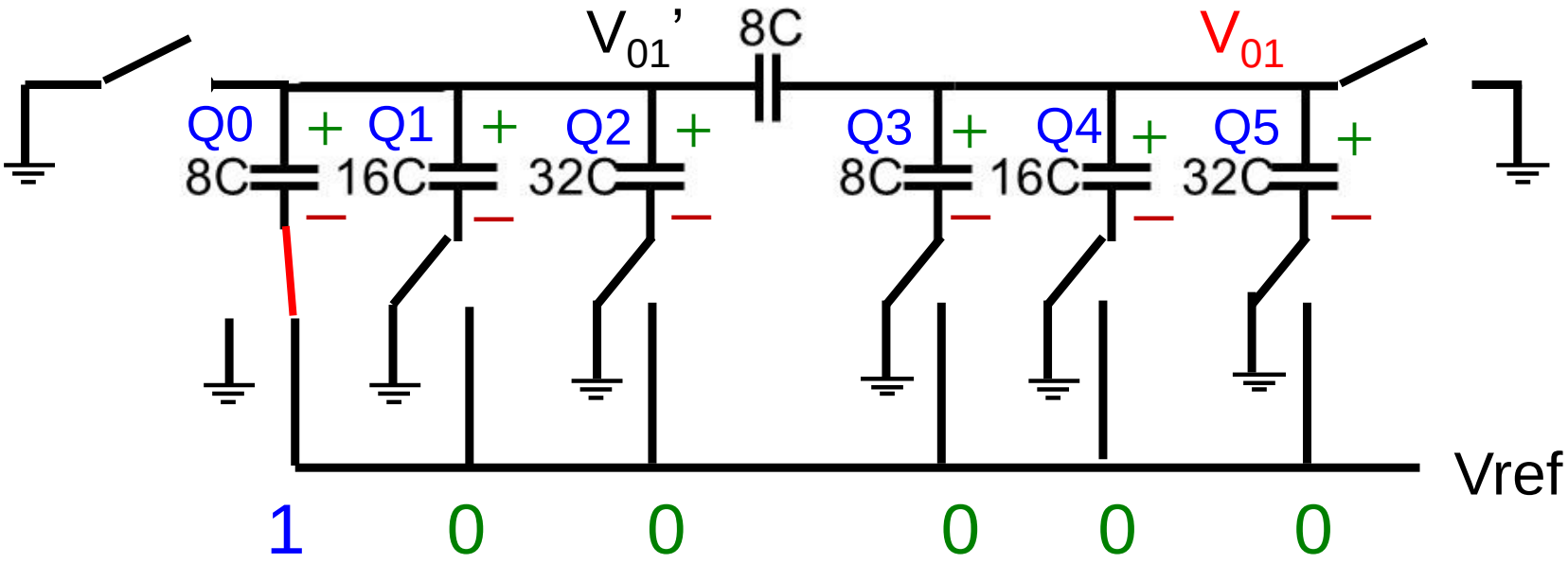


Calculation of Vxx

2C+16C=18C ➡ Vxx → V18



Calculation of $V_{01}(1)$

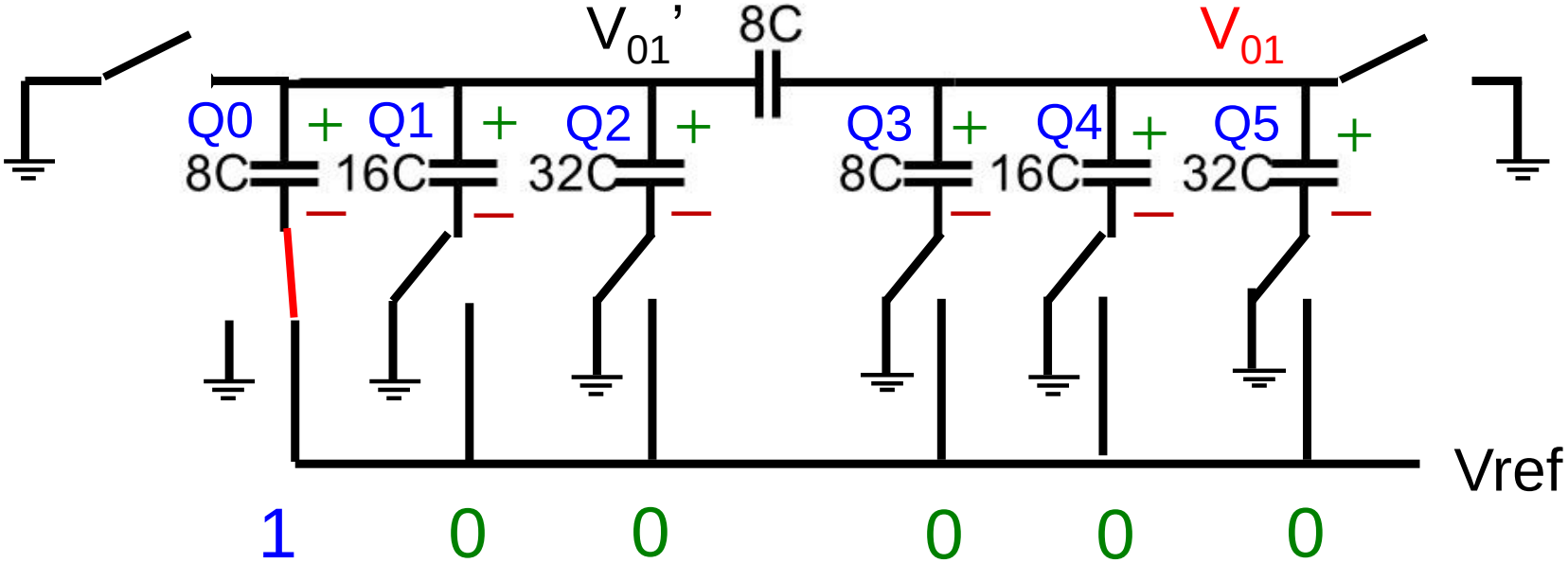


Law of conservation of electric charges

$$Q0+Q1+Q2=Qs$$

$$Qs+Q3+Q4+Q5=0$$

Calculation of $V_{01}(2)$



Q0+Q1+Q2=Qs
Qs+Q3+Q4+Q5=0

Q0=8C(V01'-Vref)
Q1=16CV01'
Q2=32CV01'
Q3=8CV01
Q4=16CV01
Q5=32CV01

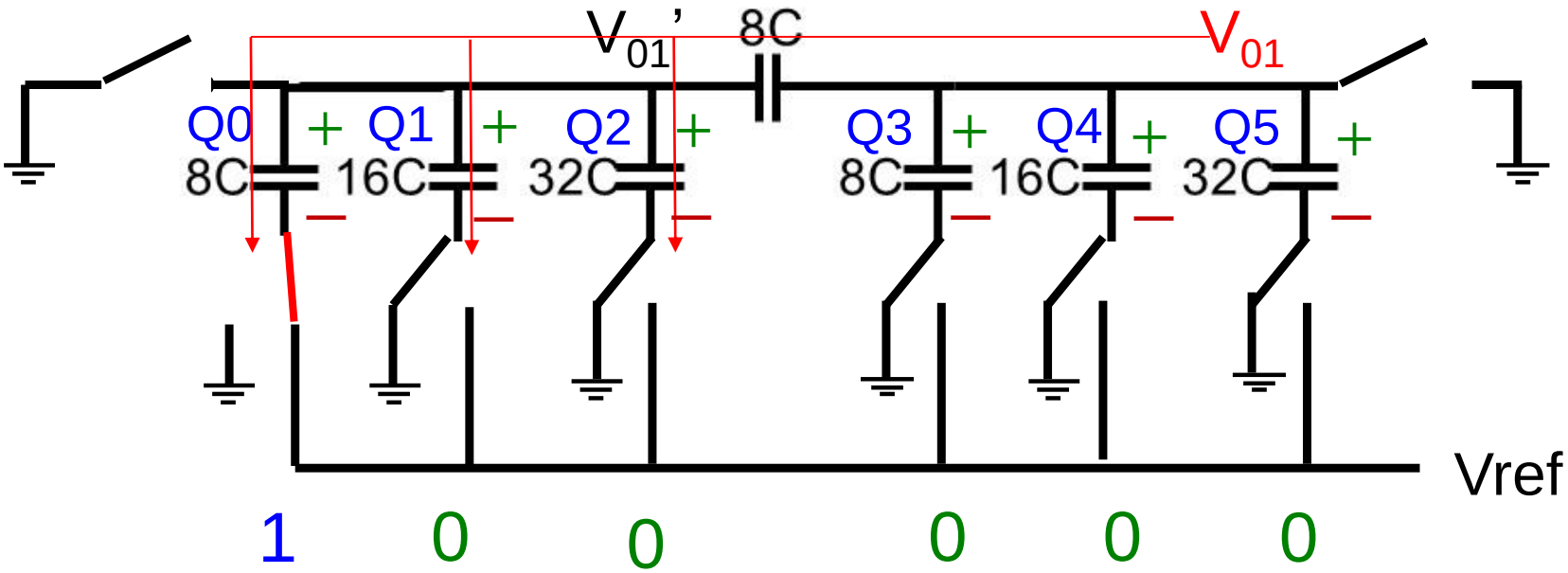
8C(V01'-Vref)+16CV01'+32CV01'+8CV01+16CV01+32CV01=0

56CV01=8CVref – 56CV01'

V01=(8/56)Vref –V01'

?

Calculation of V_{01}'



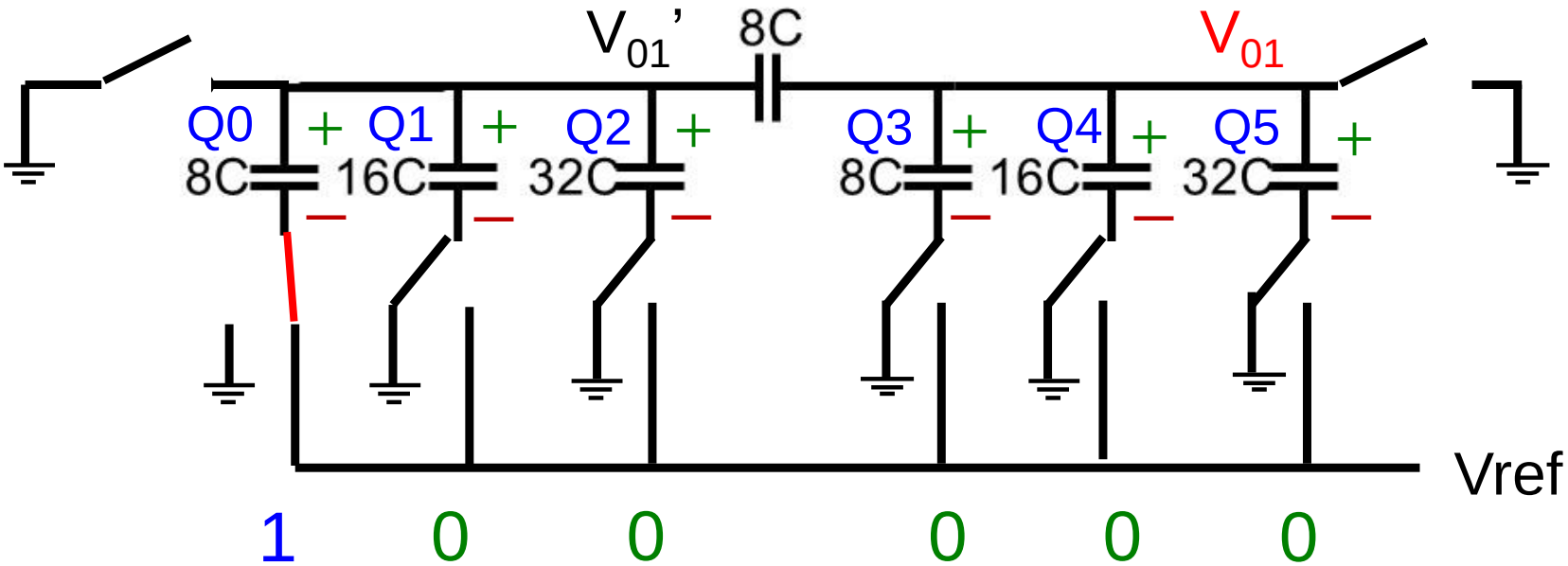
Charge of split capacitor → Sum of charges of 8C, 16C, 32C

8C(V01-V01')=8C(V01'-Vref)+16CV01'+32CV01'

64CV01'=8CVref+8CV01

$$\therefore \mathrm{V01}' = \frac{8\mathrm{Vref} + 8\mathrm{V01}}{64}$$

Calculation of V_{01}(3)



V01=(8/56)Vref – V01'

$$V01 = \frac{8Vref}{56} - \frac{8Vref + 8V01}{64}$$

Substitute

$$V01' = \frac{8Vref + 8V01}{64}$$

$$V01 = \frac{1}{63} Vref$$

Vxx formula(no parasitic capacitance)

$$V01 = \frac{1}{63}Vref$$

$$V02 = \frac{2}{63}Vref$$

$$\cdots$$

$$V05 = \frac{5}{63}Vref$$

$$\cdots$$

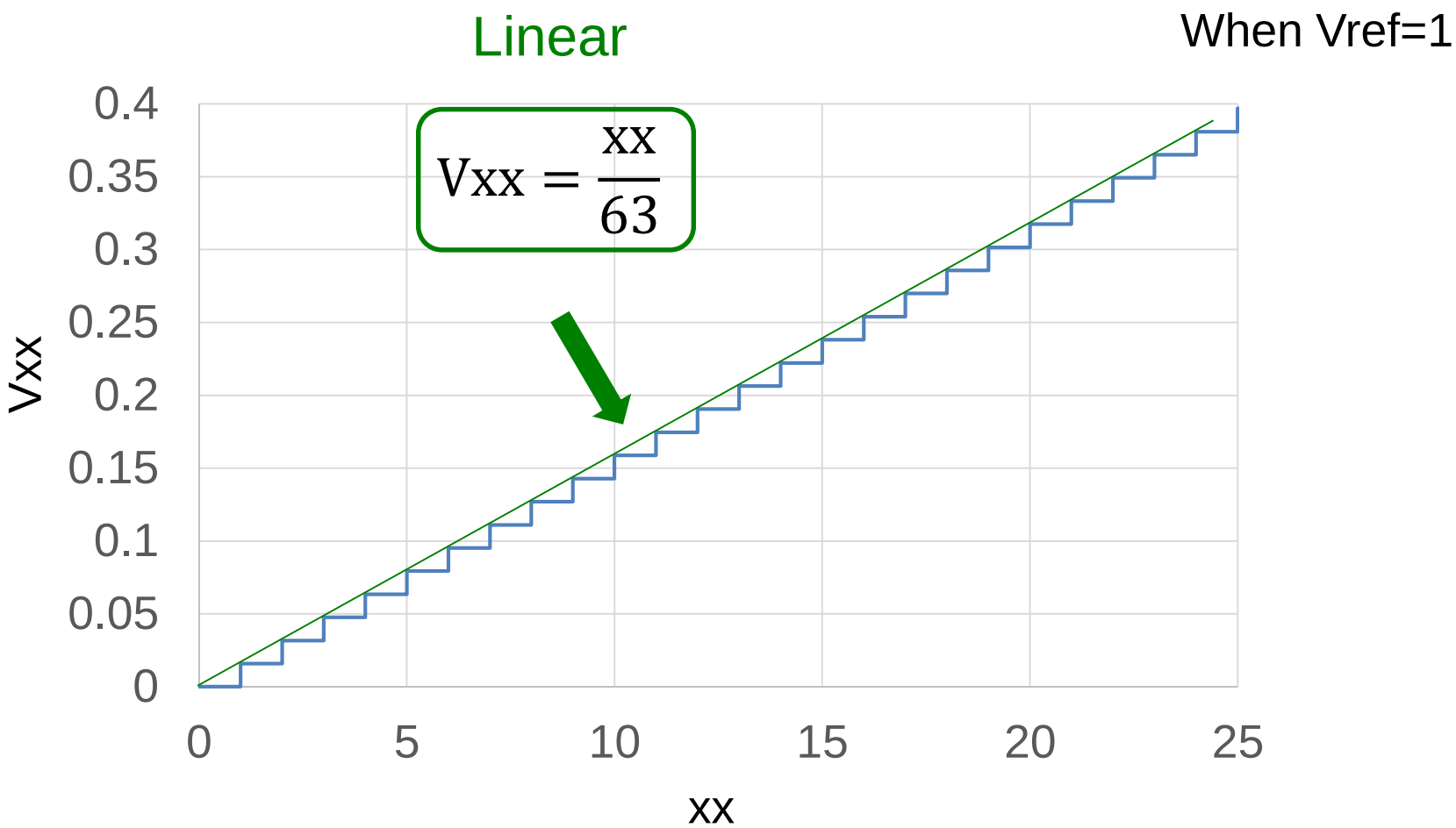
$$V29 = \frac{29}{63}Vref$$

$$\boxed{Vxx = \frac{xx}{63}Vref}$$

Vxx is proportional to xx

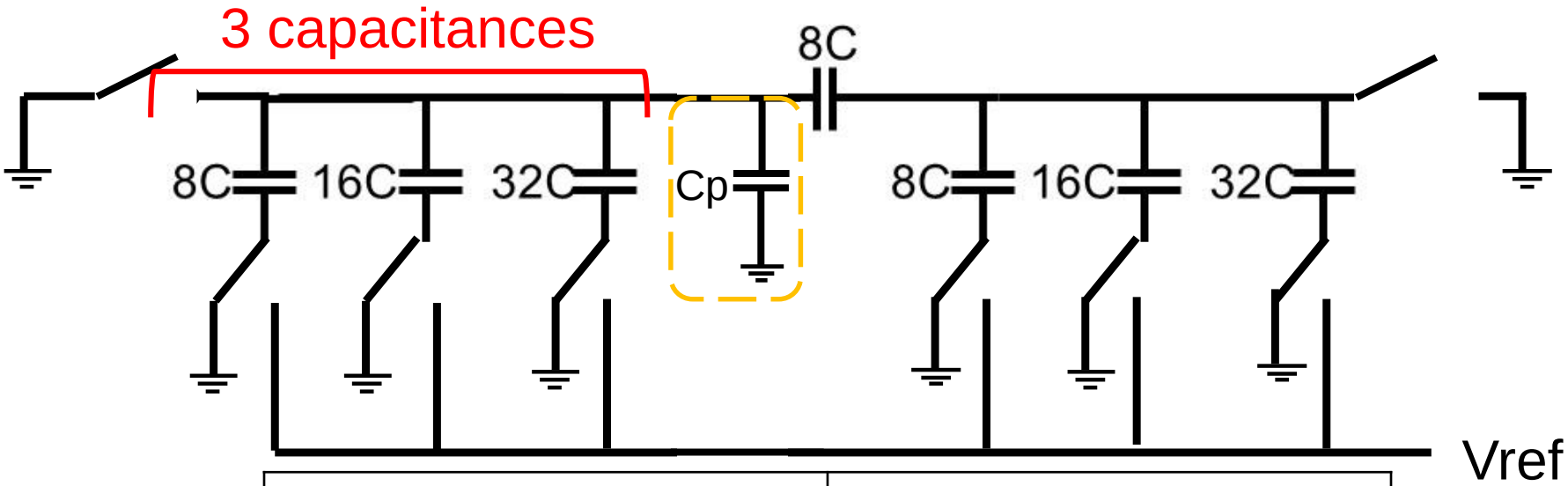
Linear

Graph without Parasitic Capacitance



No parasitic capacitance ➡ Linear characteristics

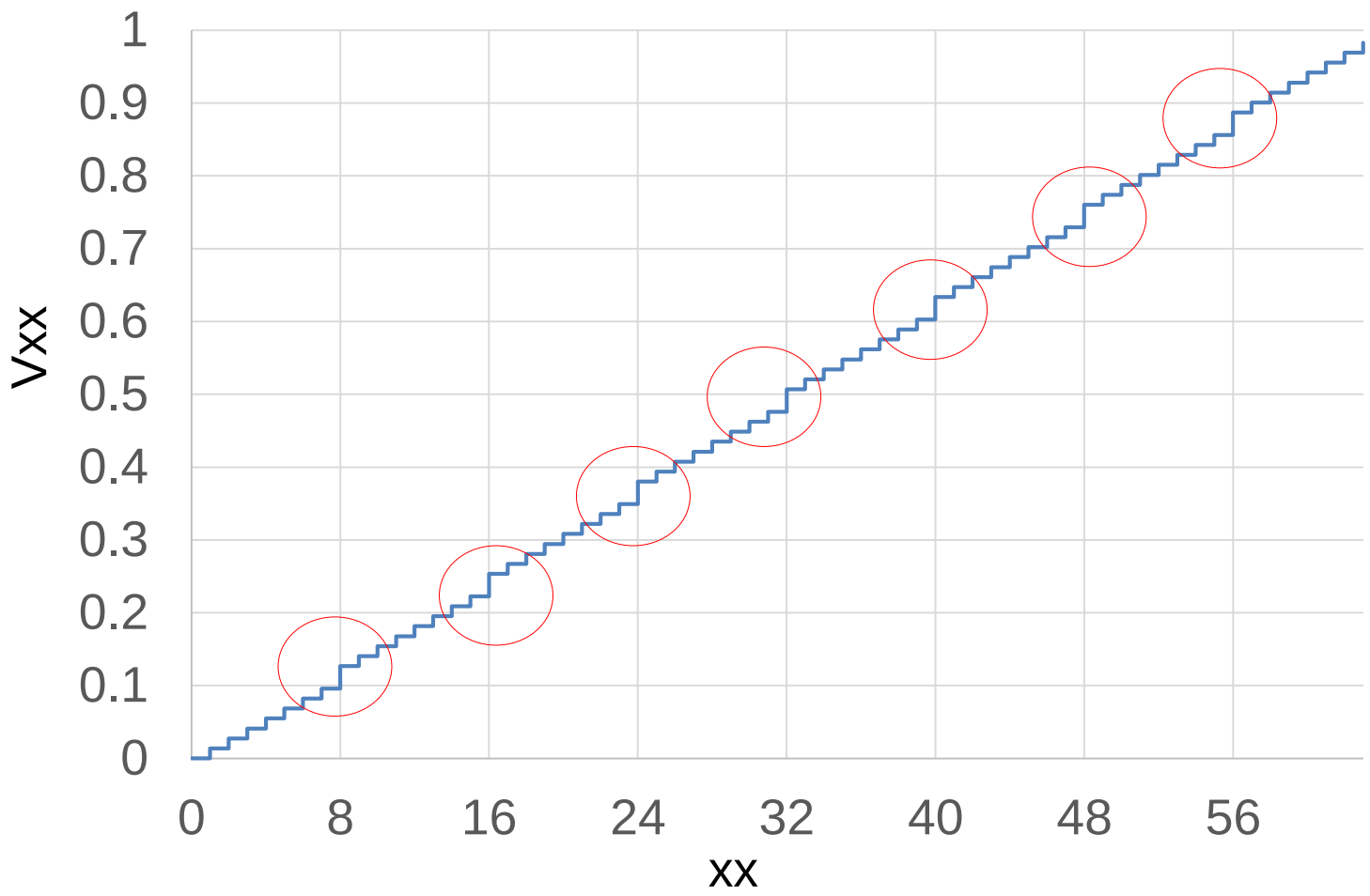
3 Capacitances to Left



xx=00～xx=07	$\mathrm{Vxx} = \frac{8\mathrm{xx}}{63 \times 8 + 8\alpha}\mathrm{Vref}$
xx=08～xx=15	$\mathrm{Vxx} = \frac{8\mathrm{xx} + \alpha}{63 \times 8 + 8\alpha}\mathrm{Vref}$
xx=16～xx=23	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 2\alpha}{63 \times 8 + 8\alpha}\mathrm{Vref}$
xx=24～xx=31	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 3\alpha}{63 \times 8 + 8\alpha}\mathrm{Vref}$

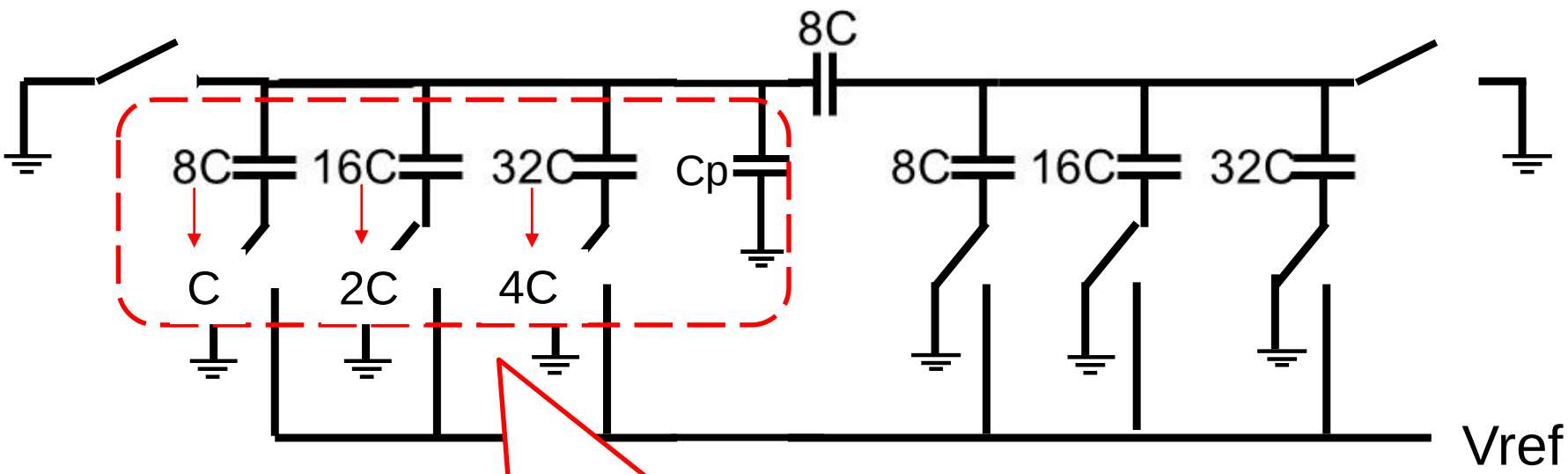
α=Cp/C

Effect of Parasitic Capacitance



Linearity breaks in multiples of 8

Consideration



7 is MAX on the left side
of Split Capacitor

The effect appears every 8

General Formula

$$Vxx = \frac{(\text{Split Capacitor}/C) \times xx + B\alpha}{63 \times (\text{Split Capacitor}/C) + A\alpha} Vref$$

Sum of total capacitors
(1+2+4+8+16+32)

A, B depend on split capacitor position

	Left capacity number 3 Split Capacitor=8C	Left capacity number 2 Split Capacitor=4C	Left capacity number 4 Split Capacitor=20C
A	8	16	17
B	Increase by 1	Increase by 1	Increase by 4

General Formula Summary

$$Vxx = \frac{(\text{Split Capacitor}/C) \times xx + B\alpha}{\boxed{63} \times (\text{Split Capacitor}/C) + A\alpha} Vref$$

Sum of total capacitors
(1+2+4+8+16+32)

$$A = \frac{\text{Sum of capacity on right side of Split Capacitor}}{\text{Minimum capacity}} + \frac{\text{Value of Split Capacitor}}{\text{Minimum capacity}}$$

$$B = \frac{\text{Capacitor weight to right of Split Capacitor}}{\text{Minimum capacity}}$$

If the shape of the circuit is known,
the general formula can be derived

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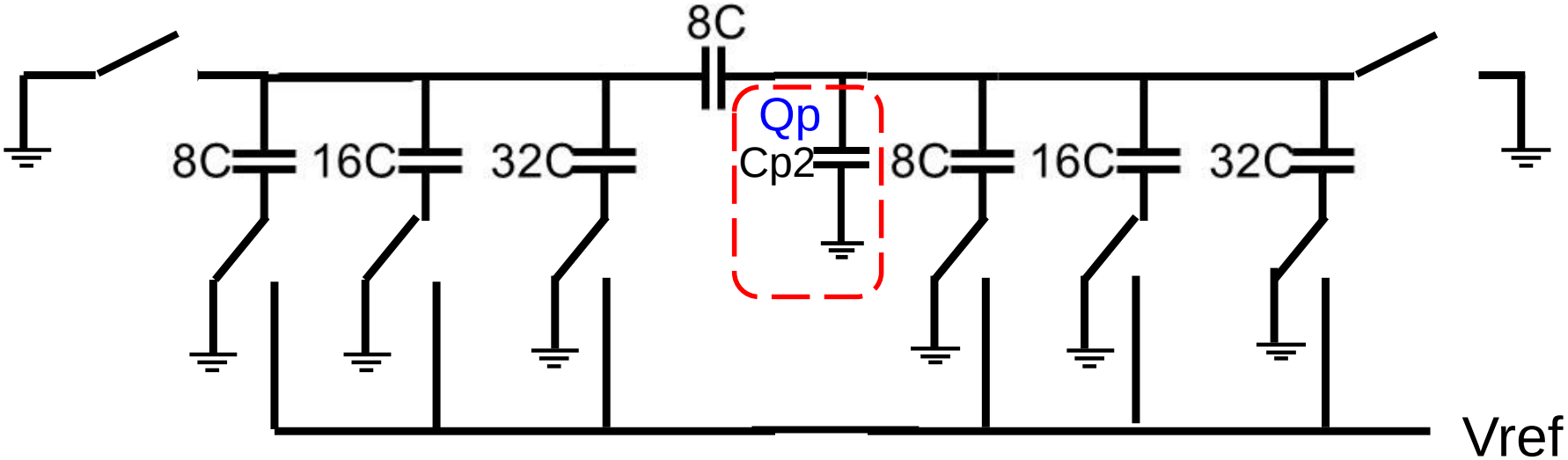
3 Capacitances to Right



$$\boxed{Vxx = \frac{xx}{63 + \beta} Vref}$$

β=Cp2/C
Cp2=βC

Parasitic capacitance : Right side of split capacitor
Vxx is proportional to xx and no non-linearity appears

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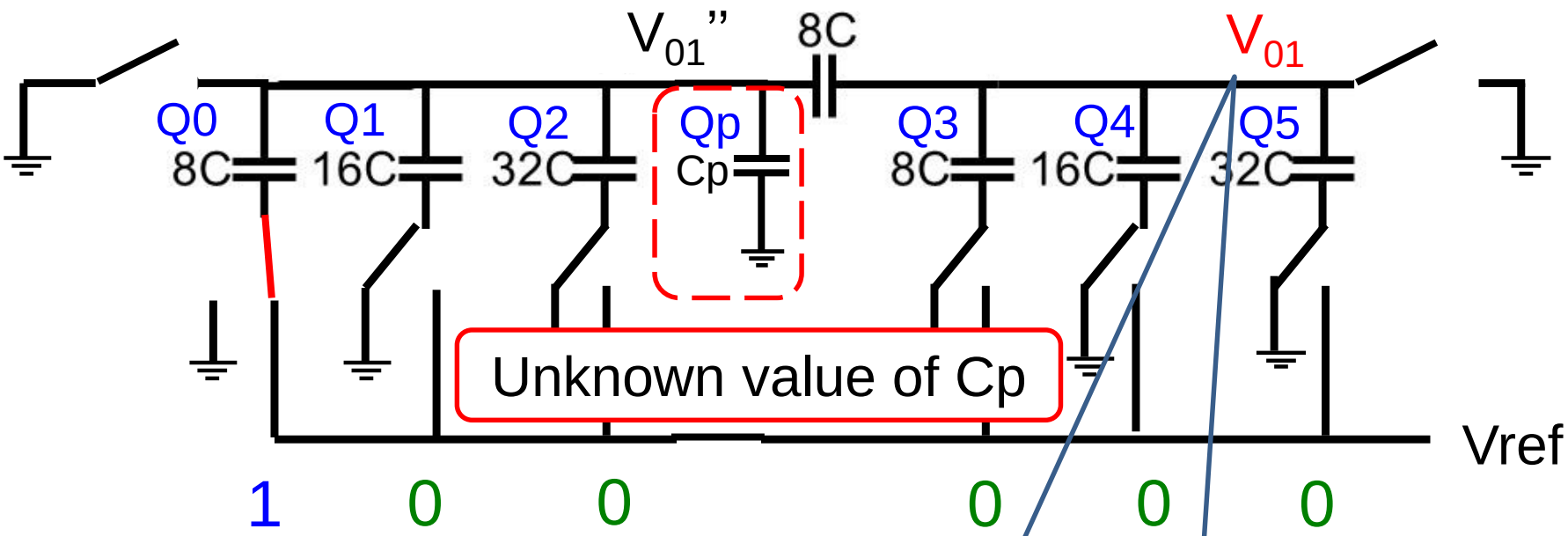
Measurement of V01

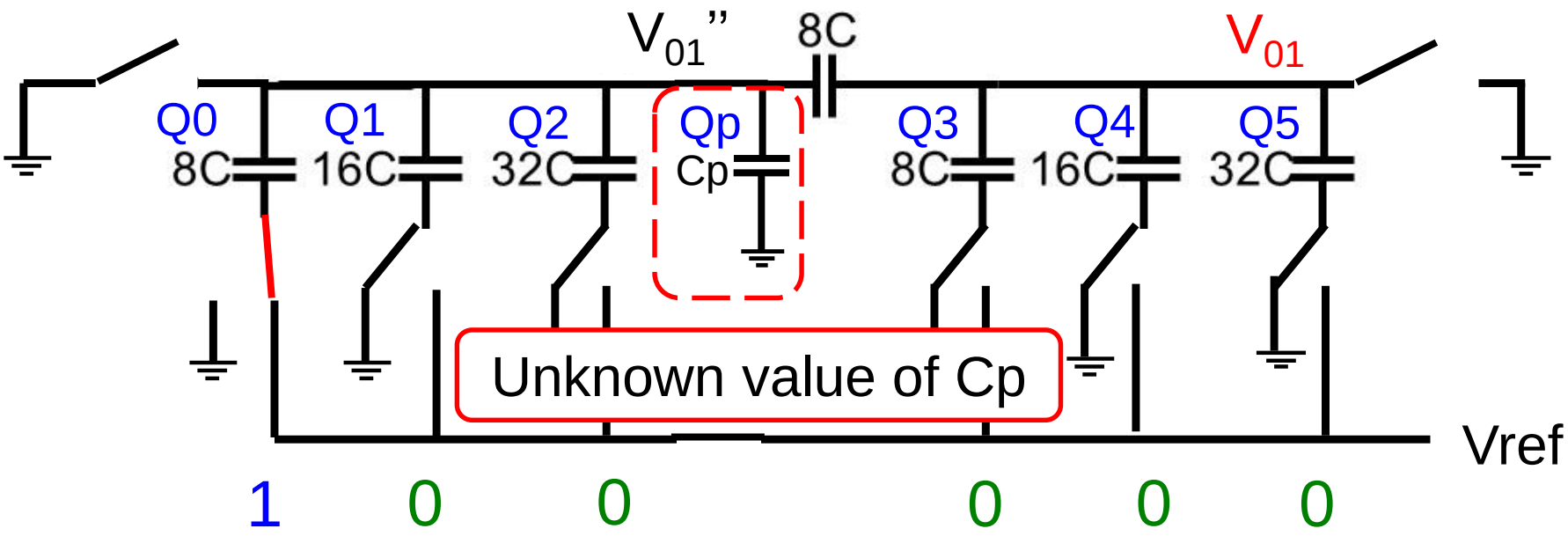


Connect only
the least significant bit to Vref
Vxx at this time is V01

With internal or external ADC
Measure V01

Suppose
V01 = 0.0136986V

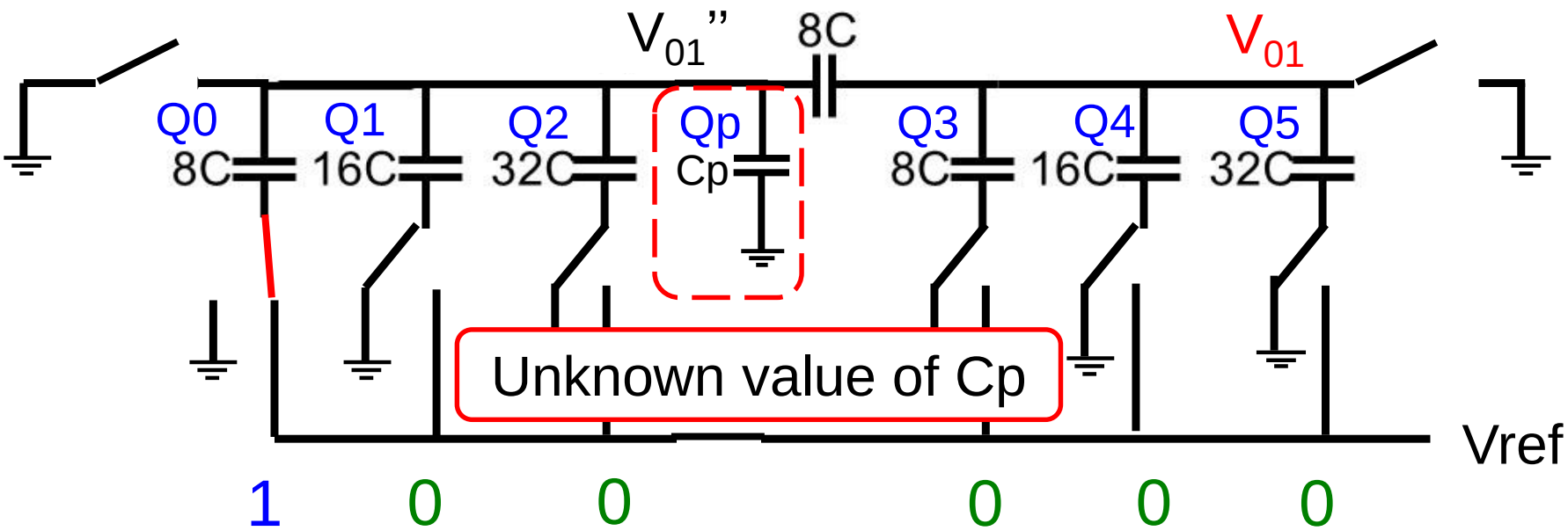
Preparation of General Formula (1)



$$A = \frac{\text{Sum of capacity on the right side of Split Capacitor}}{\text{Minimum capacity}} + \frac{\text{Value of Split Capacitor}}{\text{Minimum capacity}}$$

$$= \frac{56}{8} + \frac{8}{8} = 8$$

Preparation of General Formula (2)

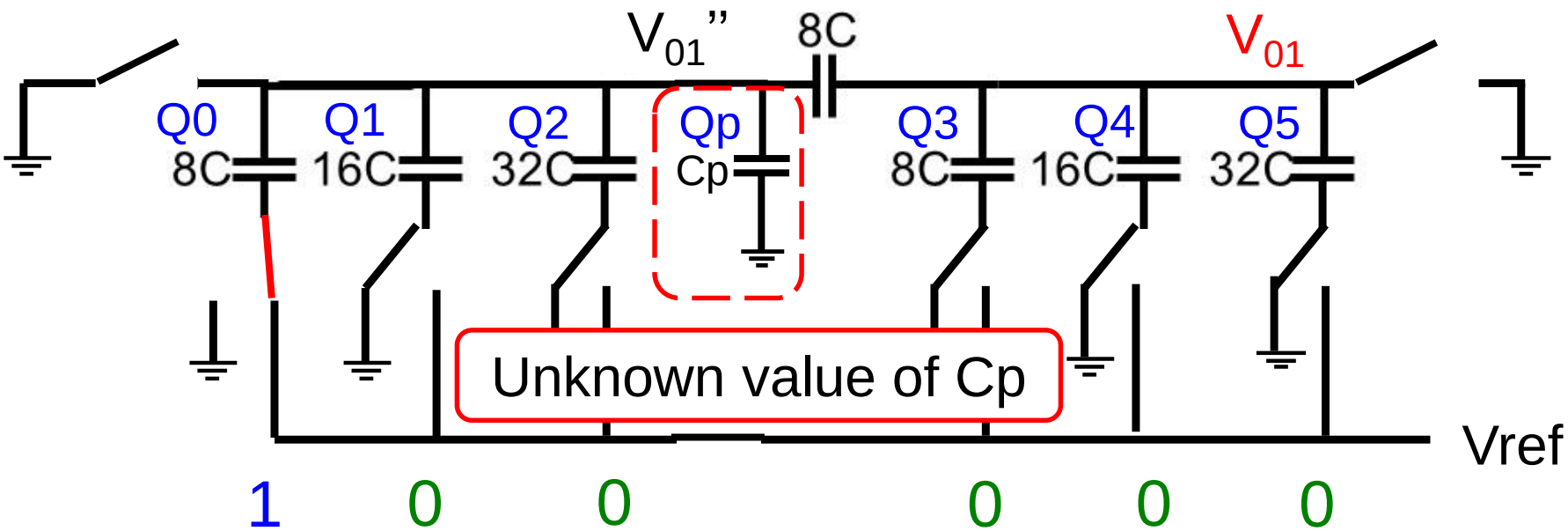


$$Vxx = \frac{(\text{Split Capacitor}/C) \times xx + B\alpha}{63 \times (\text{Split Capacitor}/C) + A\alpha} Vref$$

A=8

$$Vxx = \frac{8xx}{63 \times 8 + 8\alpha} Vref$$

Substitute in General Formula



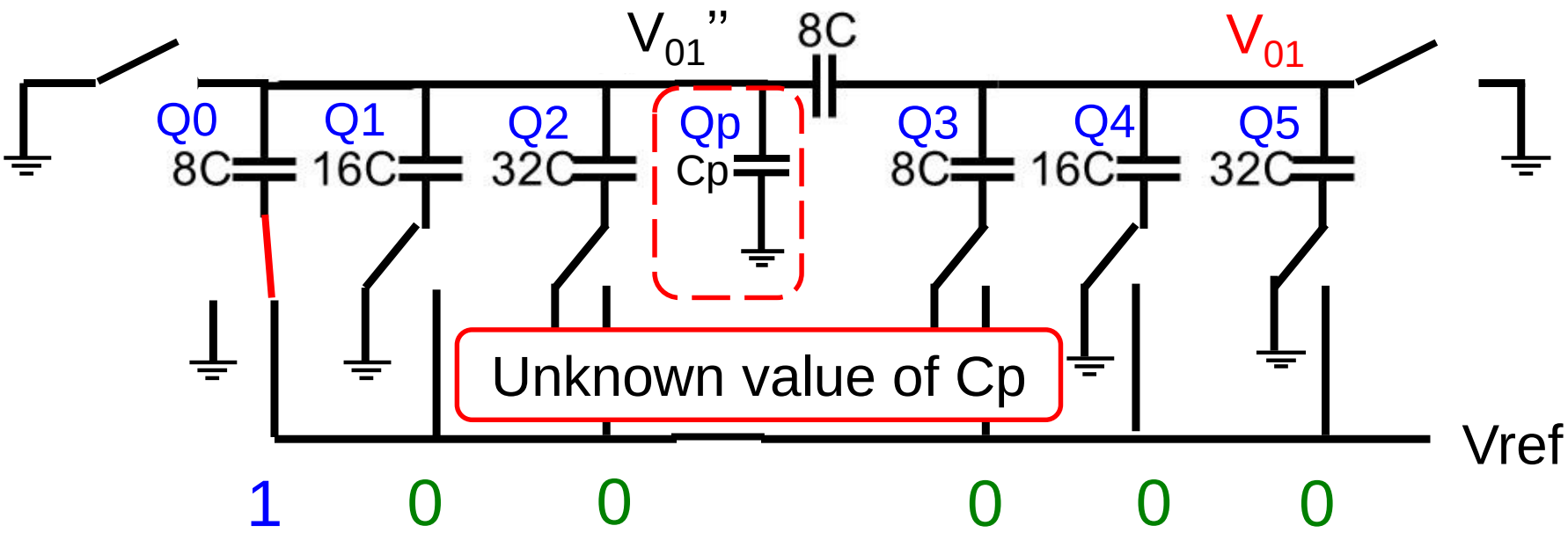
$$Vxx = \frac{8xx}{63 \times 8 + 8\alpha} Vref$$

Substitute xx=01, Vxx=0.0136986V

$$0.0136986 = \frac{8 \times 1}{63 \times 8 + 8\alpha} \times 1$$

Set Vref=1

Solve α



$$0.0136986 = \frac{1}{63 + \alpha}$$

$$0.8630118 + 0.0136986\alpha = 1$$
$$0.0136986\alpha = 0.1369882$$

$\therefore \alpha = 10.0001606$

Divide by C
Parasitic capacitance can be found

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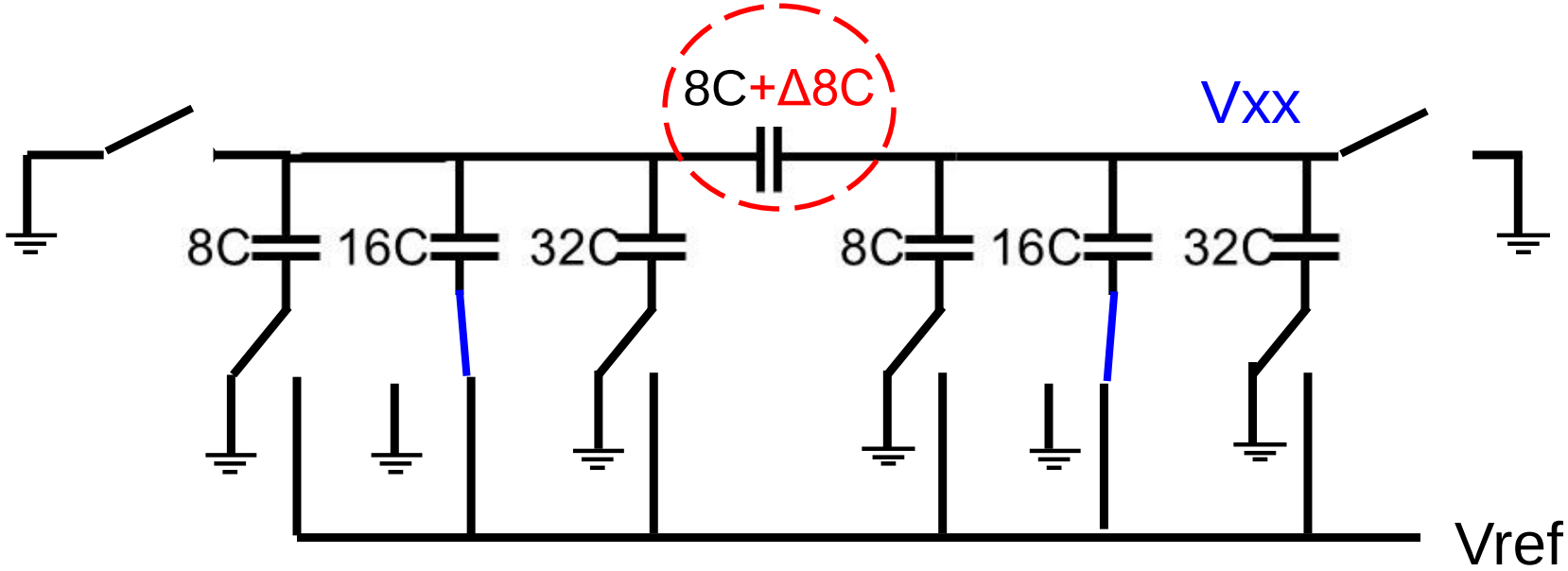
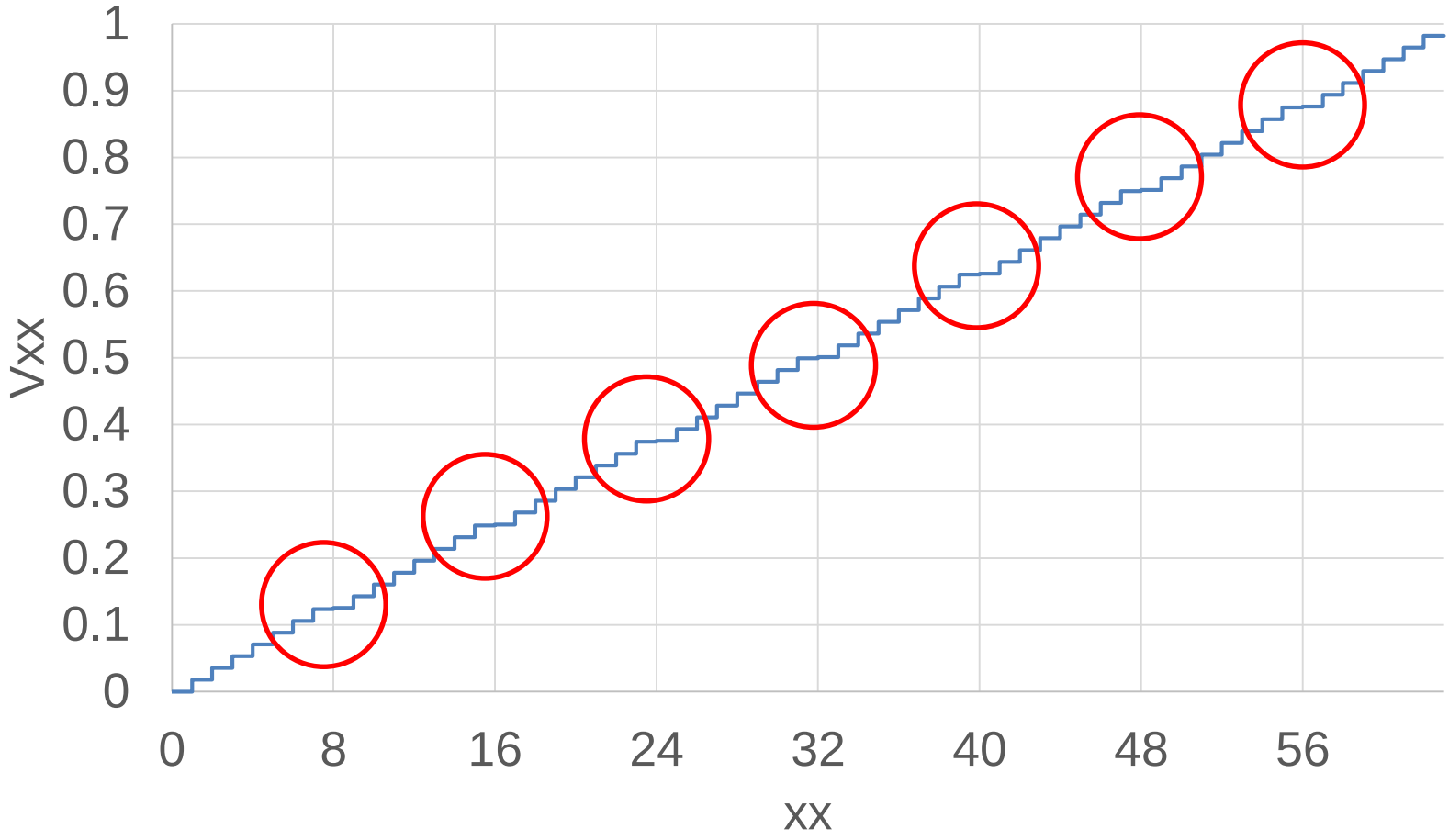
Split Capacitor Mismatch Effects

Examination in case of mismatch in split capacitor



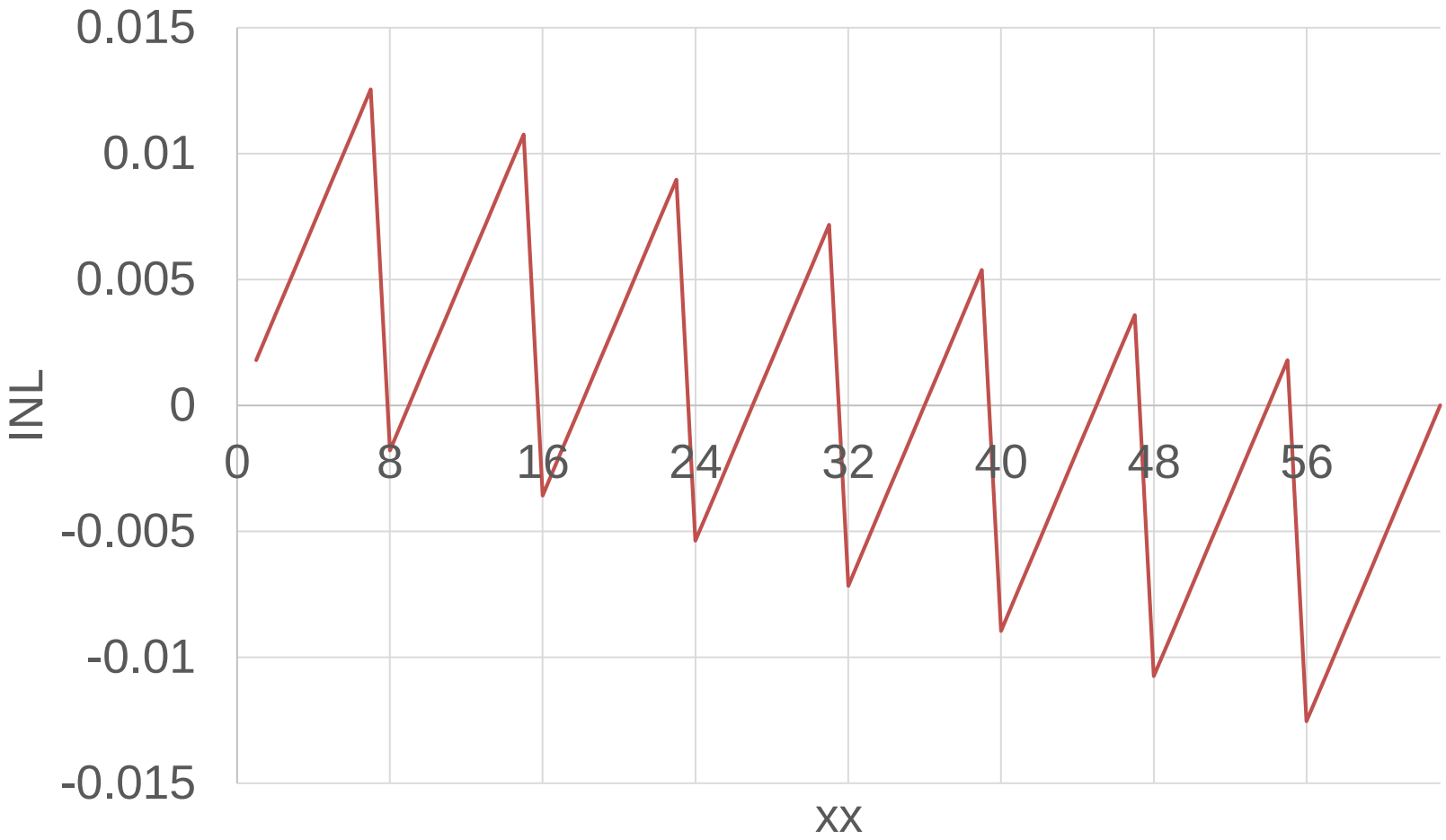
Graph of Vxx



Mismatch of split capacitor is 15%

Non-linearity at multiples of 8

Graph of INL



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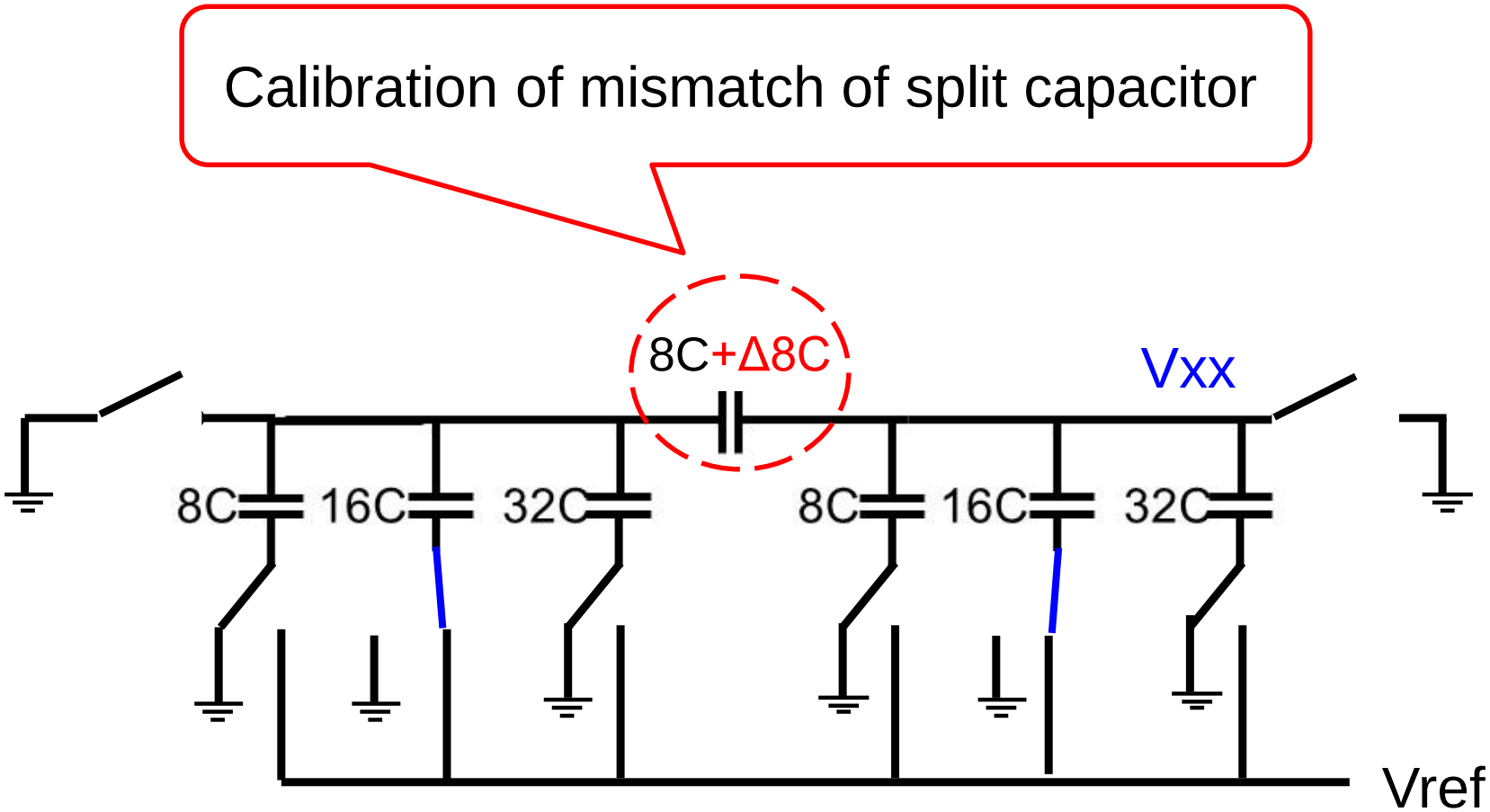
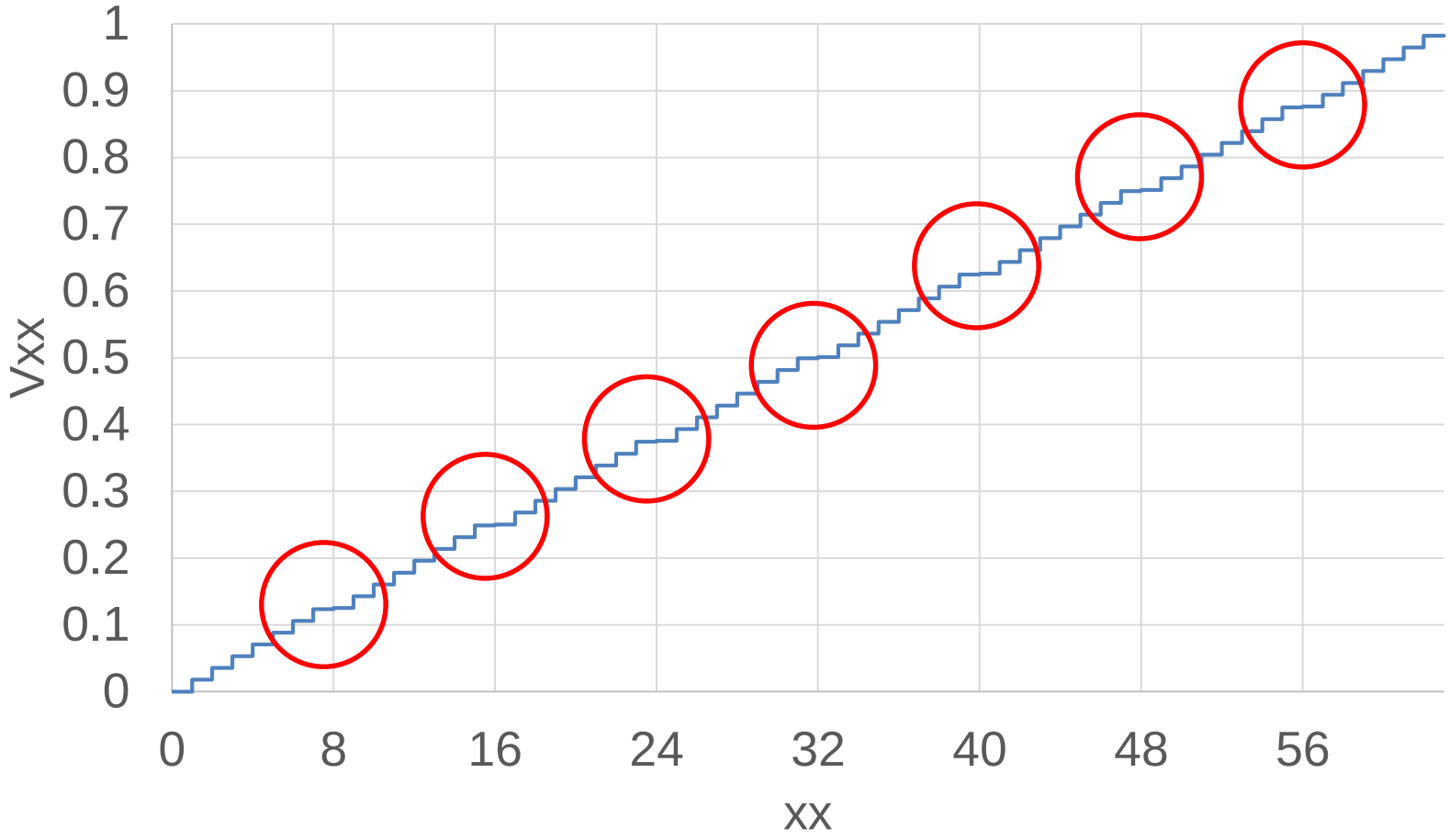
Calibration of Mismatch Effect



- Measure the error at mass production test stage and store its data in Flash memory.
- Then at normal operation stage, use it for correction.

Before Correction

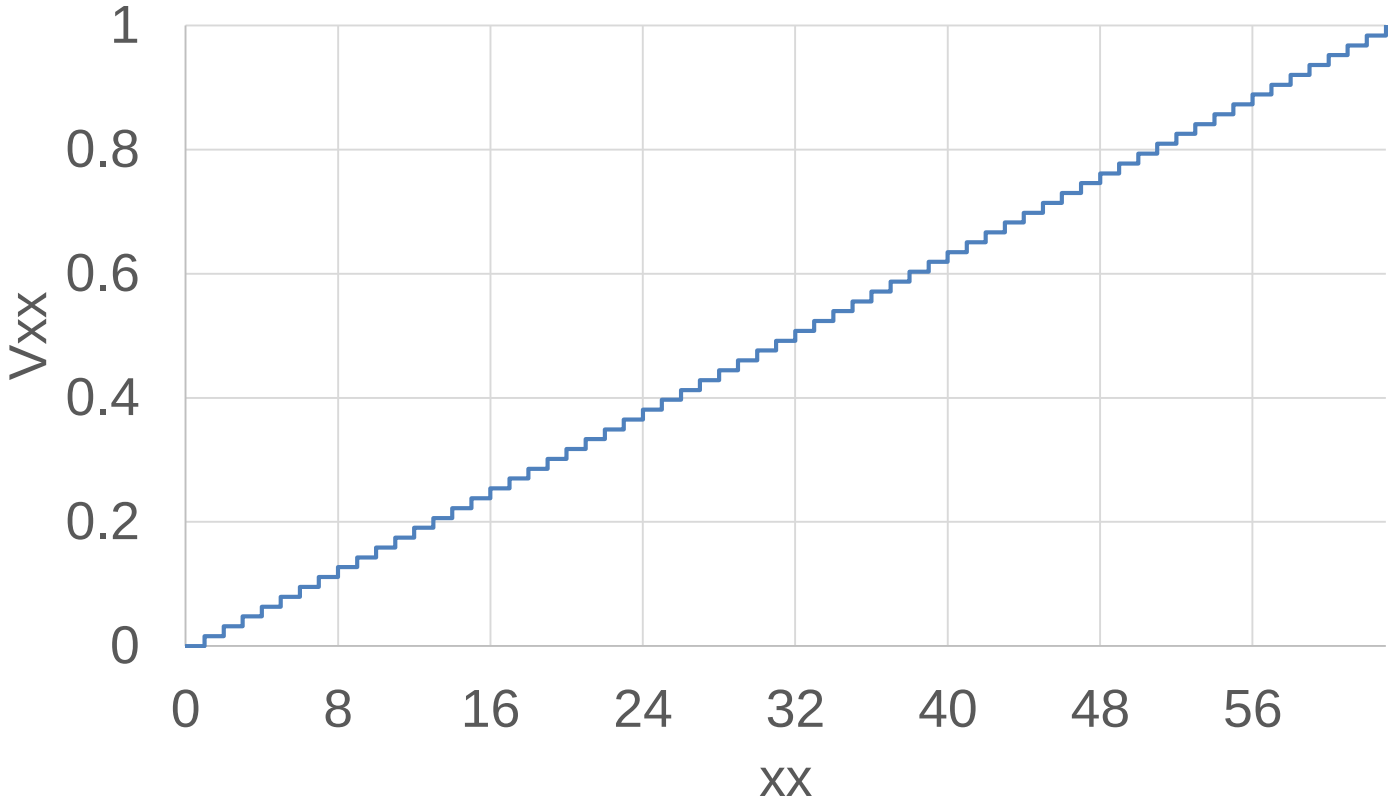


Store Vxx in memory when there is a mismatch

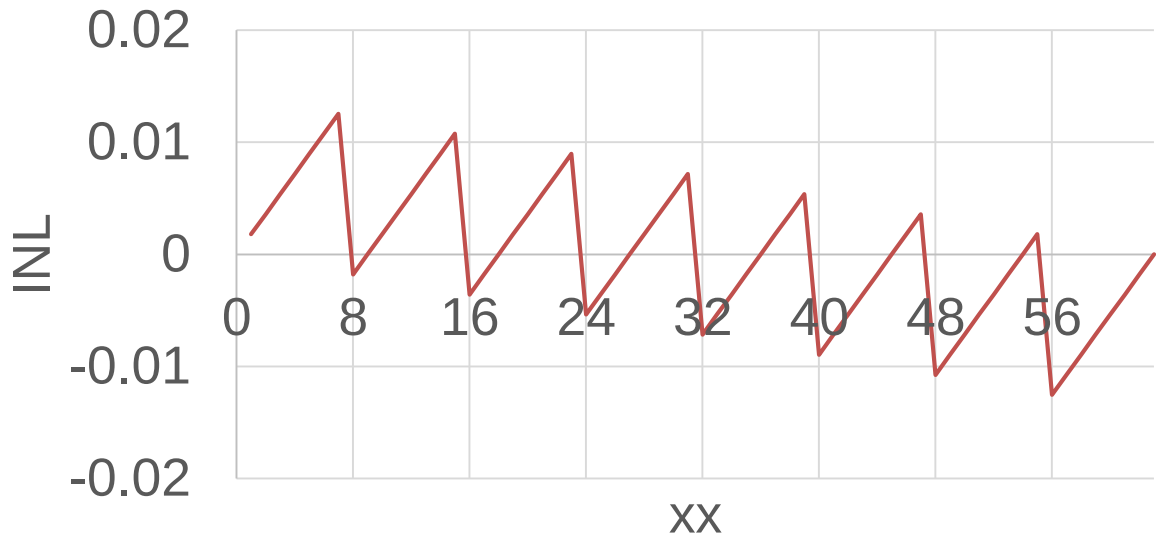
After Correction

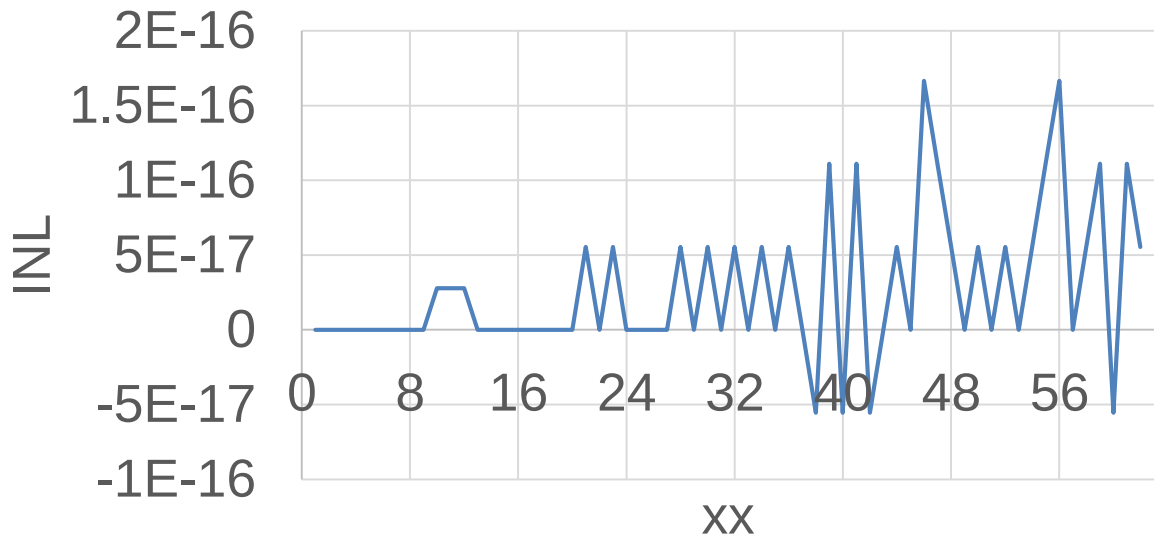
$$\mathrm{Vxx} \times \mathrm{Y} = \frac{\mathrm{xx}}{63}$$

Derive Y and multiply Vxx stored in memory by this Y



Graph of INL





INL is almost 0

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Conclusion

- Effect when split capacitor has parasitic capacitance is analyzed.
- General formula of internal output (Vxx) when there is parasitic capacitance is derived.
- Method of deriving value of parasitic capacitance from the general formula is shown.

Q&A

Q. If there are split capacitor errors and parasitic capacitance at the same time?

A. I haven't verified it yet.
I'll do future research.

Q. What is the advantage of using split capacitor?

A. Since it's not necessary to use a small capacity,
the capacity ratio becomes small and it becomes easy to manufacture.