Proceedings of International Conference on Technology and Social Science 2020 (ICTSS 2020)

Analysis, Testing and Calibration of Charge Distribution SAR ADC Architecture with Split Capacitor

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Keywords: analog-to-digital converter, successive-approximation-register, charge distribution, parasitic capacitance, split capacitor, calibration, non-linearity

Abstract. This paper describes analysis, testing and calibration of the charge distribution SAR ADC with split capacitor. (i) First, the split-capacitor-related parasitic capacitance effects to the overall SAR ADC nonlinearity are analyzed. (ii) Next, capacitor mismatch effects among the split capacitor and binary-weighted capacitors are investigated. (ii) Thirdly, a calibration or compensation method for non-linearity caused by the parasitic capacitors and mismatches are proposed, with using these error data measured at its production testing stage and stored in Flash memory. The charge distribution SAR ADC architecture is now popular which alleviates the problem of the large capacitor ratio in the conventional binary-weighted charge distribution SAR ADC with high resolution, but it has a problem that the parasitic capacitors associated with the split capacitor degrades the overall SAR ADC linearity. Also mismatches among the split capacitor and the binary-weighted capacitors degrades the linearity. We take all of these non-idealities into account; we propose to measure and store them in Flash memory at the production testing stage, and use them for the normal operation in the field. Also at mass production testing stage, by focusing on specific digital codes where nonlinearities are likely to occur due to the split capacitor associated errors, short time testing of the ADC is possible.

1. Introduction

Natural signals such as sound, light, temperature, and pressure in our environments are called analog signals, and are continuous signals in amplitude (like slopes) as well as in time. On the other hand, signals represented by a binary number of 0 or 1 are called digital signals, which are discrete amplitude (like staircases) and sampled signals. It is this digital signal that the digital processor can handle and store in memory. Therefore, a human-recognizable analog signal cannot be processed directly by a digital processor, and an analog-to-digital converter (ADC) that converts the analog signal into a digital signal is required. In recent years, with the development of various electronic devices such as smartphones, ADC technology that converts external analog information so that the electronic devices can process it has become indispensable. This paper uses a method called SAR ADC, which stands for Successive-Approximation-Register Analog-to-Digital Converter.

The ADC is required to produce a digital signal that is as close as possible to the original analog input. Since the charge distribution SAR ADC dealt with in this paper employs an AD conversion method using capacitors, a more accurate digital output can be obtained by using a minute capacitance. However, when a minute capacitance is used, the capacitance ratio with other capacitances in the circuit becomes large, which is difficult to implement accurately. Also notice that since calibration is usually performed by arranging capacitances of the same size, if the capacitances are significantly different in size, accurate calibration becomes difficult and ADC manufacturing becomes impractical [1-5]. Therefore, we have verified a method that can obtain high-precision output without using a minute capacitance by using the split capacitor for the SAR ADC.

In this study, we examine the parasitic capacitance effect caused by using the split capacitor and the measuring method the parasitic capacitance value, and also mismatches among the split capacitor and the binary weighted capacitors as well as their calibration method.

2. Charge distribution SAR ADC configuration

In this section, the circuit configuration and features of the charge distribution SAR ADC are explained. Fig. 1 shows an M-bit charge distribution SAR ADC, which consists of two power supplies, an analog input Vin and a reference voltage Vref, a capacitor array, a comparator, and an SAR logic circuit. In this method, the output from the comparator is sequentially compared and approximated, and the digital output Dout is obtained by switching the switch at the bottom plate of the capacitor. The capacitor array is binary weighted, followed by C, 2C, 4C, and so on. The general formula is approximated as follows, though there can be errors in reality:

$$C_m \cong 2^m C \quad (m = 0, 1, 2, \cdots, M-1) \tag{1}$$

From Eq. (1), the combined capacitance of this circuit is defined as follows by adding the capacitance of the part surrounded by the dotted square in Fig. 1.

$$C_T \equiv 2^{M-1}C + 2^{M-2}C + \cdots + 2C + C + C \tag{2}$$

Unlike the pipelined ADC and the ΔΣ ADC, this SAR ADC does not require high-gain operational amplifiers, which is suitable for designing with fine CMOS with which high gain operational amplifiers are difficult to realize.

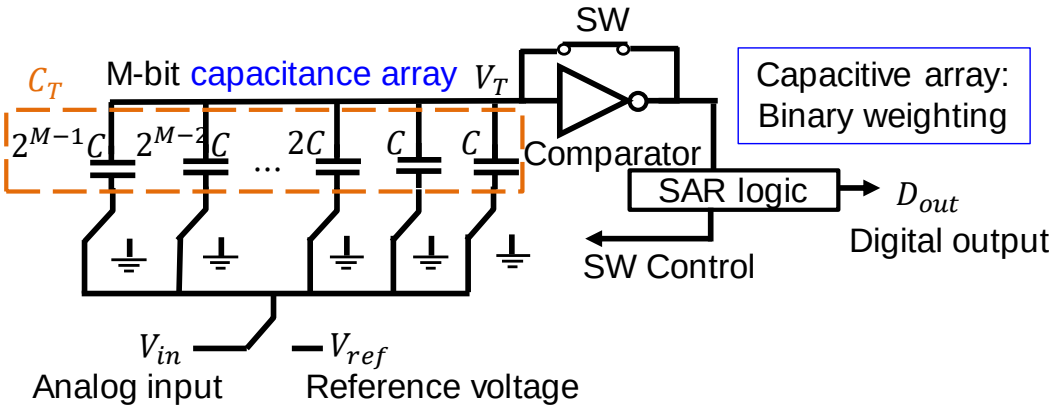


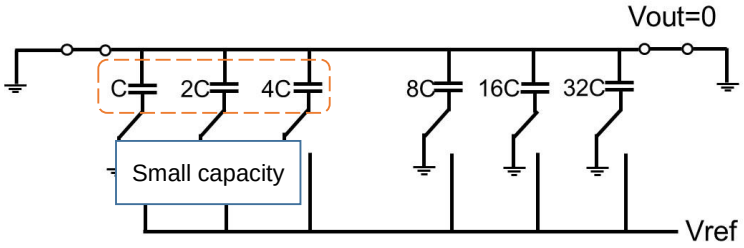
Fig. 1. Circuit configuration of an M-bit SAR ADC by charge redistribution

3. Investigated Charge Distribution SAR ADC

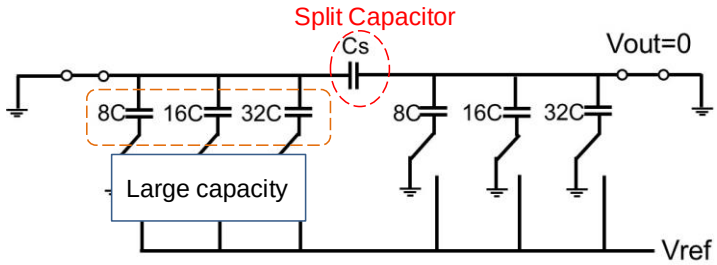
3.1 Charge distribution SAR ADC using split capacitor

Fig. 2 (a) shows a conventional 6-bit charge distribution SAR ADC with a 6-bit binary-weighted capacitor array, and Fig. 2 (b) shows our investigated circuit where two 3-bit binary-weighted capacitor arrays and a split capacitor are used. These two ADC circuits are equivalent; for example, C in Fig. 2 (a) is 8C in Fig. 2 (b), and 2C in Fig. 2 (a) is has been replaced by 16C in Fig. 2 (b). In the conventional circuit in Fig. 2 (a), the minimum capacitance is C and the maximum capacitance is 32C, so the capacitance ratio is 32, which is large, and it is difficult to obtain the ratio accuracy. However, in Fig.2 (b), since a minute capacity is not required by using the split capacitor; the minimum capacitor is 8C and the capacitor ratio is 4, which is small and relatively easy to obtain the ratio accuracy.

In this way, as shown in Fig. 2 (b), by dividing the binary weight into two parts and connecting them with the split capacitor, the large capacitor in series to the split capacitor is equivalent to the small capacitor, so that it is possible to replace a part that originally requires a small capacitor with a large capacitor. As a result, the capacitance ratio in the circuit becomes small, which makes manufacturing realistic.



(a) DAC part of conventional charge distribution SAR ADC



(b) DAC part of charge distribution SAR ADC using split capacitor
Fig. 2. Conventional and investigated circuits/

3.2 Split capacitor calculation

Next, determine the value of the split capacitor. By using the split capacitor for the charge distribution SAR ADC, the combined capacitance on the left side of the split capacitor in Fig. 2 (b) changes, so the capacitance of this part is obtained. Since the capacities of the parts surrounded by the dotted lines other than the split capacitor in Fig. 3 are all in parallel, the value 56C, which is simply the sum of the capacitors, is the combined capacitors of this part. Therefore, this equivalent circuit becomes a series circuit of 56C and split capacitor, and the required combined capacitance is as follows.

$$\frac{1}{\frac{1}{56C}+\frac{1}{C_s}}=\frac{56CC_S}{56C+C_S} \tag{3}$$

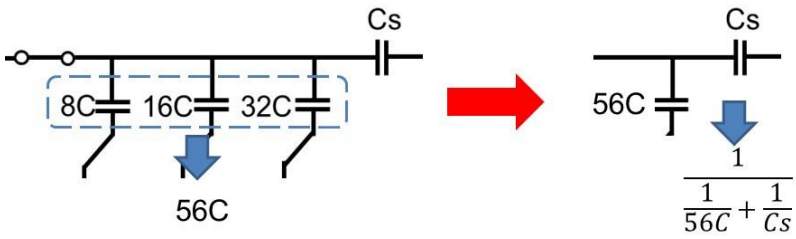


Fig. 3. Equivalent circuit on the left side of split capacitor

The combined capacitance of the obtained Eq. (3) is the capacitance of the left part including the split capacitor in Fig. 2 (b), which is equivalent to the combined capacitance of the part surrounded by the dotted line in the Fig.2 (a) without the split capacitor. Notice that the combined capacitance of the part surrounded by the dotted line in Fig. 2 (a) is as follows:

$$C + 2C + 4C = 7C \tag{4}$$

Then the following equation holds:

$$\frac{56C\,C_S}{56C + C_S} = 7C \tag{5}$$

By solving Eq. (5), the value of the split capacitor becomes as follows:

$$C_S = 8C \tag{6}$$

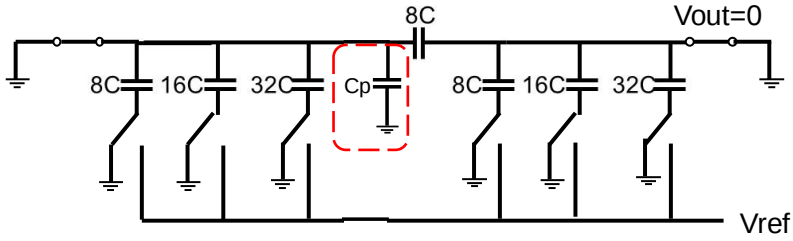
4. Split Capacitor Parasitic Capacitance Problem

The problem of capacitance ratio could be alleviated by using the split capacitor. However, as shown in Fig. 4, parasitic capacitance can be associated with the split capacitor, which causes a new problem of affecting the overall ADC linearity. Therefore, we derived a general formula when there is a parasitic capacitance, and investigated in which part of the output the non-linearity occurs. Furthermore, we have verified the method of obtaining the value of parasitic capacitance from the general formula.

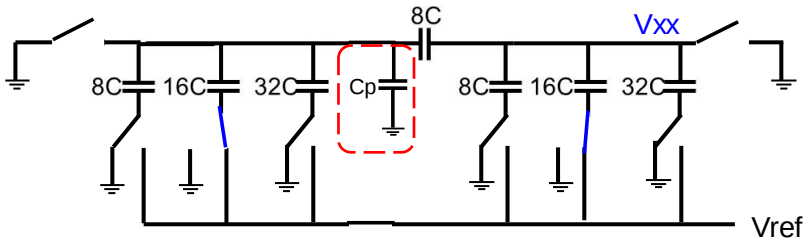
4.1 In case of parasitic capacitance in the left side of split capacitor

Here, we examine the case where there is a parasitic capacitance Cp on the left side of the split capacitor. First, in order to initialize the entire circuit, connect the entire capacitance to GND as shown in Fig. 4 (a) so that the charge amount is 0. Furthermore, turn on the switch on the right side and connect it to GND, and set the potential Vout of this part to 0.

Next, as shown in Fig. 4 (b), turn off the switches at both ends and connect an arbitrary capacitor to Vref. At this time, the value of Vxx changes depending on the capacity connected to Vref. For example, in Fig. 4 (b), the left 16C and the right 16C are connected to Vref, and the left 16C is equivalent to 2C, so here the sum of all capacitors connected to Vref is 2C+16C=18C. Vxx at this time is defined as V18, and the value of each Vxx is calculated.



(a) Conventional charge distribution SAR ADC



(b) Vxx state

Fig. 4. When there is a parasitic capacitance on the left side of the split capacitor

First, we examine the case where there is no parasitic capacitance. When digit xx=01, only 8C on the left side, which is equivalent to C, is Vref-connected, as shown in Fig. 5. Set the potential on the right side of the split capacitor 8C as V01 and the potential on the left side as V01', and calculate the value of V01. When the positive and negative charges are defined as shown in Fig. 5, the initial value is 0 for all charges, so the following equation holds from the law of conservation of electric charge.

$$Q0 + Q1 + Q2 + Q3 + Q4 + Q5 = 0 \tag{7}$$

$$Q0 = 8C(V01' - Vref) \tag{8}$$

$$Q1 = 16CV01' \tag{9}$$

$$Q2 = 32CV01' \tag{10}$$

$$Q3 = 8CV01 \tag{11}$$

$$Q4 = 16CV01 \tag{12}$$

$$Q5 = 32CV01 \tag{13}$$

Substituting Eq. (8) to (13) into Eq. (7),

$$8C(V01' - Vref) + 16CV01' + 32CV01' + 8CV01 + 16CV01 + 32CV01 = 0 \tag{14}$$

Solving Eq. (14) for V01 gives:

$$V01 = \frac{8}{56}Vref - V01' \tag{15}$$

Here, since the value of V01' is unknown, the next step is to find V01'.

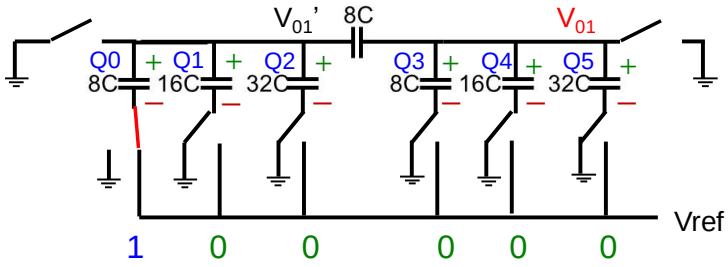


Fig. 5. Circuit diagram when digit xx=01

Since the current flows in the direction of the red arrow in Fig. 6, we see that the current flowing through the split capacitor is divided into 8C, 16C, and 32C on the left side of the Split Capacitor. In other words, since the charge in the split capacitor is the sum of the charges of 8C, 16C and 32C, the

following equation holds:

$$8C(V01 - V01') = 8C(V01' - Vref) + 16CV01' + 32CV01' \tag{16}$$

By solving Eq. (16) for V01', we have the following:

$$V01' = \frac{8Vref + 8V01}{64} \tag{17}$$

Therefore, the unknown value of V01' was obtained. Substituting this Eq. (17) into V01' of Eq. (15),

$$V01 = \frac{8Vref}{56} - \frac{8Vref + 8V01}{64} \tag{18}$$

By solving this for V01, we have the following:

$$V01 = \frac{1}{63}Vref \tag{19}$$

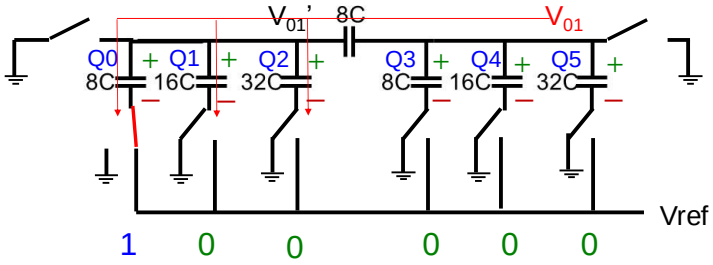


Fig. 6. Current flow when digit xx=01

If the same calculation is performed after xx=02, the formula of Vxx when there is no parasitic capacitance is derived as follows:

$$Vxx = \frac{xx}{63}Vref \tag{20}$$

We see from this equation that Vxx is proportional to xx, so it can be said to be linear.

Table 1 shows the formula derived in the same way when there is a parasitic capacitance. However, it is defined as follows:

$$\alpha = \frac{Cp}{C} \tag{21}$$

Table 1. Vxx formula with parasitic capacitance
(3 capacitances to the left of split capacitor)

xx=00～xx=07	$\mathrm{Vxx} = \frac{8\mathrm{xx}}{63 \times 8 + 8\alpha}\mathrm{Vref}$
xx=08～xx=15	$\mathrm{Vxx} = \frac{8\mathrm{xx} + \alpha}{63 \times 8 + 8\alpha}\mathrm{Vref}$
xx=16～xx=23	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 2\alpha}{63 \times 8 + 8\alpha}\mathrm{Vref}$
xx=24～xx=31	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 3\alpha}{63 \times 8 + 8\alpha}\mathrm{Vref}$

xx=32～xx=39	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 4\alpha}{63 \times 8 + 8\alpha}\mathrm{Vref}$
xx=40～xx=47	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 5\alpha}{63 \times 8 + 8\alpha}\mathrm{Vref}$
xx=48～xx=55	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 6\alpha}{63 \times 8 + 8\alpha}\mathrm{Vref}$
xx=56～xx=63	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 7\alpha}{63 \times 8 + 8\alpha}\mathrm{Vref}$

It was found from Table 1 that the formula of Vxx changes every 8. If there is no parasitic capacitance, Cp=0, that is, α=0, so Vxx=(xx/63)Vref for any xx, which is consistent with the Vxx formula (20) when there is no parasitic capacitance.

Fig. 7 shows a graph of Table 1, and it can be seen that it is non-linear in multiples of digit 8. The reason why the linearity is broken every multiple of digit 8 is that the capacitance on the left side of Split Capacitor is 8C, 16C, 32C, which is equivalent to C, 2C, 4C, so the maximum value represented by the capacitor on the left side of the split capacitor is 7, which is a circuit in which digits are carried up every 8. In other words, the equation of Vxx changes at the timing when the capacitance on the right side of the split capacitor moves up, and the linearity collapses.

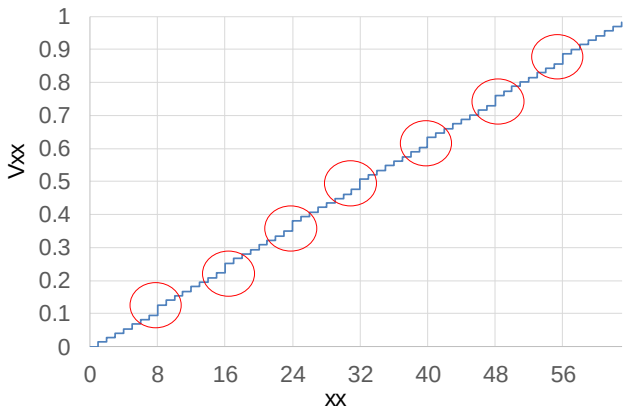


Fig. 7. Effect of parasitic capacitance (3 capacitances to the left of split capacitor)

Next, the circuit on the left side of the split capacitor when the number of capacitors is 2 is verified. In the case of no parasitic capacitance, Vxx=(xx/63)Vref as before, and Vxx became linear in proportion to xx. This is because even if the number of capacitors on the left side of the split capacitor changes from 3 to 2, the total capacitance sum remains 63, so the Vxx formula does not change either.

Furthermore, if the parasitic capacitance Cp is on the left side of the split capacitor, it will be as shown in Table 2.

Table 2. Vxx formula with parasitic capacitance
(2 capacitances to the left of split capacitor)

xx=00～xx=03	$\mathrm{Vxx} = \frac{4\mathrm{xx}}{63 \times 4 + 16\alpha}\mathrm{Vref}$
xx=04～xx=07	$\mathrm{Vxx} = \frac{4\mathrm{xx} + \alpha}{63 \times 4 + 16\alpha}\mathrm{Vref}$

xx=08～xx=11	$\mathrm{Vxx} = \frac{4\mathrm{xx} + 2\alpha}{63 \times 4 + 16\alpha}\mathrm{Vref}$
xx=12～xx=15	$\mathrm{Vxx} = \frac{4\mathrm{xx} + 3\alpha}{63 \times 4 + 16\alpha}\mathrm{Vref}$
xx=16～xx=19	$\mathrm{Vxx} = \frac{4\mathrm{xx} + 4\alpha}{63 \times 4 + 16\alpha}\mathrm{Vref}$
xx=20～xx=23	$\mathrm{Vxx} = \frac{4\mathrm{xx} + 5\alpha}{63 \times 4 + 16\alpha}\mathrm{Vref}$
xx=24～xx=27	$\mathrm{Vxx} = \frac{4\mathrm{xx} + 6\alpha}{63 \times 4 + 16\alpha}\mathrm{Vref}$
xx=28～xx=31	$\mathrm{Vxx} = \frac{4\mathrm{xx} + 7\alpha}{63 \times 4 + 16\alpha}\mathrm{Vref}$

It was found from Table 2 that the formula of Vxx changes every digit 4. In this case as well, if there is no parasitic capacitance, Cp=0, that is, α=0, so Vxx=(xx/63)Vref for any xx, which matches the Vxx formula (20) when there is no parasitic capacitance.

Fig. 8 shows a graph of Table 2, which shows that it is non-linear in multiples of digit 4. The reason why the linearity collapses every multiple of digit 4 is that the formula of Vxx changes at the timing when the capacitance on the right side of the split capacitor moves up as before.

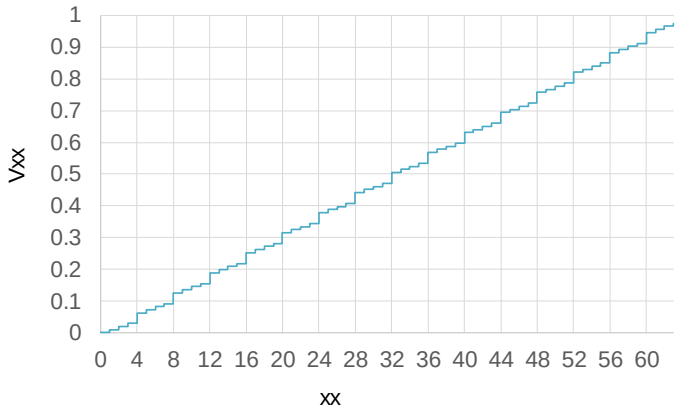


Fig. 8. Effect of parasitic capacitance (2 capacitances to the left of split capacitor)

Finally, the circuit on the left side of the split capacitor when the number of capacities is 4 is verified. In the case of no parasitic capacitance, in this case as well, the total capacity sum 63 is the same as above, so Vxx=(xx/63)Vref, and Vxx is proportional to xx and becomes linear.

Furthermore, if the parasitic capacitance Cp is on the left side of the split capacitor, it will be as shown in Table 3. It was found from Table 3 that the formula of Vxx changes every digit 16. In this case as well, if there is no parasitic capacitance, Cp=0, that is, α=0, so Vxx=(xx/63)Vref for any xx, which matches the Vxx formula (20) when there is no parasitic capacitance.

Fig. 9 shows a graph of Table 3, which shows that it is non-linear in multiples of 16. The reason why the linearity collapses every multiple of 4 is that the formula of Vxx changes at the timing when the capacitance on the right side of the Split Capacitor moves up as before.

Table 3. Vxx formula with parasitic capacitance
(4 capacitances to the left of split capacitor)

xx=00～xx=15	$\mathrm{Vxx}=\dfrac{20\mathrm{xx}}{63\times 20+17\alpha}\mathrm{Vref}$
xx=16～xx=31	$\mathrm{Vxx}=\dfrac{20\mathrm{xx}+4\alpha}{63\times 20+17\alpha}\mathrm{Vref}$
xx=32～xx=47	$\mathrm{Vxx}=\dfrac{20\mathrm{xx}+8\alpha}{63\times 20+17\alpha}\mathrm{Vref}$
xx=48～xx=63	$\mathrm{Vxx}=\dfrac{20\mathrm{xx}+12\alpha}{63\times 20+17\alpha}\mathrm{Vref}$

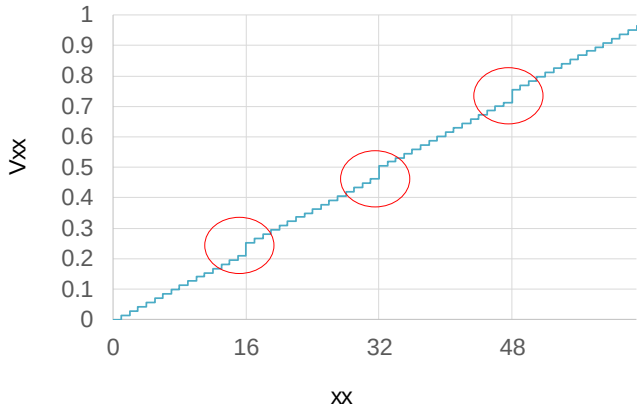


Fig. 9. Effect of parasitic capacitance (4 capacitances to the left of Split Capacitor)

4.2 General formula (when there is parasitic capacitance on the left side of Split Capacitor)

Here, the general formula is derived based on the pattern verified in 4.1. The formula is complicated by the parasitic capacitance, but I will explain it because it turns out that there is a law.

The Vxx formulas in Tables 1 to 3 can be summarized as follows.

$$Vxx=\frac{(Split\ \ Capacitor/C)\times xx+B\alpha}{63\times(Split\ \ Capacitor/C)+A\alpha}Vref \tag{22}$$

Table 4 shows A and B.

Table 4. A and B in Eq. (22)

	Left capacity number 3 Split Capacitor=8C	Left capacity number 2 Split Capacitor=4C	Left capacity number 4 Split Capacitor=20C
A	8	16	17
B	Increase by 1	Increase by 1	Increase by 4

Since 63 in the denominator of Eq. (22) is the sum of total capacitors, and these three patterns differ only in the position of the split capacitor, this sum of total capacitors 63 is common. It is A and B that change depending on the position of the Split Capacitor, and these general formulas are as follows.

$$\mathrm{A}=\frac{\text{Sum of capacity on the right side of Split Capacitor}}{\text{Minimum capacity}}+\frac{\text{Value of Split Capacitor}}{\text{Minimum capacity}} \tag{23}$$

$$B = \frac{\text{Capacitor weight to the right of Split Capacitor}}{\text{Minimum capacity}} \tag{24}$$

It can be said from the above that the general formula of Vxx can be obtained if the shape of the circuit, that is, the sum of total capacitance and the position of the split capacitor is known.

4.3 In case of parasitic capacitance on the right side of the Split Capacitor

Next, as shown in Fig. 10, the case where there is a parasitic capacitance on the right side of the split capacitor was verified in the same way as when there was a parasitic capacitance on the left side. At this time, Vxx becomes Eq. (25), and it was found that the term β of the parasitic capacitance only appears in the denominator and does not become non-linear. The figure shows the circuit when the number of capacitors on the left side of the split capacitor is 3, but the same formula is used when the number of capacitors is 2 or 4. From the above, it was found that when the parasitic capacitance is on the right side, the resolution fluctuates only slightly and the linearity is not affected, and the general formula is the same regardless of the position of the split capacitor.

$$Vxx = \frac{xx}{63 + \beta} Vref \tag{25}$$

$$\beta = \frac{Cp2}{C} \tag{26}$$

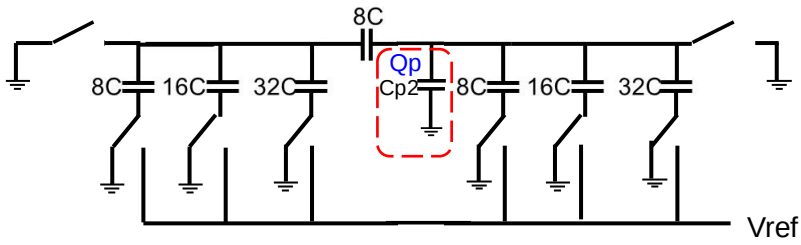


Fig. 10. When there is a parasitic capacitance on the right side of the split capacitor

4.4 How to find the parasitic capacitance value

Using the formula derived above, we explain here how to find the parasitic capacitance value. The parasitic capacitance value (Cp) in Fig. 11 is unknown, and the voltage value of V01 is measured using an internal or external ADC; this time, it is assumed that V01=0.0136986V. First, substituting into Eq. (23) gives the following:

$$A = \frac{56}{8} + \frac{8}{8} = 8 \tag{27}$$

(At this time, since it is V01, it is not necessary to derive B. Since the non-linearity is caused at multiples of digit 8, the term B related to the non-linearity is unnecessary at xx=01 before becoming non-linear.) Substituting this A into Eq. (22) gives the following:

$$Vxx = \frac{8xx}{63 \times 8 + 8\alpha} Vref \tag{28}$$

Substituting digit xx=01 and Vxx=0.0136986V into this formula and setting Vref=1 gives as follows:

$$\alpha = 10.0001606 \tag{29}$$

Dividing the value of α by C gives the value of parasitic capacitance Cp. That is, since the general formula can be obtained from the shape of the circuit, the parasitic capacitance can be derived by

measuring Vxx at a certain xx and substituting it into the general formula. By obtaining the value of the parasitic capacitance, it is possible to predict in advance how much the linearity will be affected, and the ideal output will be possible after subtracting the error for the parasitic capacitance.

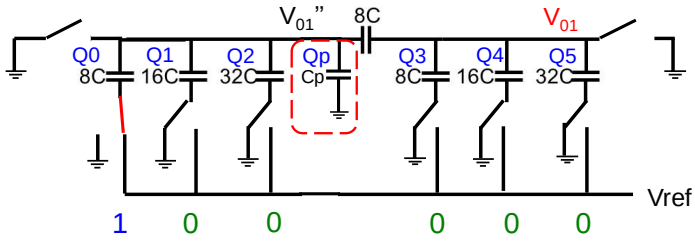


Fig. 11. How to find the parasitic capacitance value associated with the split capacitor.

5. Capacitor Mismatch Effects to SAR ADC Non-Linearity

This section investigates the split capacitor value mismatch effects in the capacitor network in Fig. 11 to the overall non-linearity of the SAR ADC.

5.1 Split capacitor mismatch effects

This subsection investigates the split capacitor value (Cs) mismatch effects to the overall non-linearity of the SAR ADC. Assuming that the mismatch of split capacitor is +Δ8C, the formula of Vxx is as shown in Table 5. Here, γ=Δ8C/C.

Table 5. Vxx formula when there is the mismatch in the split capacitor

xx=00～xx=07	$Vxx = \frac{8xx + \gamma xx}{63 \times 8 + 14\gamma} Vref$
xx=08～xx=15	$Vxx = \frac{8xx + \gamma(xx\text{-}7)}{63 \times 8 + 14\gamma} Vref$
xx=16～xx=23	$Vxx = \frac{8xx + \gamma(xx\text{-}14)}{63 \times 8 + 14\gamma} Vref$
xx=24～xx=31	$Vxx = \frac{8xx + \gamma(xx\text{-}21)}{63 \times 8 + 14\gamma} Vref$
xx=32～xx=39	$Vxx = \frac{8xx + \gamma(xx\text{-}28)}{63 \times 8 + 14\gamma} Vref$
xx=40～xx=47	$Vxx = \frac{8xx + \gamma(xx\text{-}35)}{63 \times 8 + 14\gamma} Vref$
xx=48～xx=55	$Vxx = \frac{8xx + \gamma(xx\text{-}42)}{63 \times 8 + 14\gamma} Vref$
xx=56～xx=63	$Vxx = \frac{8xx + \gamma(xx\text{-}49)}{63 \times 8 + 14\gamma} Vref$

Table 4 shows that the formula changes every time xx is a multiple of 8. In other words, it became clear that if there is the mismatch in the split capacitor, it becomes non-linear every multiple of 8.

The graph of Vxx when the mismatch of split capacitor is 15% is as shown in Fig. 12, and the graph of INL at this time is as shown in Fig. 13. The γ at this time is as shown in Eq. (30).

$$\gamma = \frac{\Delta 8C}{C} = \frac{8C \times 0.15}{C} = 1.2 \tag{30}$$

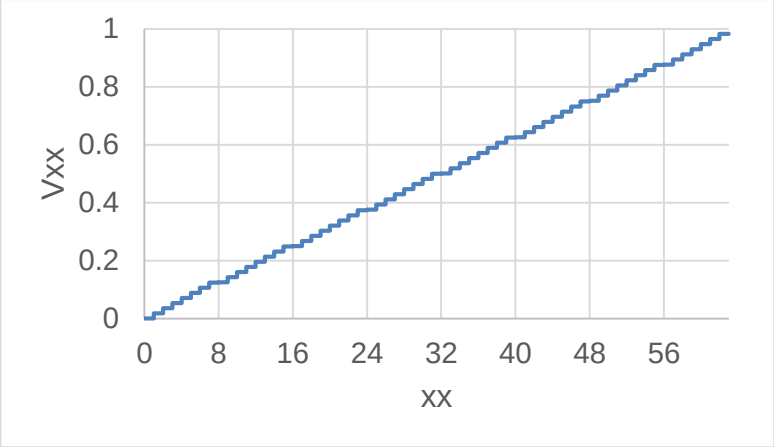


Fig. 12. Vxx in case the mismatch of split capacitor is 15% (Vref=1)

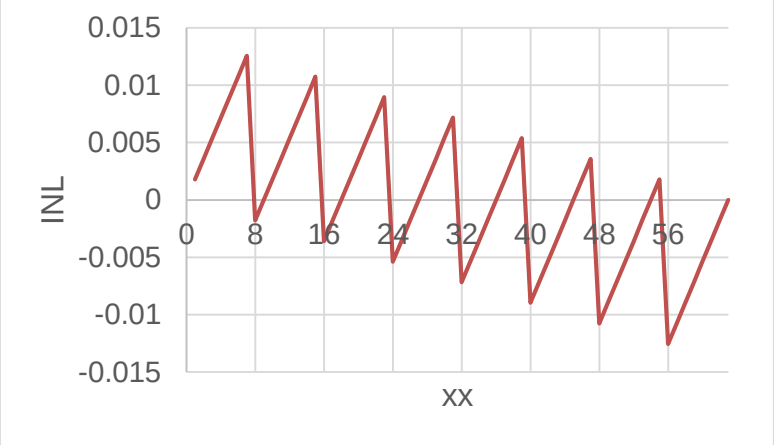


Fig. 13. INL in case the split capacitor mismatch is 15% (Vref=1)

5.2 Capacitor mismatch effects in MSB-side binary-weighted capacitor array

This subsection investigates the capacitor value mismatch effects in MSB-side binary-weighted capacitor array (right-side 8C, 16C in Fig. 11) to the overall non-linearity of the SAR ADC.

First, assuming that the mismatch of right side 8C is +Δ8C, the formula of Vxx is as shown in Table 6. Here, γ=Δ8C/C.

Table 6. Vxx formula when there is the mismatch in the right side 8C

(a) When 8C is Vref connection

xx=08~15	$Vxx = \frac{8xx + 8\gamma}{63 \times 8 + 8\gamma} Vref$
xx=24~31	
xx=40~47	
xx=56~63	

(b) When 8C is GND connection

xx=00~07	

xx=16~23	$Vxx = \frac{8xx}{63 \times 8 + 8\gamma} Vref$
xx=32~39	
xx=48~55	

The graph of Vxx when the mismatch of right side 8C is 12% is as shown in Fig. 14, and the graph of INL at this time is as shown in Fig. 15. The γ at this time is as shown in Eq. (31).

$$\gamma = \frac{\Delta 8C}{C} = \frac{8C \times 0.12}{C} = 0.96 \quad (31)$$

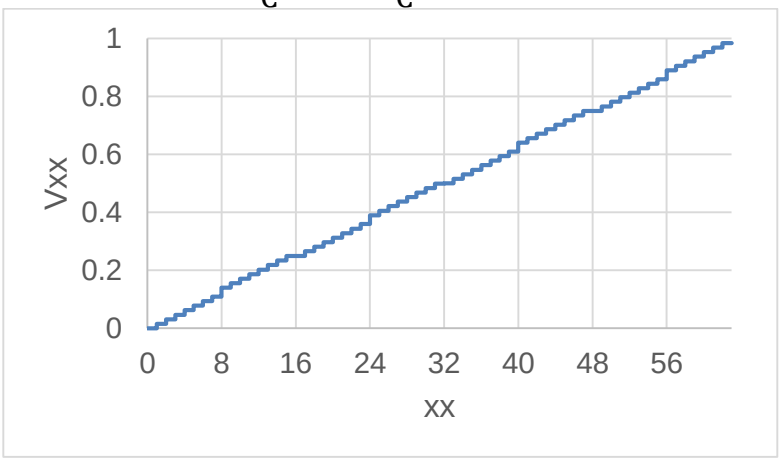


Fig. 14. Vxx in case the mismatch of right side 8C is 12% (Vref=1)

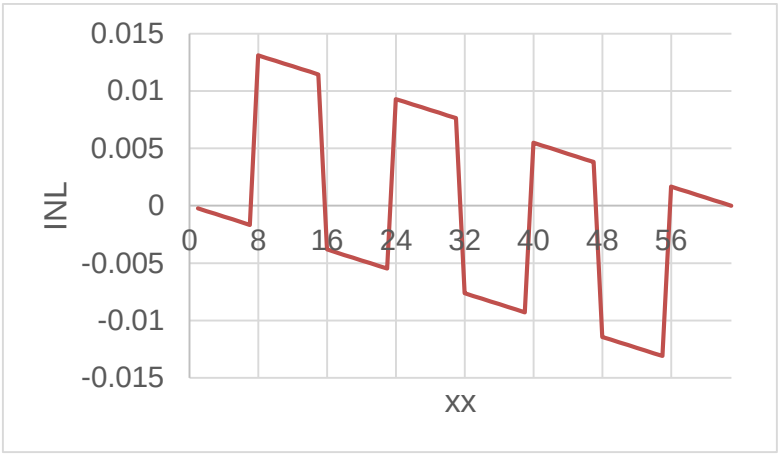


Fig. 15. INL in case the mismatch of right side 8C is 12% (Vref=1)

Next, assuming that the mismatch of right side 16C is +Δ16C, the formula of Vxx is as shown in Table 7. Here, γ=Δ16C/C.

Table 7. Vxx formula when there is the mismatch in the right side 16C

(a) When 16C is Vref connection

xx=16~31	$Vxx = \frac{8xx + 8\gamma}{63 \times 8 + 8\gamma} Vref$
xx=48~63	

(b) When 16C is GND connection

xx=00~15	$Vxx = \frac{8xx}{63 \times 8 + 8\gamma} Vref$
xx=32~47	

The graph of Vxx when the mismatch of right side 16C is 12% is as shown in Fig. 16, and the graph of INL at this time is as shown in Fig. 17. The γ at this time is as shown in Eq. (32).

$$\gamma = \frac{\Delta 16C}{C} = \frac{16C \times 0.12}{C} = 1.92 \quad (32)$$

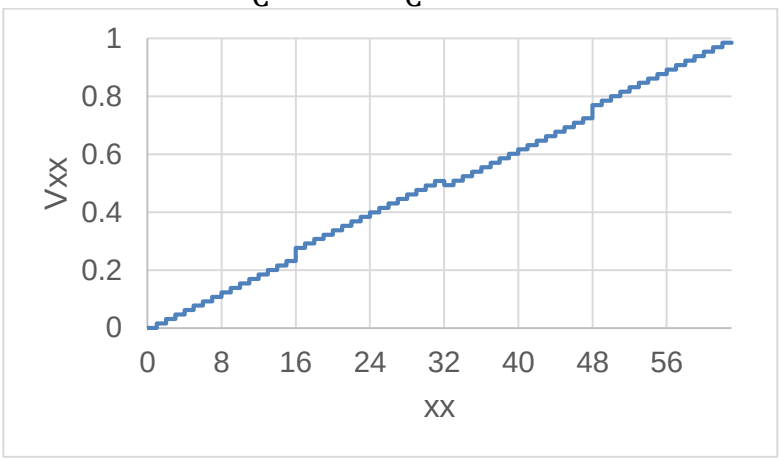


Fig. 16. Vxx in case the mismatch of right side 16C is 12% (Vref=1)

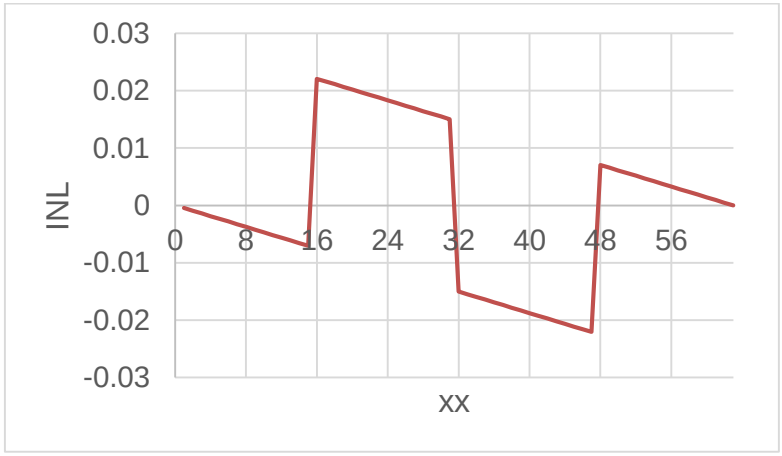


Fig. 17. INL in case the mismatch of right side 16C is 12% (Vref=1)

5.3 Capacitor mismatch effects in LSB-side binary-weighted capacitor array

This subsection investigates the capacitor value mismatch effects in LSB-side binary-weighted capacitor array (left-side 8C, 16C in Fig. 11) to the overall non-linearity of the SAR ADC.

First, assuming that the mismatch of left side 8C is +Δ8C, the formula of Vxx is as shown in Table 8. Here, γ=Δ8C/C.

Table 8. Vxx formula when there is the mismatch in the left side 8C

(a) In case 8C is connected to Vref (When xx is odd)

xx=01, 03, 05, 07	$\mathrm{Vxx} = \frac{8\mathrm{xx} + \gamma}{63 \times 8 + 8\gamma}\mathrm{Vref}$
xx=09, 11, 13, 15	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 2\gamma}{63 \times 8 + 8\gamma}\mathrm{Vref}$
xx=17, 19, 21, 23	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 3\gamma}{63 \times 8 + 8\gamma}\mathrm{Vref}$
xx=25, 27, 29, 31	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 4\gamma}{63 \times 8 + 8\gamma}\mathrm{Vref}$
xx=33, 35, 37, 39	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 5\gamma}{63 \times 8 + 8\gamma}\mathrm{Vref}$
xx=41, 43, 45, 47	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 6\gamma}{63 \times 8 + 8\gamma}\mathrm{Vref}$
xx=49, 51, 53, 55	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 7\gamma}{63 \times 8 + 8\gamma}\mathrm{Vref}$
xx=57, 59, 61, 63	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 8\gamma}{63 \times 8 + 8\gamma}\mathrm{Vref}$

(b) In case 8C is connected to GND (When xx is even)

xx=00, 02, 04, 06	$\mathrm{Vxx} = \frac{8\mathrm{xx}}{63 \times 8 + 8\gamma}\mathrm{Vref}$
xx=08, 10, 12, 14	$\mathrm{Vxx} = \frac{8\mathrm{xx} + \gamma}{63 \times 8 + 8\gamma}\mathrm{Vref}$
xx=16, 18, 20, 22	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 2\gamma}{63 \times 8 + 8\gamma}\mathrm{Vref}$
xx=24, 26, 28, 30	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 3\gamma}{63 \times 8 + 8\gamma}\mathrm{Vref}$
xx=32, 34, 36, 38	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 4\gamma}{63 \times 8 + 8\gamma}\mathrm{Vref}$
xx=40, 42, 44, 46	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 5\gamma}{63 \times 8 + 8\gamma}\mathrm{Vref}$
xx=48, 50, 52, 54	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 6\gamma}{63 \times 8 + 8\gamma}\mathrm{Vref}$
xx=56, 58, 60, 62	$\mathrm{Vxx} = \frac{8\mathrm{xx} + 7\gamma}{63 \times 8 + 8\gamma}\mathrm{Vref}$

The graph of Vxx when the mismatch of left side 8C is -6% is as shown in Fig. 18, and the graph of INL at this time is as shown in Fig. 19. The γ at this time is as shown in Eq. (33).

$$\gamma = \frac{\Delta 8C}{C} = \frac{8C \times (-0.06)}{C} = -0.48 \tag{33}$$

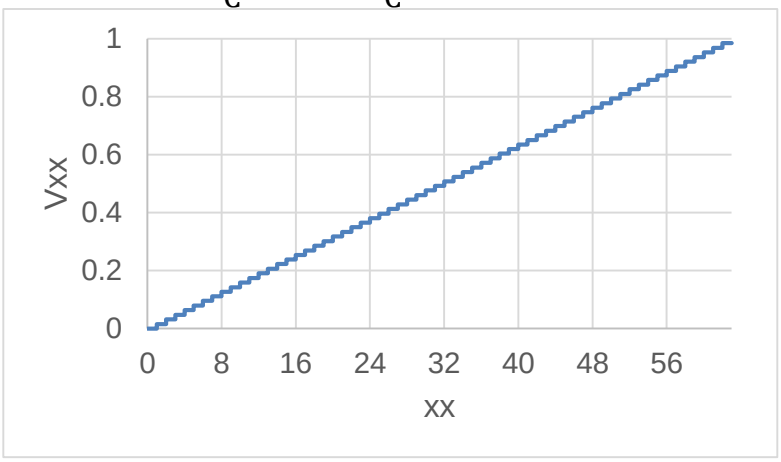


Fig. 18. Vxx in case the mismatch of left side 8C is -6% (Vref=1)

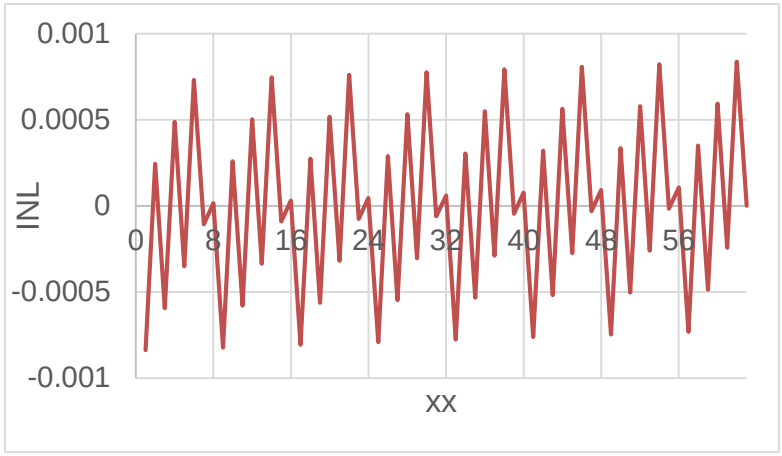


Fig. 19. INL in case the mismatch of left side 8C is -6% (Vref=1)

Next, assuming that the mismatch of left side 16C is +Δ16C, the formula of Vxx is as shown in Table 9. Here, γ=Δ16C/C.

Table 9. Vxx formula when there is the mismatch in the left side 16C

(a) When 16C is connected to Vref

xx=02, 03, 06, 07	$Vxx = \frac{8xx + \gamma}{63 \times 8 + 8\gamma} Vref$
xx=10, 11, 14, 15	$Vxx = \frac{8xx + 2\gamma}{63 \times 8 + 8\gamma} Vref$
xx=18, 19, 22, 23	$Vxx = \frac{8xx + 3\gamma}{63 \times 8 + 8\gamma} Vref$
xx=26, 27, 30, 31	$Vxx = \frac{8xx + 4\gamma}{63 \times 8 + 8\gamma} Vref$
xx=34, 35, 38, 39	$Vxx = \frac{8xx + 5\gamma}{63 \times 8 + 8\gamma} Vref$

xx=42, 43, 46, 47	$Vxx = \frac{8xx + 6\gamma}{63 \times 8 + 8\gamma} Vref$
xx=50, 51, 54, 55	$Vxx = \frac{8xx + 7\gamma}{63 \times 8 + 8\gamma} Vref$
xx=58, 59, 62, 63	$Vxx = \frac{8xx + 8\gamma}{63 \times 8 + 8\gamma} Vref$

(b) In case 16C is connected to GND

xx=00, 01, 04, 05	$Vxx = \frac{8xx}{63 \times 8 + 8\gamma} Vref$
xx=08, 09, 12, 13	$Vxx = \frac{8xx + \gamma}{63 \times 8 + 8\gamma} Vref$
xx=16, 17, 20, 21	$Vxx = \frac{8xx + 2\gamma}{63 \times 8 + 8\gamma} Vref$
xx=24, 25, 28, 29	$Vxx = \frac{8xx + 3\gamma}{63 \times 8 + 8\gamma} Vref$
xx=32, 33, 36, 37	$Vxx = \frac{8xx + 4\gamma}{63 \times 8 + 8\gamma} Vref$
xx=40, 41, 44, 45	$Vxx = \frac{8xx + 5\gamma}{63 \times 8 + 8\gamma} Vref$
xx=48, 49, 52, 53	$Vxx = \frac{8xx + 6\gamma}{63 \times 8 + 8\gamma} Vref$
xx=56, 57, 60, 61	$Vxx = \frac{8xx + 7\gamma}{63 \times 8 + 8\gamma} Vref$

The graph of Vxx when the mismatch of left side 16C is -6% is as shown in Fig. 20, and the graph of INL at this time is as shown in Fig. 21. γ at this time is as shown in Eq. (34).

$$\gamma = \frac{\Delta 16C}{C} = \frac{16C \times (-0.06)}{C} = -0.96 \quad (34)$$

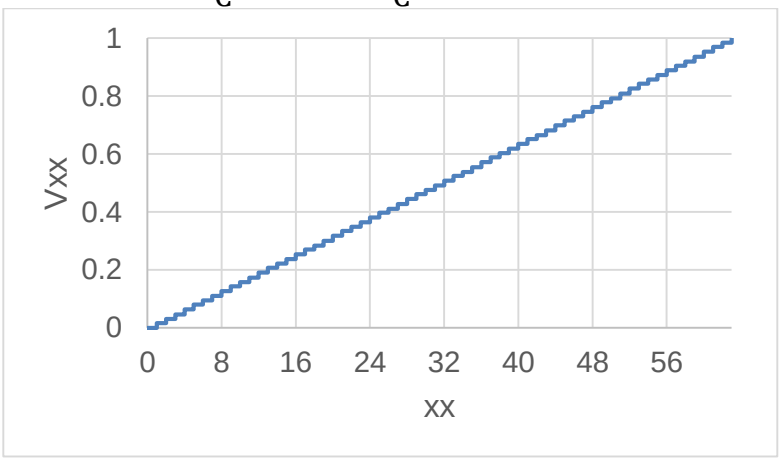


Fig. 20. Vxx in case the mismatch of left side 16C is -6% (Vref=1)

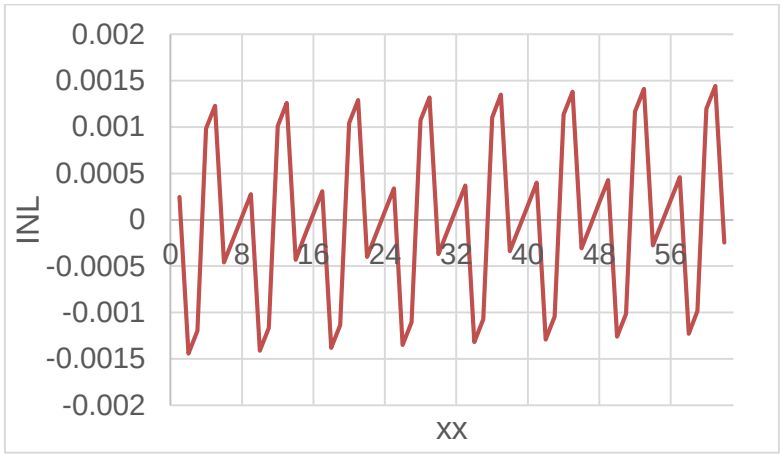


Fig. 21. INL in case the mismatch of left side 16C is -6% (Vref=1)

From the above, when the capacitance with mismatch is connected to GND, the formula is the same as when there is a parasitic capacitance in split capacitor, so if there is the mismatch in the capacitance on the right side, it becomes linear, and there is the mismatch in the capacitance on the left side, it becomes non-linear. Therefore, the accuracy of the capacitance on the left side affects the linearity, so high accuracy is important. On the other hand, when the capacitance with the mismatch is Vref-connected, the term of the mismatch of the numerator becomes large, so that the mismatch becomes larger than when the split capacitor has a parasitic capacitance. At this time, both when there is the mismatch in the capacitance on the right side and when there is the mismatch in the capacitance on the left side, it becomes non-linear. Also, if there is the mismatch in the left 8C, it is non-linear every other, if there is an error in the left 16C, it is non-linear, if there is an error in the right 8C, it is non-linear every eight, and if there is the mismatch in the right 16C, it is non-linear every 16th, and it was found that the capacitance with the mismatch becomes non-linear in the code connected by Vref as a whole graph.

6. Testing and Calibration

We propose here the calibration of parasitic capacitance effects associated with the split capacitor by measuring the integral non-linearity (INL) SAR ADC at the production testing stage [6]; the measured data is stored in Flash memory. During its normal operation in the field, the raw DAC output is corrected with some calibration DAC s based on the data in Flash memory and its linearity can be improved. Simulation results with specific numerical examples are shown.

Case 1: Assuming a mismatch of 12% of the capacity on the MSB side

When there is a 12% mismatch in 8C on the right side, $\Delta 8C=8C\times0.12=0.96C$, so $\gamma=\Delta 8C/C=0.96$. First of all, the value of Vxx is stored in the memory. Vxx at this time is shown in Table 10.

Table 10. Vxx formula when there is the 12% mismatch in the right side 8C

(a) When 8C is connected to Vref

xx=08~15	$Vxx=\frac{8xx+7.68}{511.68}Vref$
xx=24~31	
xx=40~47	

xx=56~63	

(b) When 8C is connected to GND

xx=00~07	$Vxx = \frac{8xx}{511.68}Vref$
xx=16~23	
xx=32~39	
xx=48~55	

Multiplying a value Y in the formula at this time to obtain an ideal formula xx/63 with no mismatch gives the following.

$$Vxx \times Y = \frac{xx}{63} \tag{35}$$

Solving this for Y gives:

$$Y = \frac{xx}{63Vxx} \tag{36}$$

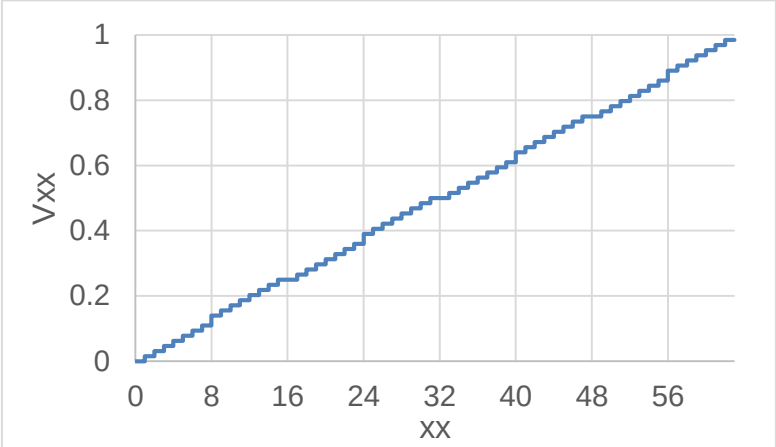
Therefore, the correction formula in the Table 10 (a) is

$$Y = \frac{511.68xx}{63(8xx + 7.68)Vref} \tag{37}$$

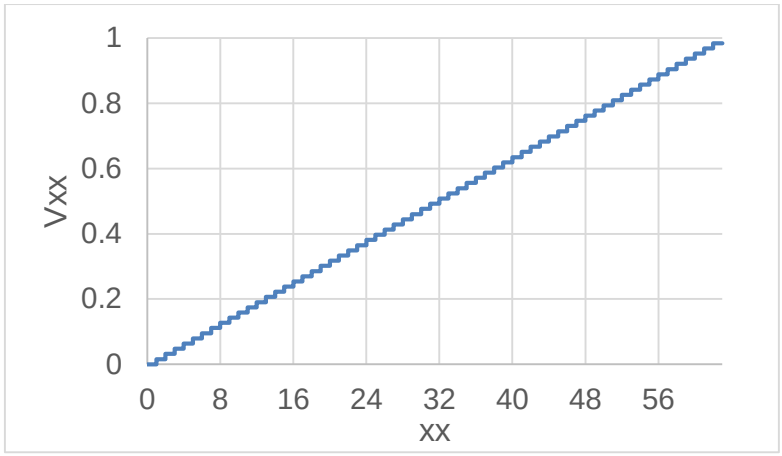
The correction formula in the Table 10 (b) is

$$Y = \frac{511.68}{63 \times 8Vref} \tag{38}$$

When the correction formula (37), (38) is multiplied by the Vxx stored in the memory, the Vxx is corrected as shown in the Fig. 22. Here, Vref=1.



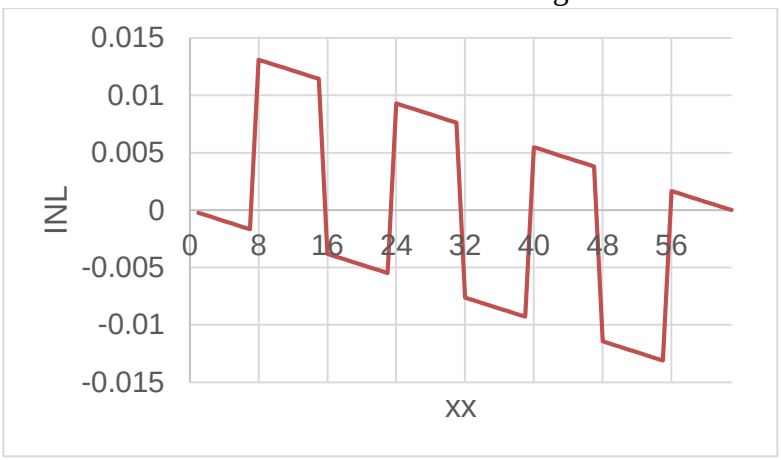
(a) Before correction



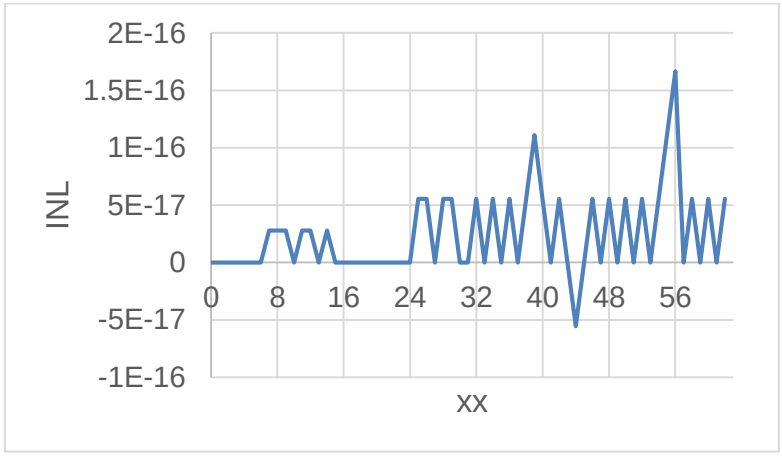
(b) After correction

Fig. 22 Vxx in case the mismatch of right side 8C is 12%

The graphs of INL before and after correction are shown in Fig. 23.



(a) Before correction



(b) After correction

Fig. 23 INL when the mismatch of right side 8C is 12%

In this way, the corrected INL is as close to 0 as possible, which is an ideal value.

Case 2: Assuming a mismatch of -6% of the capacity on the LSB side

When there is a -6% mismatch in 16C on the left side, Δ16C=16C×(-0.06)=-0.96C, so γ=Δ16C/C=-0.96. First of all, the value of Vxx is stored in the memory. Vxx at this time is shown in Table 11.

Table 11. Vxx formula in case there is -6% mismatch in the left side 16C

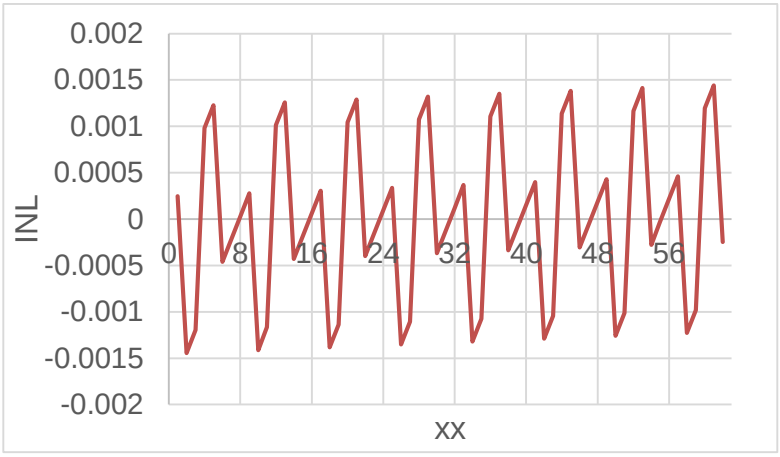
(a) In case 16C is connected to Vref.

xx=02, 03, 06, 07	$\mathrm{Vxx}=\frac{8\mathrm{xx}-0.96}{496.32}\mathrm{Vref}$
xx=10, 11, 14, 15	$\mathrm{Vxx}=\frac{8\mathrm{xx}-1.92}{496.32}\mathrm{Vref}$
xx=18, 19, 22, 23	$\mathrm{Vxx}=\frac{8\mathrm{xx}-2.88}{496.32}\mathrm{Vref}$
xx=26, 27, 30, 31	$\mathrm{Vxx}=\frac{8\mathrm{xx}-3.84}{496.32}\mathrm{Vref}$
xx=34, 35, 38, 39	$\mathrm{Vxx}=\frac{8\mathrm{xx}-4.8}{496.32}\mathrm{Vref}$
xx=42, 43, 46, 47	$\mathrm{Vxx}=\frac{8\mathrm{xx}-5.76}{496.32}\mathrm{Vref}$
xx=50, 51, 54, 55	$\mathrm{Vxx}=\frac{8\mathrm{xx}-6.72}{496.32}\mathrm{Vref}$
xx=58, 59, 62, 63	$\mathrm{Vxx}=\frac{8\mathrm{xx}-7.68}{496.32}\mathrm{Vref}$

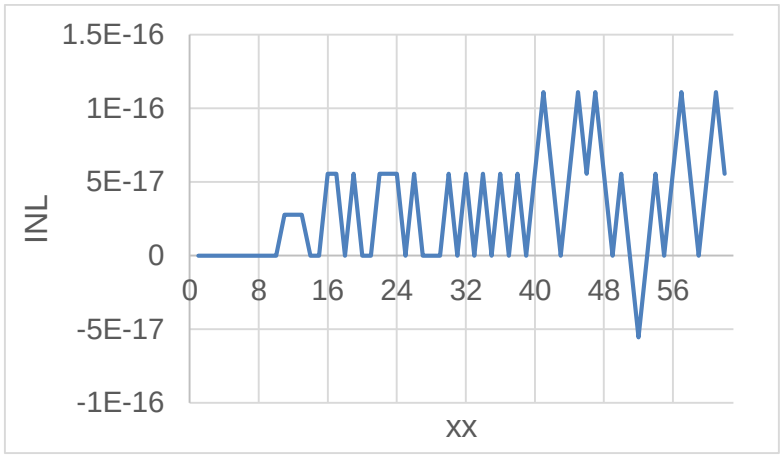
(b) In case 16C is connected GND

xx=00, 01, 04, 05	$\mathrm{Vxx}=\frac{8\mathrm{xx}}{496.32}\mathrm{Vref}$
xx=08, 09, 12, 13	$\mathrm{Vxx}=\frac{8\mathrm{xx}-0.96}{496.32}\mathrm{Vref}$
xx=16, 17, 20, 21	$\mathrm{Vxx}=\frac{8\mathrm{xx}-1.92}{496.32}\mathrm{Vref}$
xx=24, 25, 28, 29	$\mathrm{Vxx}=\frac{8\mathrm{xx}-2.88}{496.32}\mathrm{Vref}$
xx=32, 33, 36, 37	$\mathrm{Vxx}=\frac{8\mathrm{xx}-3.84}{496.32}\mathrm{Vref}$
xx=40, 41, 44, 45	$\mathrm{Vxx}=\frac{8\mathrm{xx}-4.8}{496.32}\mathrm{Vref}$
xx=48, 49, 52, 53	$\mathrm{Vxx}=\frac{8\mathrm{xx}-5.76}{496.32}\mathrm{Vref}$
xx=56, 57, 60, 61	$\mathrm{Vxx}=\frac{8\mathrm{xx}-6.72}{496.32}\mathrm{Vref}$

If the correction is performed in the same way as in case 1, it will be as shown in Fig. 24. Since it is difficult to understand that Vxx is non-linear at this time, the comparison of Vxx is omitted and only INL is shown.



(a) Before correction



(b) After correction

Fig. 24 INL in case the mismatch of left side 16C is -6%

In this way, the corrected INL is as close to 0 as possible, which is an ideal value.

Case 3: Assuming a mismatch of 15% of the split capacitor

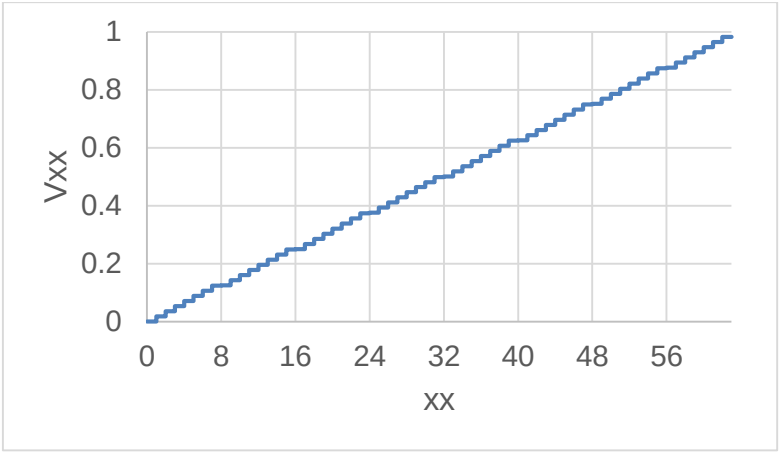
When there is a 15% mismatch in 8C on the split capacitor, $\Delta 8C=8C\times(0.15)=1.2C$, so $\gamma=\Delta 8C/C=1.2$. First of all, the value of Vxx is stored in the memory. Vxx at this time is shown in Table 12.

Table 12. Vxx formula in case there is 15% mismatch in the split capacitor

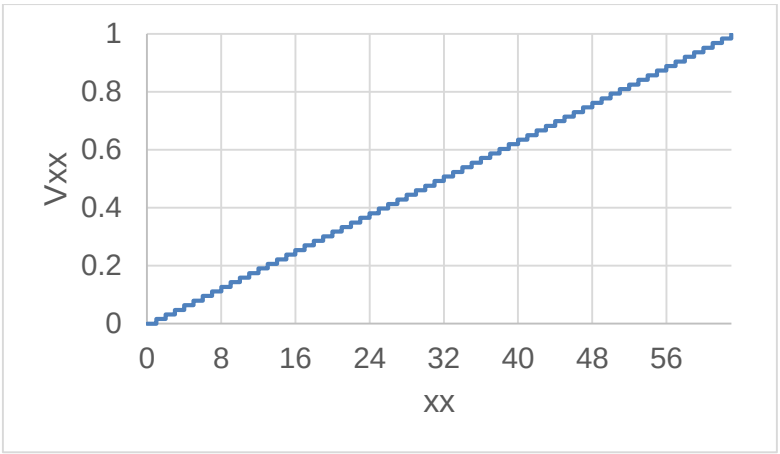
xx=00～xx=07	$Vxx=\frac{8xx+1.2xx}{520.8}Vref$
xx=08～xx=15	$Vxx=\frac{8xx+1.2(xx\text{-}7)}{520.8}Vref$
xx=16～xx=23	$Vxx=\frac{8xx+1.2(xx\text{-}14)}{520.8}Vref$

xx=24～xx=31	$Vxx = \frac{8xx + 1.2(xx\text{-}21)}{520.8} Vref$
xx=32～xx=39	$Vxx = \frac{8xx + 1.2(xx\text{-}28)}{520.8} Vref$
xx=40～xx=47	$Vxx = \frac{8xx + 1.2(xx\text{-}35)}{520.8} Vref$
xx=48～xx=55	$Vxx = \frac{8xx + 1.2(xx\text{-}42)}{520.8} Vref$
xx=56～xx=63	$Vxx = \frac{8xx + 1.2(xx\text{-}49)}{520.8} Vref$

If the correction is performed in the same way as in case 1,2, it will be as shown in Fig. 25.



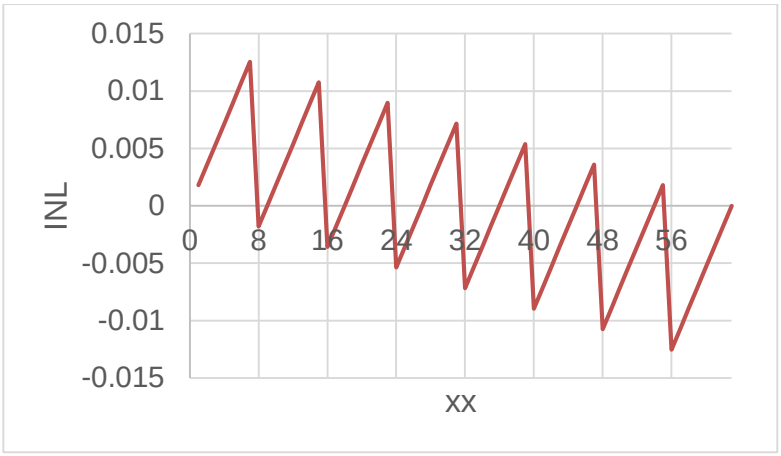
(a) Before correction



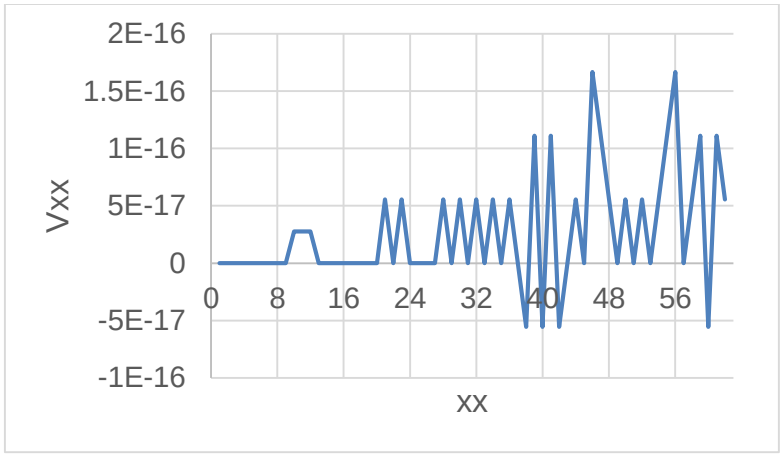
(b) After correction

Fig. 25 Vxx in case the mismatch of split capacitor is 15%

The graphs of INL before and after correction are shown in Fig. 26.



(a) Before correction



(b) After correction

Fig. 26 INL in case the mismatch of split capacitor is 15%

In this way, the corrected INL is as close to 0 as possible, which is an ideal value. Therefore, even if at other xx or there is the mismatch in other places, a linear ideal value can be obtained by deriving Y with the mismatch value γ substituted and multiplying it to the measurement data.

7. Conclusion

In this paper, we have explained a charge redistribution SAR ADC using a split capacitor, which solves the problem that the capacitance ratio in the circuit of the conventional charge distribution SAR ADC becomes large. For the new problem that parasitic capacitance is generated at both ends of the split capacitor and affects the output linearity by using split capacitor, the general formulas for the case where the parasitic capacitance is on the left and right are derived respectively. Furthermore, the method of calculating the value of parasitic capacitance from the general formula is shown. By clarifying the value of parasitic capacitance, it became possible to predict in advance how much non-linearity would occur in which code, and the problem of non-linearity, which had been a problem, could be solved. Also mismatches among the split capacitor and the binary-weighted capacitors are analyzed. Then a calibration method at production testing stage is described with several examples.

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