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Efficient Linearity Self- Calibration Condition with Histogram Method for Time-to-Digital Converter

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Abstract. This paper describes efficient linearity self-calibration condition with histogram method for a flash-type time-to-digital converter (TDC). There two clock signals with different frequencies are used and we have investigated their ratio for high efficiency calibration. We have found with simulations that when it is a golden ratio, the calibration can be done efficiently. This is inspired by our another research related to the equivalent time sampling technique in the sampling oscilloscope.

1. Introduction

This paper investigates a linearity self-calibration method with a histogram method for a flash-type time-to-digital converter (TDC). There in the calibration mode, two clock signals with different frequencies f1, f2 are used as the TDC input signals [1-3]. We have found that the frequency ratio of f1/f2 is a golden ratio [4], silver ratio, or other metallic ratios, the linearity self-calibration can be done accurately in short time. On the other hand, the ratio is some value, the accurate self-calibration is not achieved efficiently. We have found that this is similar to so-called waveform missing phenomena of the equivalent-time sampling technique used in sampling oscilloscopes [5-9]. We have performed theoretical analysis and simulation to confirm the validation of our results.

2. Time-to-Digital Converter

In electronic instrumentation and signal processing, a time-to-digital converter (abbreviated as TDC) is used as a device for recognizing timing events and providing a digital representation of the time they occurred. For example, the TDC might output the time of arrival for each incoming pulse. Some applications wish to measure the time interval between two timing events rather than some notion of an absolute time.

The TDC is used in many different applications, where the time interval between two signal pulses (start and stop pulses) should be determined. Measurement is started and stopped, when either the rising or the falling edge of a signal pulse crosses a set threshold. These requirements are fulfilled in

many physical experiments, like time-of-flight and lifetime measurements in atomic and high energy physics, experiments that involve laser ranging and electronic research involving the testing of integrated circuits and high-speed data transfer.

Figure 1 shows the configuration of a basic flash-type TDC; the reference CLK passes through a buffer delay line, which consists of a chain of inverters, and the delayed reference CLK signals are used as the data input for some flip-flop (DFF) circuits. The measured signal is used as the clock signal of the flip-flops. We obtain the outputs of the flip-flops as a thermometer code, according to the rise-edge-timing interval between the reference "START" edge and the "STOP" edge, and the encoder transforms it into a binary code. The time resolution is determined by the gate delay τ .

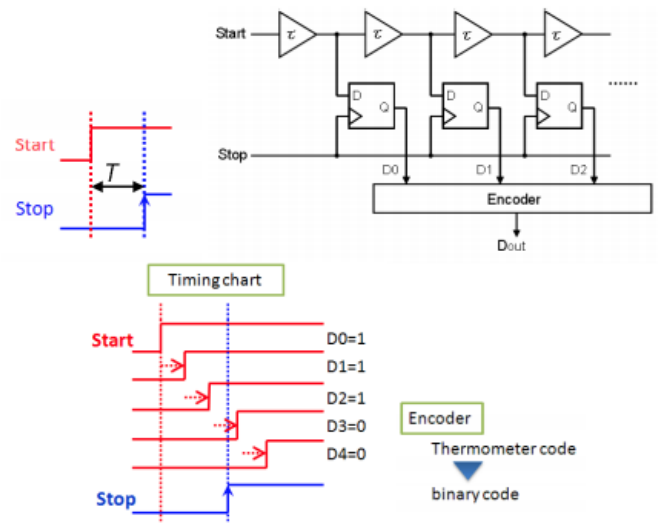


Fig. 1. Flash-type TDC architecture and operation.

3. Linearity Self-Calibration with Histogram Method for Time-to-Digital Converter

The investigated TDC has self-calibration circuits to compensate for this nonlinearity. Our TDC uses a two-ring-oscillator configuration in the self-calibration mode, as shown in Figs. 2 and 3. Since the oscillation frequencies of the two oscillators are different from each other and not synchronized, the histograms in all bins would be equal, after collection of a sufficiently large number of data, if the TDC had perfect linearity. In self-calibration mode, the histogram engine collects histogram data as DNL values, and obtains INL by accumulating the DNL values. Then it calculates the inverse function of the INL values and stores them in memory.

In normal operation mode, the encoder output is corrected by the inverse function of the INL values in memory, to obtain linear TDC input-output characteristics. The above self-calibration can be done using all-digital methods, and Fig. 5 shows simulation results.

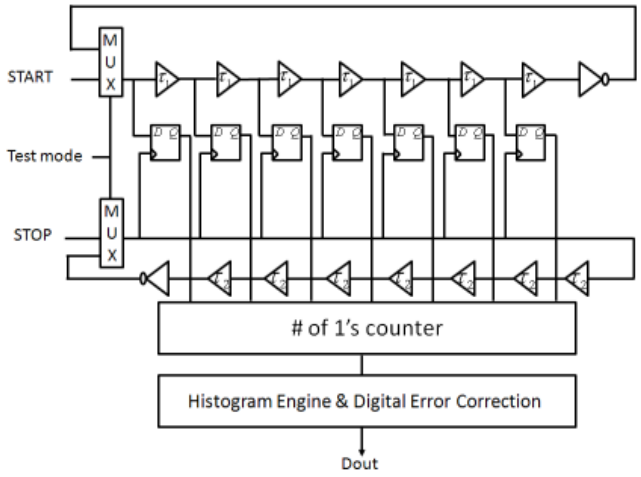


Fig.2. Flash-type TDC architecture with self-calibration.

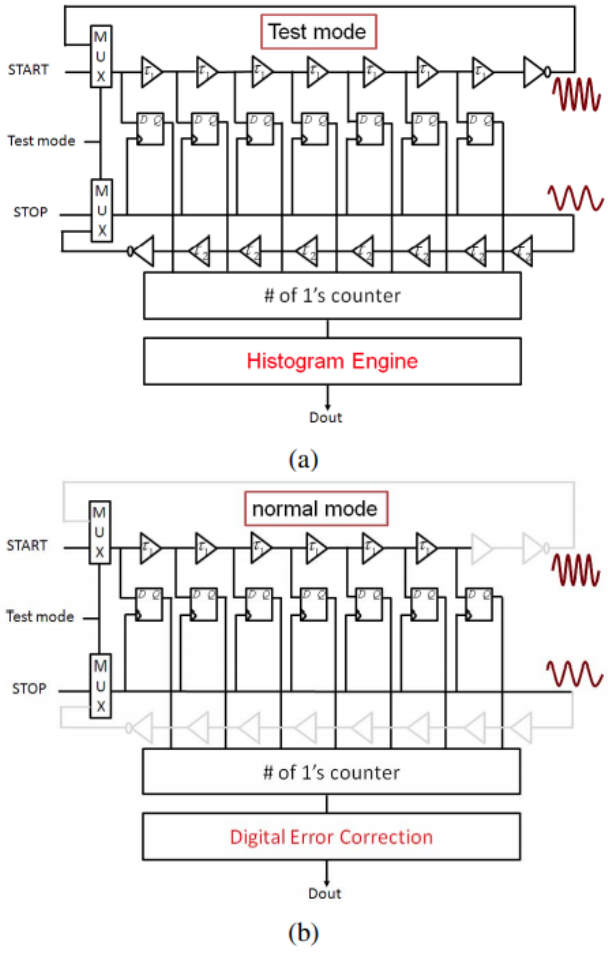


Fig. 3. Operation of the flash-type TDC architecture with self-calibration.
(a) Self-calibration mode. (b) Normal operation mode.

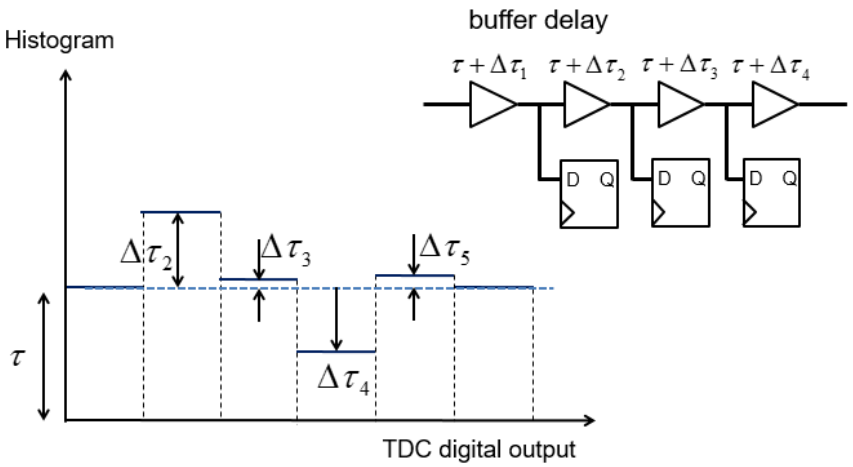


Fig. 4. Histogram and DNL in self-calibration

Figure 3 explains the principle of the self-calibration. In self-calibration mode, the histogram engine collects histogram data as DNL values, and obtains INL by accumulating the DNL values (Fig. 4). Then it calculates the inverse function of the INL values and stores them in memory. In normal operation mode, the encoder output is corrected by the inverse function of the INL values in memory, to obtain linear TDC input-output characteristics. The above self-calibration can be done using all-digital methods, and Fig.5 shows simulation result, while Fig. 6 shows TDC characteristics before and after calibration

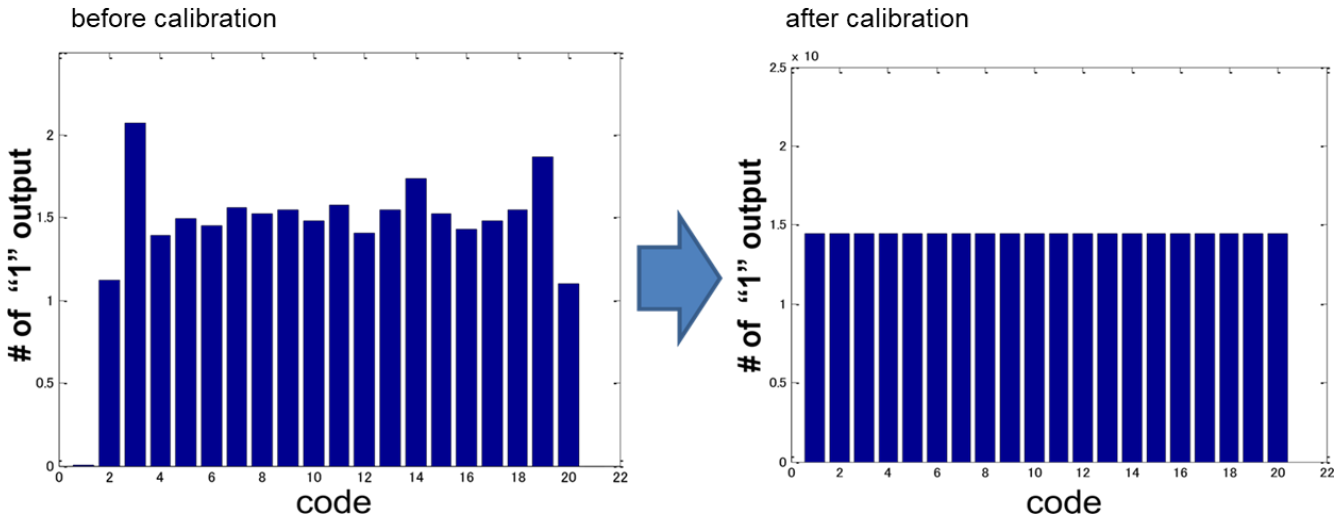


Fig.5 Simulation result of self-calibration. Histogram before calibration (left). Histogram after calibration (right).

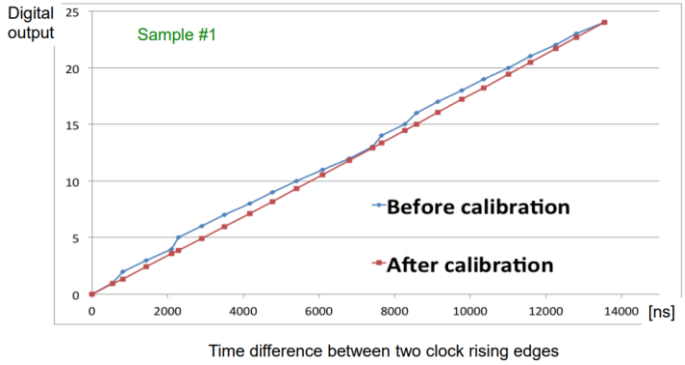


Fig. 6. TDC characteristics before and after calibration

4. Investigation of Efficient Linearity Self-Calibration Condition with Histogram Method for Time-to-Digital Converter

In order to carry out the self-calibration described in Section 3, all codes of the digital output (Dout) should output. It is inefficient if the signal is concentrated on only some codes of the digital output (Dout). In this research, we propose a method to evenly distribute the signal to all codes of the digital output (Dout). A simulation was performed for the TDC in Fig. 7 with N = 24-bit. The buffer delay variation ($\Delta\tau_i$) described in Section 3 is not mentioned in Section 4. During one START cycle, Dout is obtained only by the first STOP signal. Second and subsequent STOP signals do nothing. The number of non-working STOP signals are counted as "fail points". For example, in Fig. 7, there are two fail points.

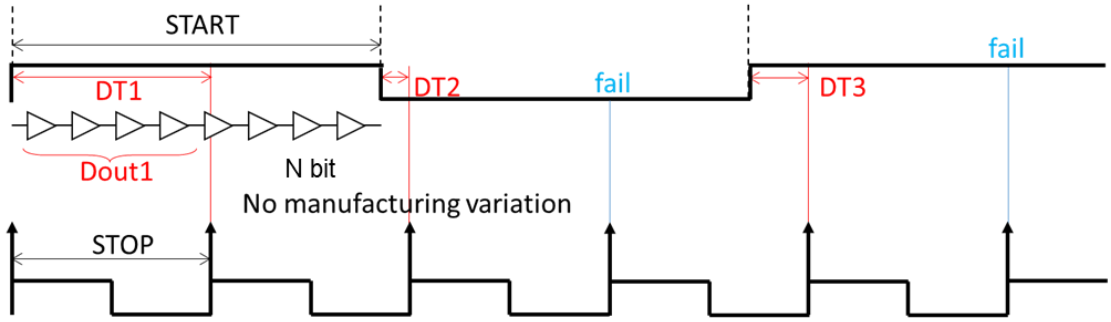
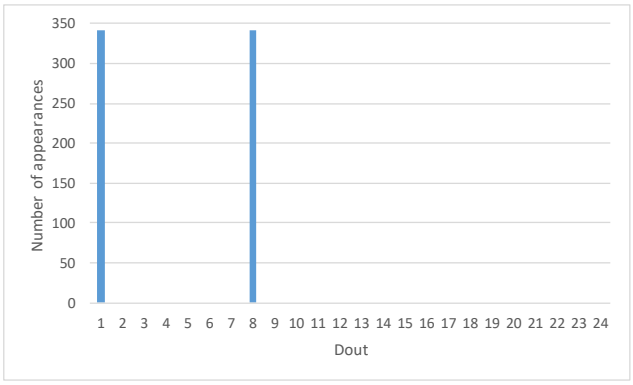
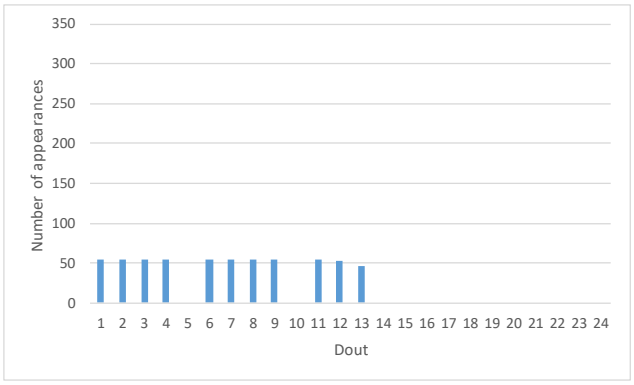


Fig. 7. Definition of simulation condition for our research here.

The START is fixed at 1.0, and the STOP is changed between 1.0 and 0.25. RATIO defined as START/STOP moves in the range of 1.0 to 4.0 in 0.1 increments. Figure 8 (a) shows an inefficient example with RATIO of 1.5. You can see that only Dout =1 and 8 output signal, and other Dout's don't output signal. Figure 8 (b) shows an efficient example with RATIO of 1.9. You can see that the histogram is distributed for many codes of Dout.



(a) An inefficient example (RATIO = 1.5).



(b) An efficient example (RATIO = 1.9).

Fig. 8. Histogram showing the frequency of occurrence of values in each Dout.

To compare the efficiencies quantitatively, RMS defined in Eq. (1) is used.

$$\mathrm{RMS} = \sqrt{\sum_i (Dout_i - ideal)^2} \tag{1}$$

For example, if N = 4bit (There are $Dout_1$, $Dout_2$, $Dout_3$, $Dout_4$) and the STOP signal is input 20 times, the $ideal$ becomes 5. The ideal histogram has $Dout_1 = Dout_2 = Dout_3 = Dout_4 = 5$ and RMS=0. Smaller RMS means better efficiency.

The fact that the RMS is small means that the sampled phase is uniform as well as random. The maximum number of the sampling points depends on whether the sampling clock and the input signal are synchronous. For example, suppose that an input signal clock period is 1.0 and the sampling clock period is 0.618 (hence they are synchronous), then the maximum number of the sampling points is 500[points] as 0.618 = 618/1000 = 309/500. After 500 times acquisition, you cannot obtain further data with new phases. In other words, the frequency ratio between the input signal and the sampling clock had to be an irrational number (in other words, both are asynchronous) for data acquisition with many phases.

Figure 9 shows RATIO vs RMS when the STOP signal is input 1024 times. If the START signal and STOP signal are synchronized, such as when RATIO is 1.0, 2.0, 3.0, 4.0, RMS is large.

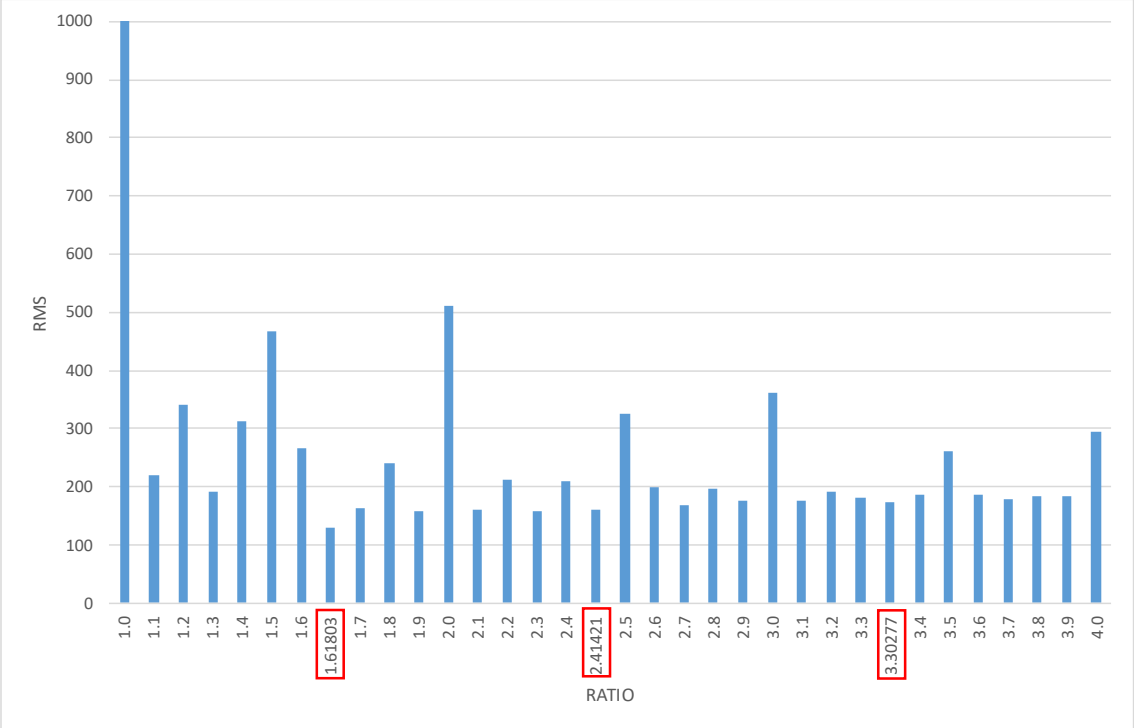


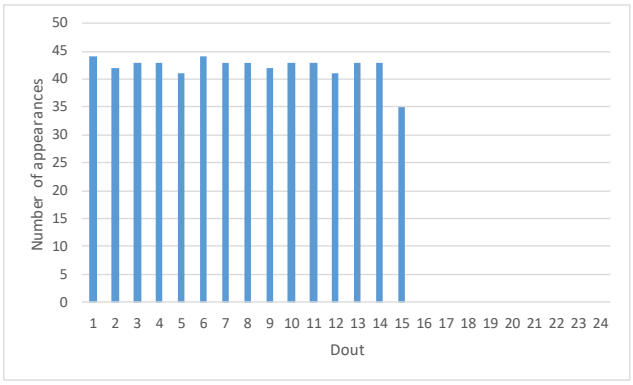
Fig. 9. RATIO vs RMS.

Here, we explain the case of "metallic ratio". The metallic ratio is expressed as follows:

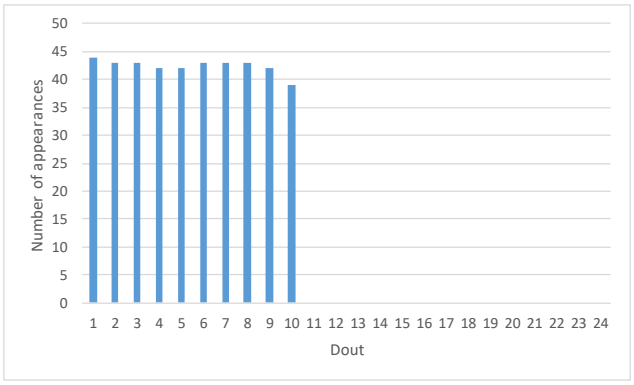
$$1 : \frac{n+\sqrt{n^2+4}}{2} \qquad (n\text{: natural number}) \tag{2}$$

It has special name when $n = 1,2,3$ that is, the golden ratio (1: 1.61803 ...) for n=1, the silver ratio (1: 2.41421 ...) for n=2, and the bronze ratio (1: 3.30277 ...) for n=3. Our research group is trying to use the metallic ratio for efficient circuit design [11]. In this study, we also investigate the TDC self-calibration efficiency when RATIO is the metallic ratio; they are shown in Fig. 9 and we see that when RATIO is the golden ratio, RMS is small.

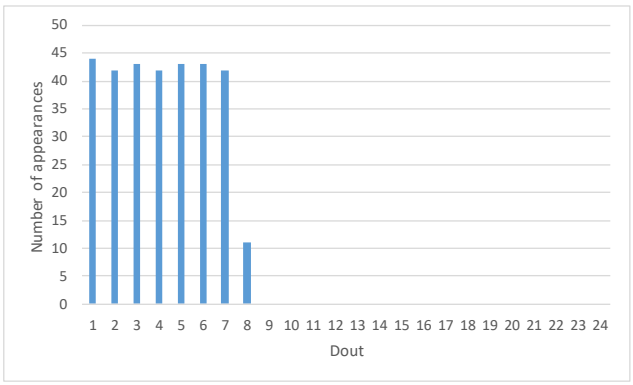
Figure 10 shows a histogram obtained by using the metallic ratio. In each case, the signal is output evenly to Dout. If the RATIO is large, signal is not able to output in large Dout. This is because the number of the fail points increases when the RATIO is large. The fact could be shown in the RATIO vs fail points graph shown in Fig. 13. Therefore, it can be said that the Golden Ratio is the most efficient under the conditions of this study.



(a). Golden ratio.



(b) Silver ratio.



(c) Bronze ratio.

Fig. 10. Histogram showing the frequency of occurrence of values in each Dout.

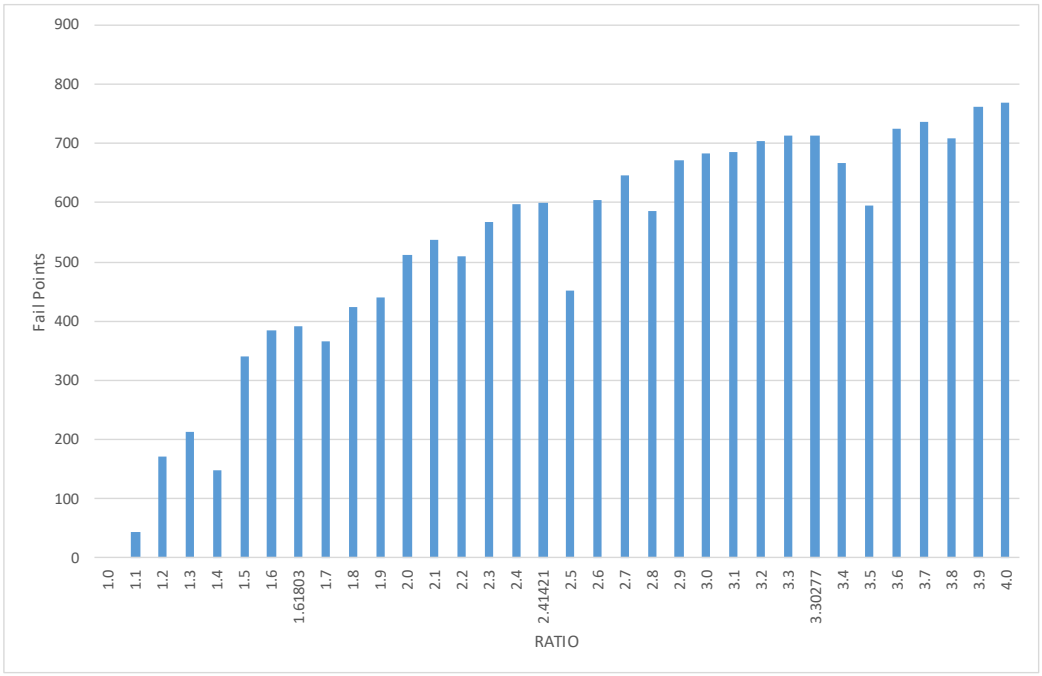


Fig. 11. RATIO vs fail points.

5. Summary and future challenge

In this paper we have investigated a linearity self-calibration method with a histogram method for a flash-type time-to-digital converter (TDC), inspired by the similarity of the golden ratio of two clock signal frequencies and measurement technologies as follows:

(i) ADC testing with histogram method: The histogram method with a sine wave input is widely used for ADC test. For its given sampling clock frequency, its input frequency can be chosen to obtain the histogram data efficiently with relatively small number of data.

(ii) Flash-type TDC self-calibration with histogram method: Non-linearity of a flash-type time-to-digital converter can be calibrated by applying two asynchronous clocks to two inputs and obtaining the histogram of its output data. If the ratio of their frequencies is related to the golden ratio, then the calibration may be performed effectively.

(iii) Integral-type TDC Converter: A high performance integral-type time-to-digital converter [10] which uses two clocks can be realized if their frequency ratio is the golden-ratio. Two repetitive signals with different frequencies are used, and one of its repetitive frequency should be known so that the other frequency should be adjusted controlled.

This paper presents the case of (ii) with simulation.

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