Advanced Data Converter Session

22 Oct. 2020
14:15-14:30

Nonlinearity Analysis of Resistive Ladder-Based Current-Steering Digital-to-Analog Converter

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Outline

- Background & Objective
- Architecture of *N*-ary DAC
  - Ternary-Ladder DAC
  - Quaternary-Ladder DAC
- DNL Simulation Results
  - σ_{DNL} of Some Ladder-based DACs
- Conclusion

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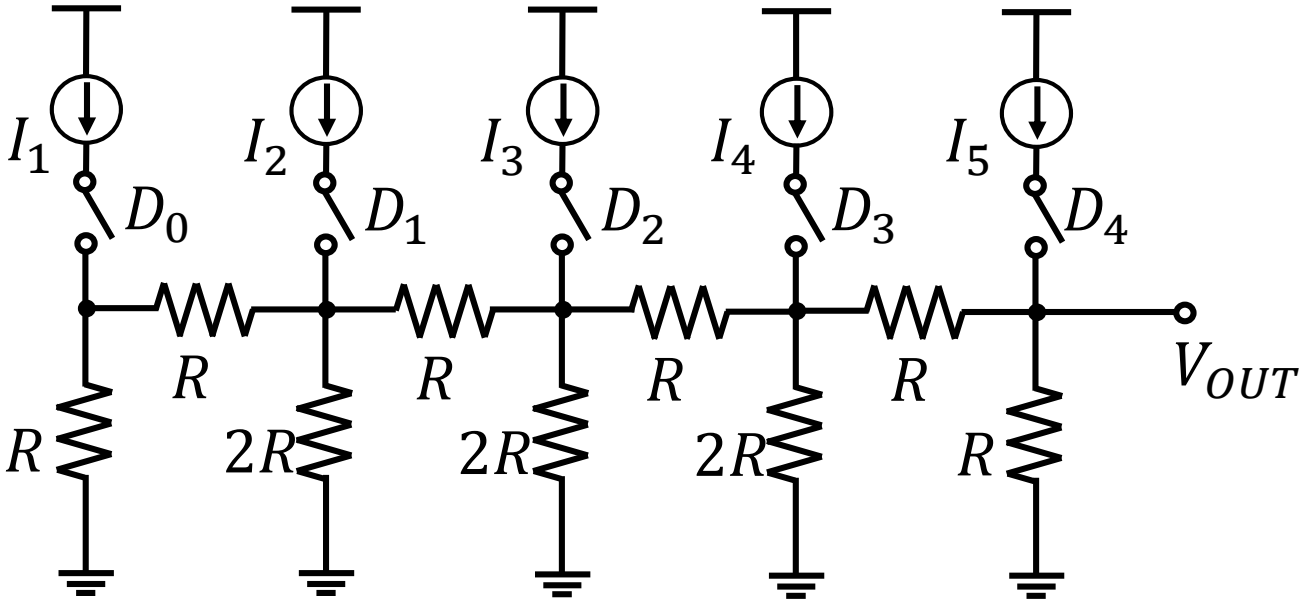
Background

- **R-2R current-steering DAC**



High-speed

Simple architecture, No need for decoder

Background & Objective

- **R-2R current-steering DAC**
  - **But, the linearity deteriorates with a clear pattern on the input code**

Cause

Mismatches { **among current sources** / **among resistors**

- **Our previous investigation**
  - **DAC with *N*-ary Resistive Ladder**

Clarify DNL tendencies for *N*-ary Ladder

- **To Develop efficient calibration and testing methods**

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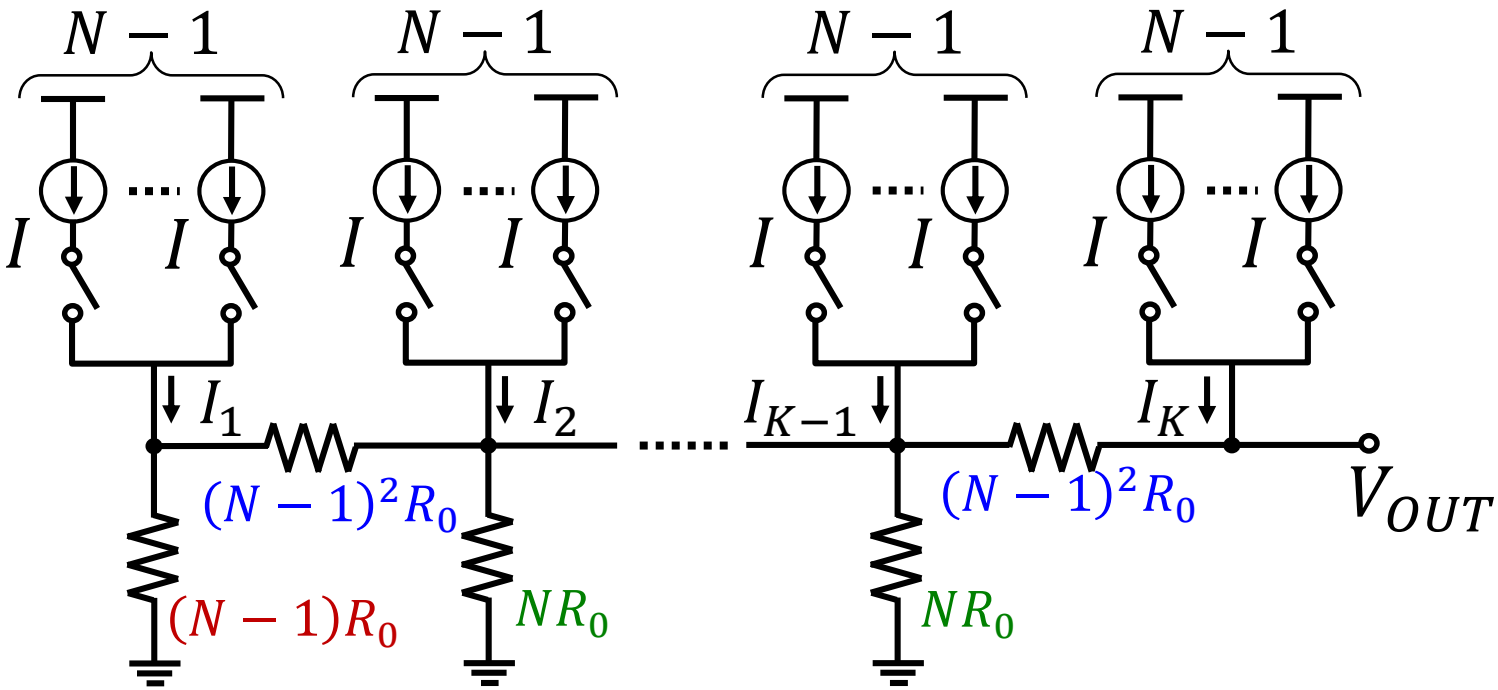
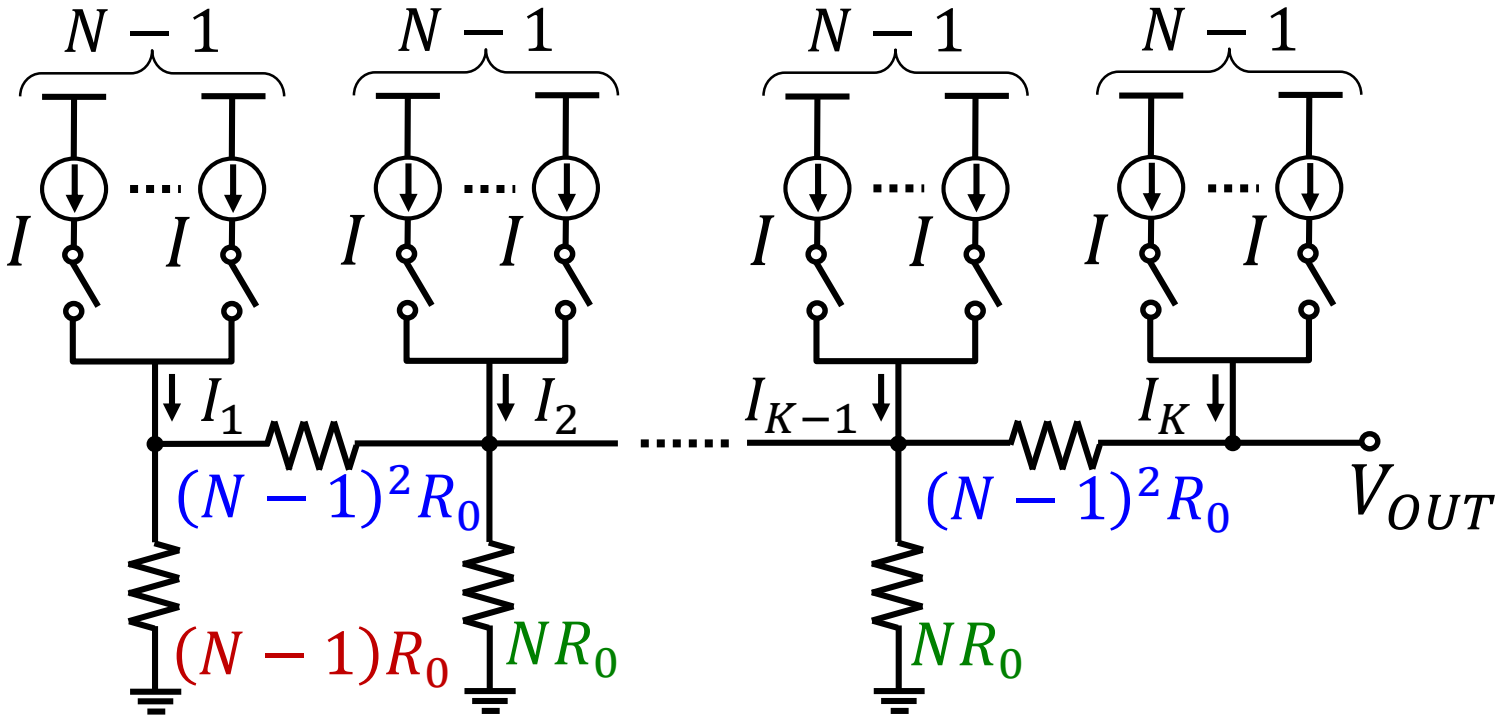
[3] M. Hirai, S. Yamamoto, H. Arai, A. Kuwana, H. Tanimoto, Y. Gendai, H. Kobayashi, "Systematic Construction of Resistor Ladder Network for N-ary DACs", IEEE ASICON (Oct. 2019)

Architecture of *N*-ary DAC

- ***N*-ary DAC**
  - **Generalized resistive-ladder based DAC**
  - **Current division ratio is different from R-2R**



Architecture of *N*-ary DAC



N **: Current division ratio,**
I**$_1$,⋯,** ***I*****$_K$: Injected currents,**
R**$_0$: Unit resistance**

K : Stage number
I **: Unit current**

Theoretical output voltage

- **Output voltage**

$$V_{OUT}(I_1, \cdots, I_K, R_0, N, K) = R_0 \cdot N(N-1) \sum_{k=1}^{K} \left(\frac{I_k}{N^{K-k}} \right)$$

- **Output voltage steps ⇒** $N^K - 1$
- **When *N* = 2**

  ⇒ K-bit, R-2R current-steering DAC

Notation

N **: Current division ratio,**	**K : Stage number**
$I_1, \cdots, I_K$ **: Injected currents,**	***I*** **: Unit current**
R_0 **: Unit resistance**	

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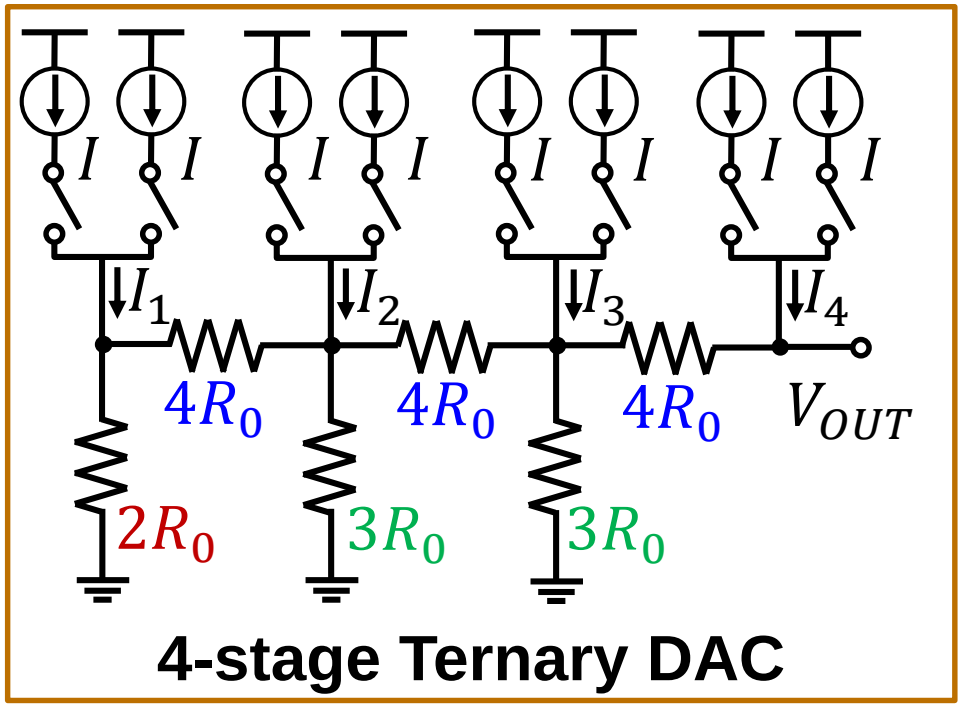
N = 3, Ternary-Ladder DAC

- **Resistance ratio**
  $4R_0 : 3R_0 : 2R_0$
- **Voltage steps**
  $N^K - 1$
  $= 3^4 - 1 = 80$ steps



4-stage Ternary DAC

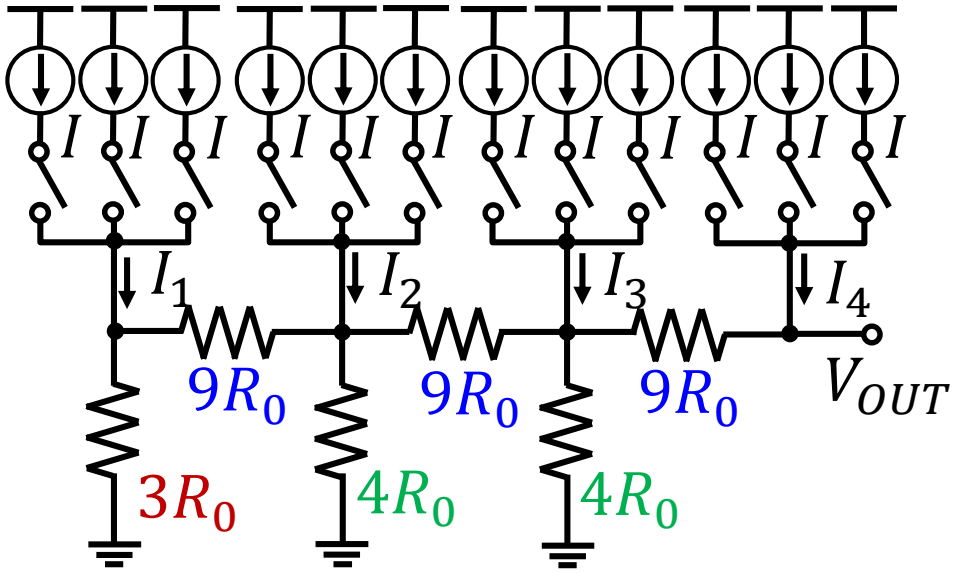
- **Output voltage**

$$V_{OUT}(I_1, I_2, I_3, I_4, R_0) = R_0 \cdot 6\left(I_4 + \frac{1}{3^1} I_3 + \frac{1}{3^2} I_2 + \frac{1}{3^3} I_1\right)$$

Each $I_k \rightarrow$ ternary weighted.

N = 4, Quaternary-Ladder DAC

- **Resistance ratio**
  $9R_0 : 4R_0 : 3R_0$
- **Voltage steps**
  $N^K - 1 = 4^4 - 1$
  $= 255$ steps



4-stage Quaternary DAC

- **Output voltage**

$$V_{OUT}(I_1, I_2, I_3, I_4, R_0) = R_0 \cdot 12\left(I_4 + \frac{1}{4^1} I_3 + \frac{1}{4^2} I_2 + \frac{1}{4^3} I_1\right)$$

Each $I_k \rightarrow$ quaternary weighted.

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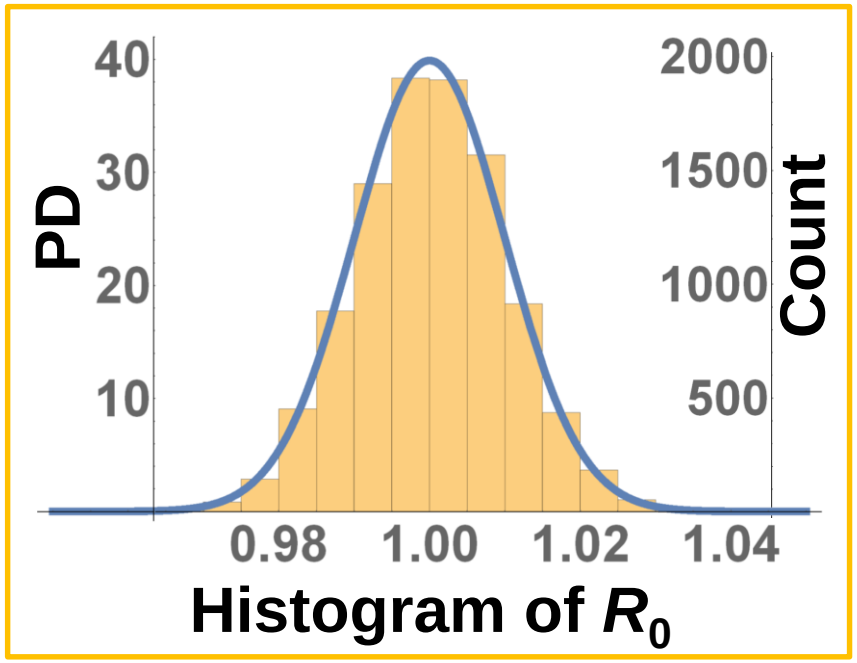
Monte-Carlo Simulation

- **Definition of Differential nonlinearity (DNL)**

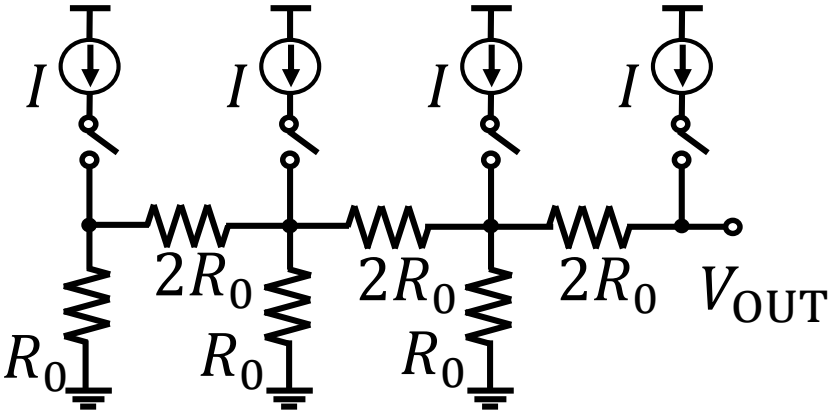
$$DNL(i) = \frac{V_{OUT}(i) - V_{OUT}(i-1)}{V_{LSB}} - 1$$

V_{LSB} : Ideal step size

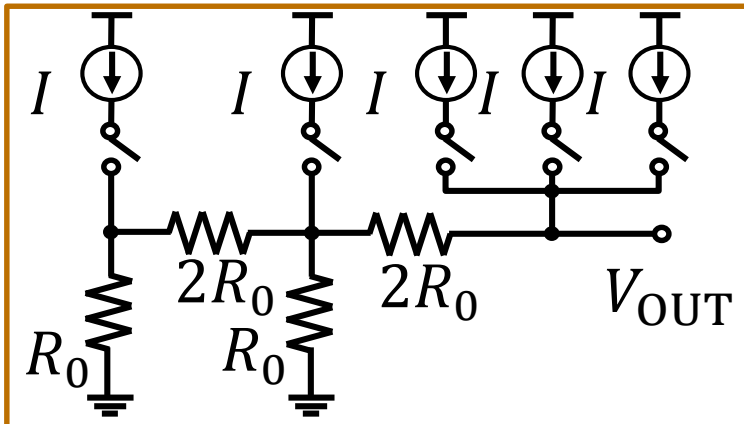
- **Simulation conditions**
  - **10,000 simulations**
  - **Random errors follow the normal distribution**
  - σ = 0.01 of R_0 and I



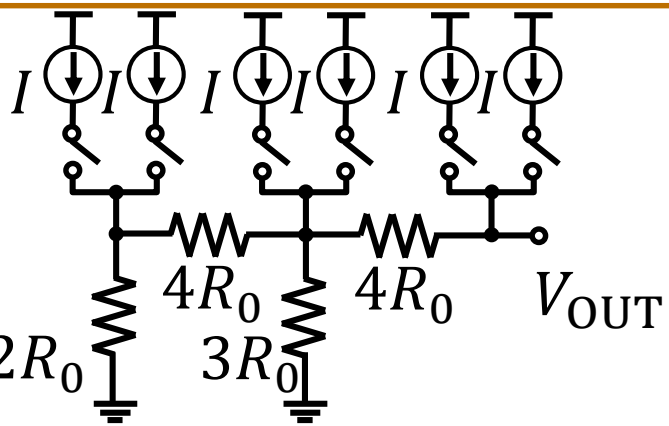
Simulated Circuits



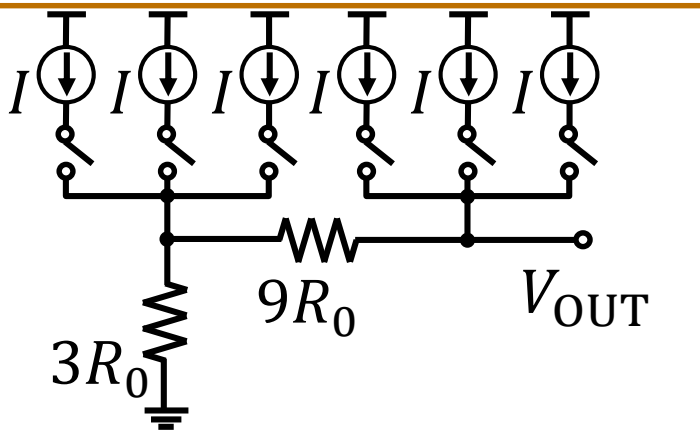
4-bit R-2R DAC



4-bit segmented DAC



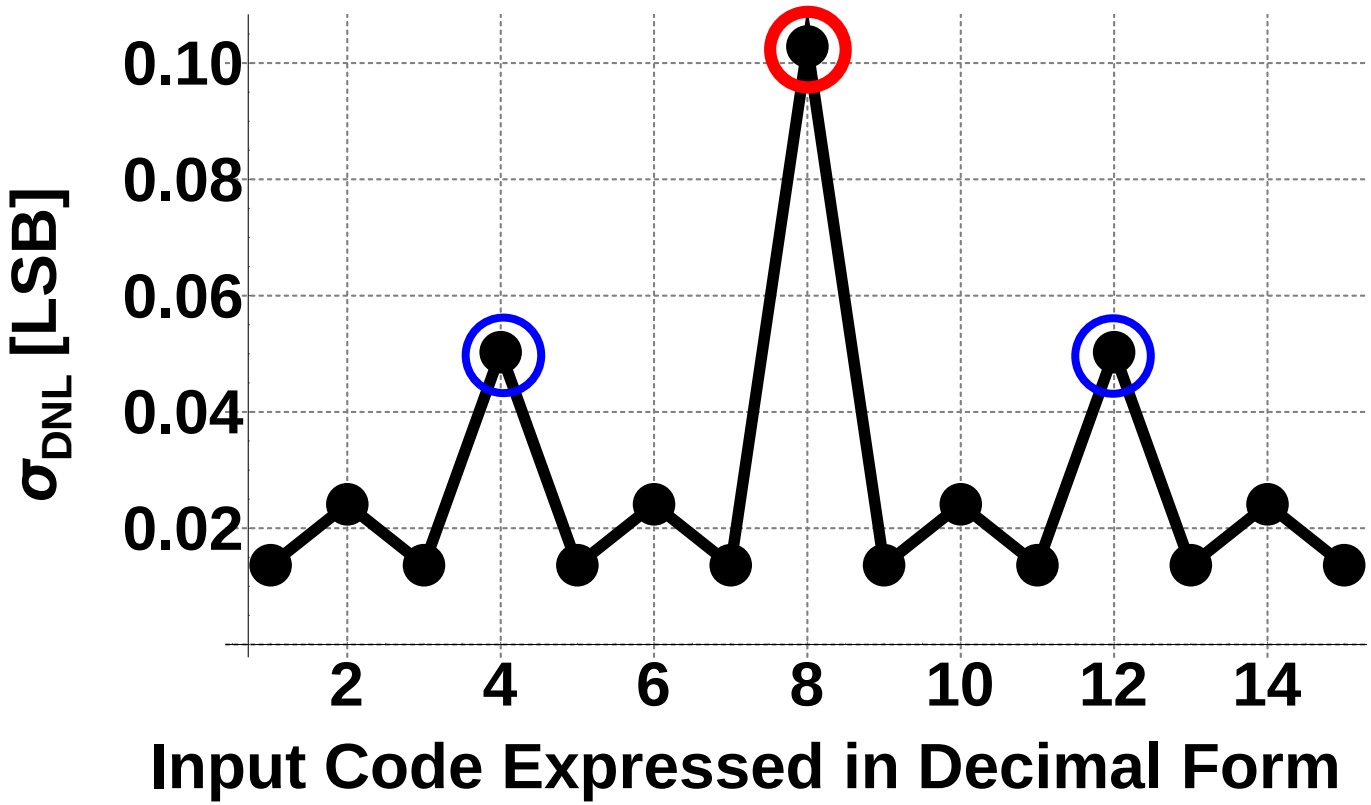
3-stage ternary DAC



2-stage quaternary DAC

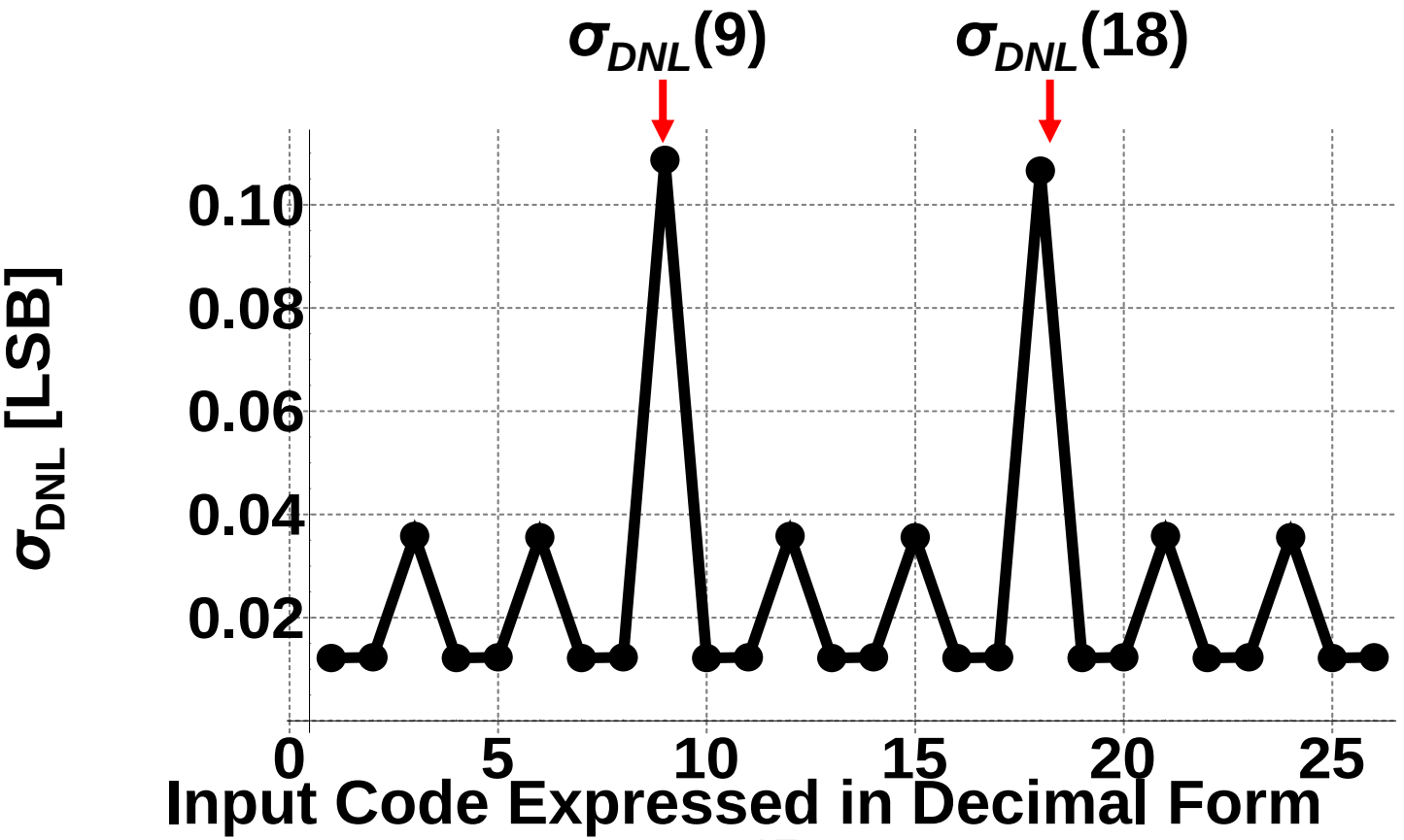
Result of 4-bit R-2R DAC

- σ_{DNL} becomes the largest at the MSB transition, the 2nd largest at the 2nd-MSB transition



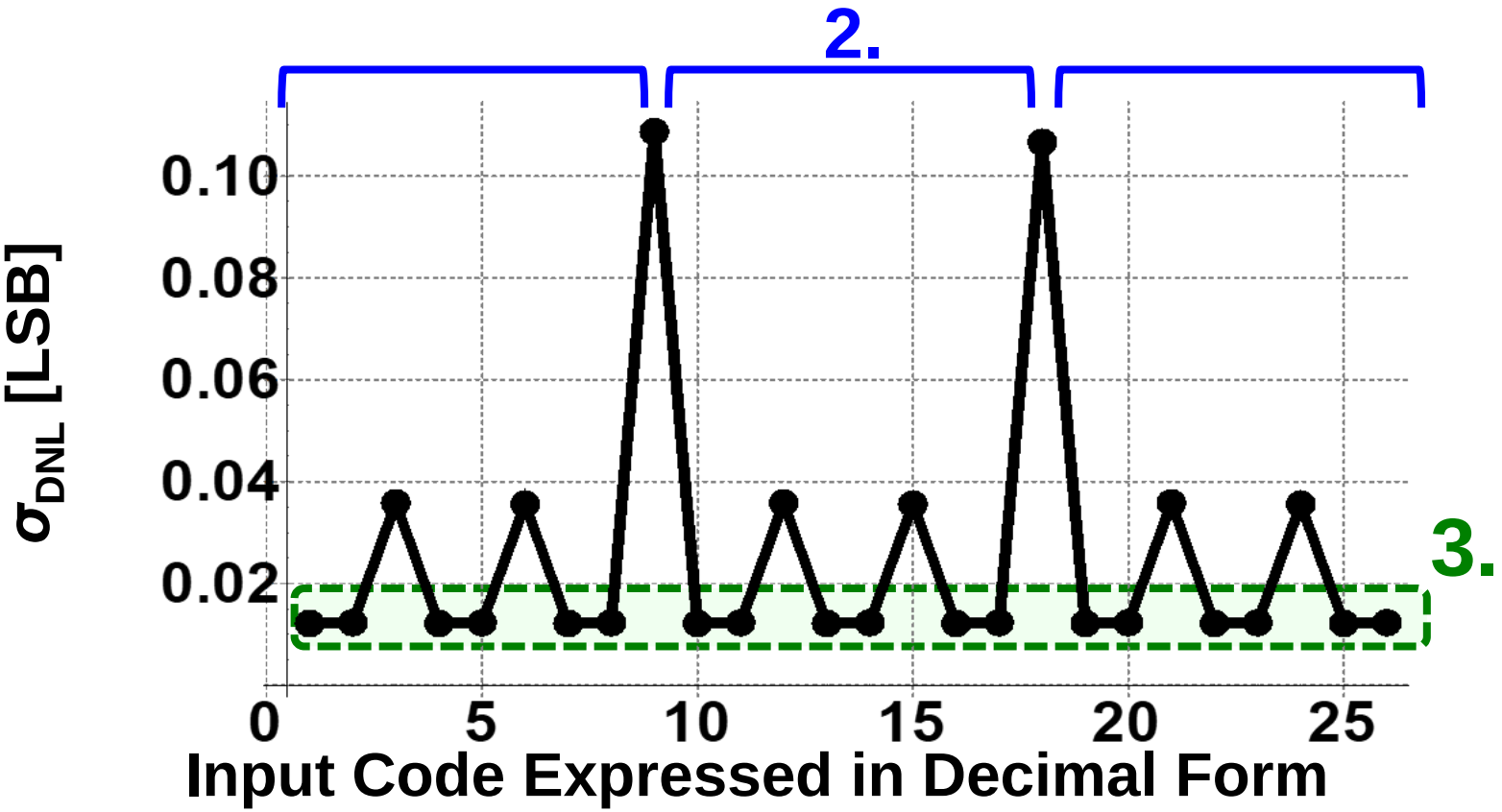
Result of 3-stage Ternary DAC

1. σ_{DNL} becomes the largest at 9 and 18, 1/3 and 2/3 of the input range



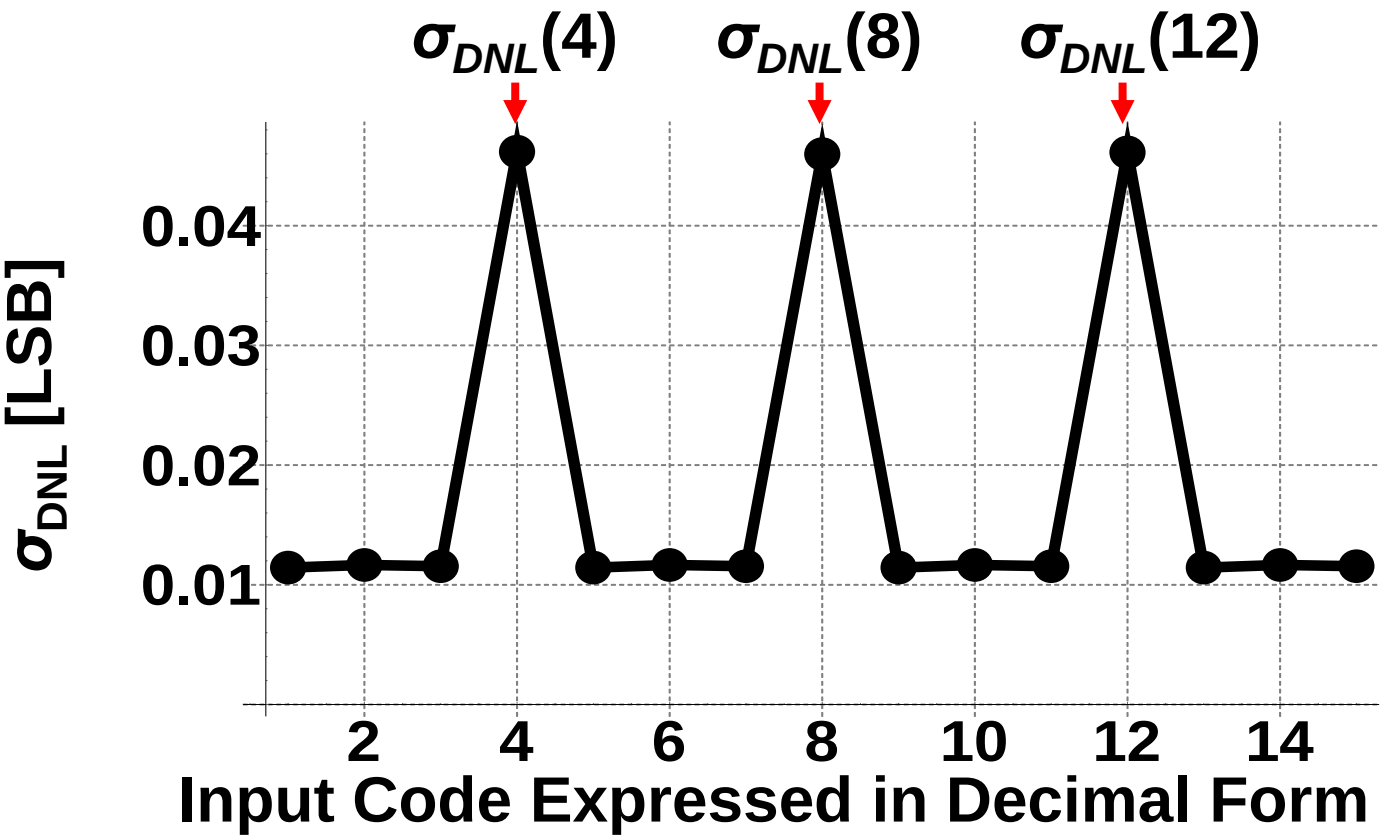
Result of 3-stage Ternary DAC

2. Similar tendencies in divided ranges
3. Minimum σ_{DNL}'s appear at two consecutive codes.



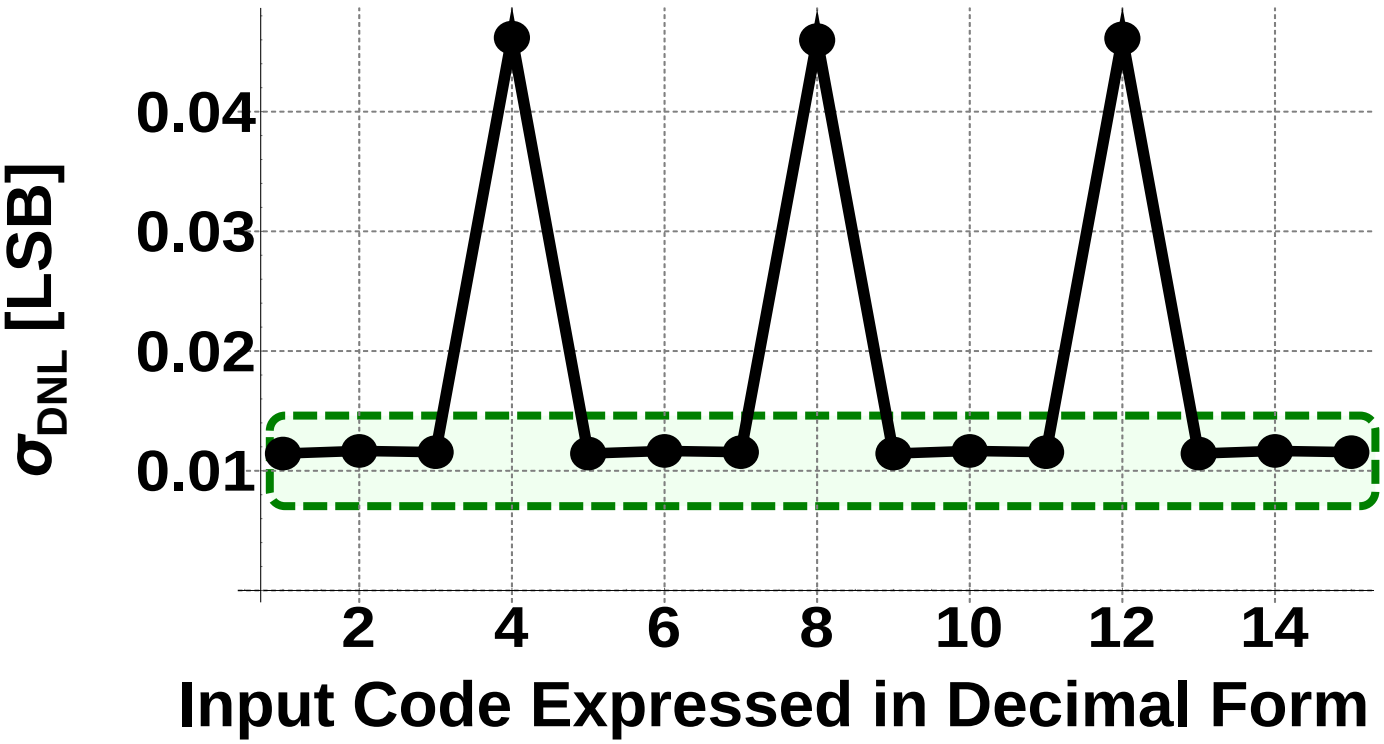
Result of 2-stage Quaternary DAC

1. σ_{DNL} becomes the largest at 4, 8 and 12.
   1/4, 1/2 and 3/4 of input range



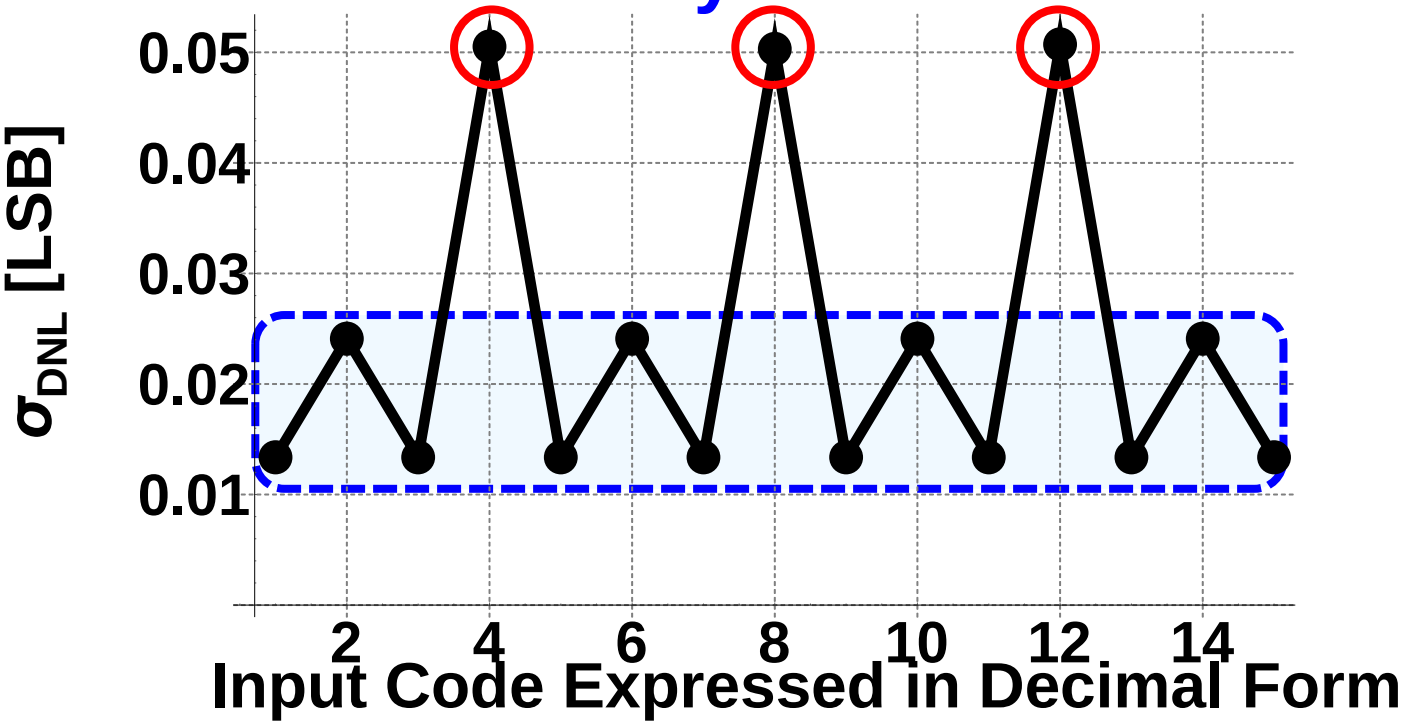
Result of 2-stage Quaternary DAC

2. Minimum σ_{DNL}'s appear at three consecutive codes.



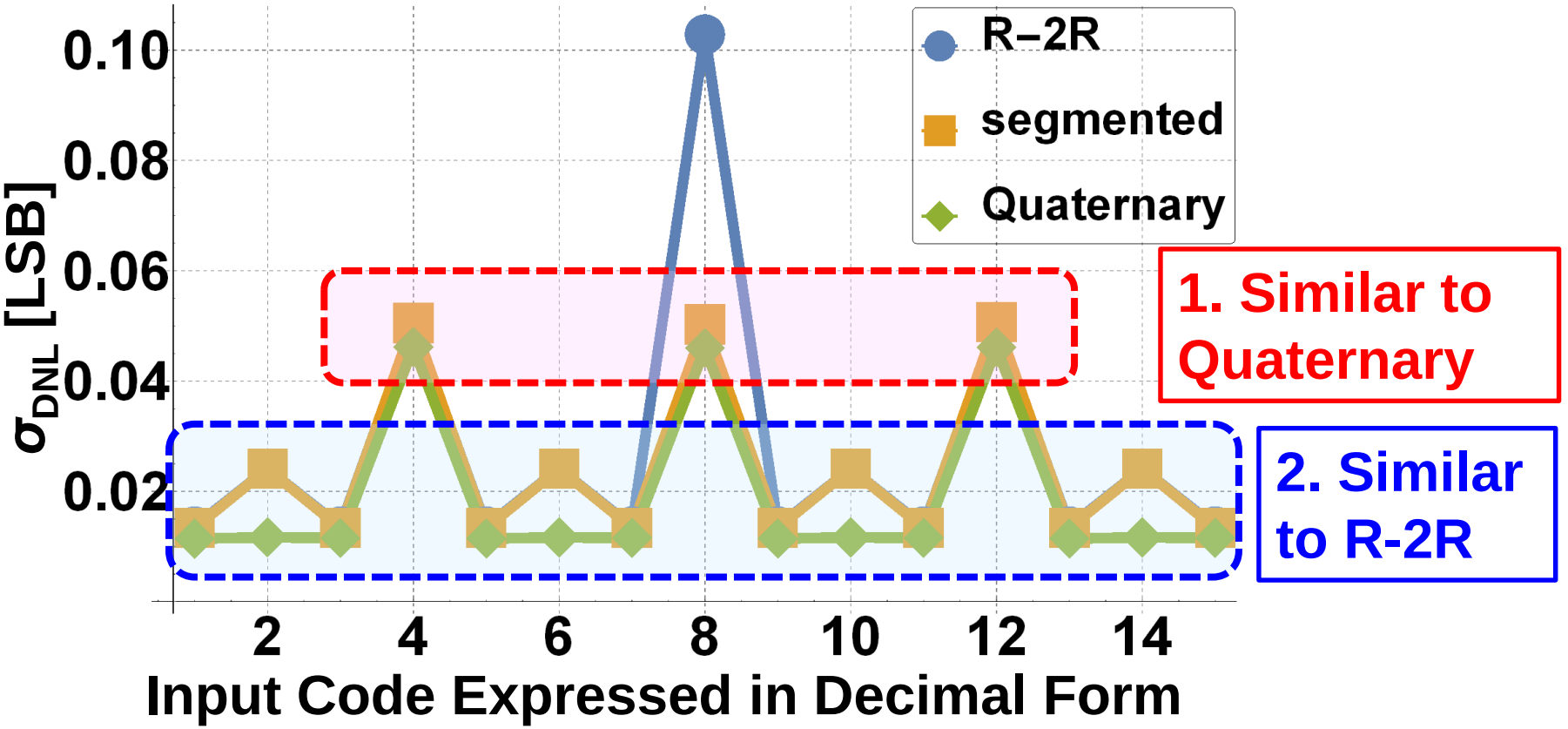
4-bit Segmented DAC

1. At 4, 8 and 12
   ⇒ similar tendency to quaternary DAC
2. The others
   ⇒ similar tendency to R-2R DAC



Comparison of σ_{DNL}'s

- Compare the result of
  R-2R, segmented DAC and Quaternary DAC



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Conclusion

- **We have shown the DNL tendencies for some types of resistor ladder-based DAC**
  - **Due to mismatches of current sources and resistors**
- **σ_{DNL} becomes the largest at specific input codes, which depend on the DAC structure.**
  - **By focusing on the code, these results would be useful to develop self-calibration techniques and production testing methods**