Charge-Domain Folding Analog-to-Digital Converter
電荷モード折り返しAD変換器

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OUTLINE

• Research Background and Objective
• Conventional High-Speed ADCs
  - Flash ADC
  - Current-Domain Folding ADC
• Proposed Charge-Domain Folding ADC
• Conclusions
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• Conventional High-Speed ADCs
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Research Background

Importance of ADC / DAC

- Rapid development of digital electronics technology
- A natural signal is analog
Objective:
Development of CMOS fast and small circuit ADC architecture.

Our Approach:
Folding ADC architecture
+ CMOS nonlinear switched capacitor circuit
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3-bit Flash ADC Configuration

Comparator array

Binary digital output

Truth table of digital encoder

<table>
<thead>
<tr>
<th>d7 d6 d5 d4 d3 d2 d1 d0</th>
<th>o2 o1 o0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 0 0 0 0</td>
<td>0 0 0</td>
</tr>
<tr>
<td>0 0 0 0 0 0 1 0</td>
<td>0 0 1</td>
</tr>
<tr>
<td>0 0 0 0 0 1 0 0</td>
<td>0 1 0</td>
</tr>
<tr>
<td>0 0 0 0 1 0 0 0</td>
<td>0 1 1</td>
</tr>
<tr>
<td>0 0 0 1 0 0 0 0</td>
<td>1 0 0</td>
</tr>
<tr>
<td>0 0 1 0 0 0 0 0</td>
<td>1 0 1</td>
</tr>
<tr>
<td>0 1 0 0 0 0 0 0</td>
<td>1 1 0</td>
</tr>
<tr>
<td>1 0 0 0 0 0 0 0</td>
<td>1 1 1</td>
</tr>
</tbody>
</table>

Analog input

Vin = 3.56 V
In case $V_{in} = 4.5\, V$
3-bit Flash ADC Operation

In case $V_{in} = 4.5$ V

Redundant

Working effectively

Redundant
Features of Flash ADC

- Fastest ADC
- Large hardware

N-bit Flash ADC
\[ \Rightarrow 2^N - 1 \] comparators

3-bit (N=3) case
\[ \Rightarrow 7 \] comparators

- In actual implementation, N is limited up-to 8.
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Features of Folding ADC

- Fastest ADC
- Usage of analog encoding circuit
  \[ \Rightarrow \text{Remove “redundancy of flash ADC”} \]
- Small hardware

N-bit folding ADC
  \[ \Rightarrow N \text{ comparators} \]

3-bit (N=3) case
  \[ \Rightarrow 3 \text{ comparators} \]
Gray Code

- Frank Gray at Bell Lab invented **Gray code** in 1947.
- Robust code compared to binary code.
- Often used in ADC.
## Binary Code versus Gray Code

<table>
<thead>
<tr>
<th>Decimal numbers</th>
<th>Binary Code</th>
<th>Gray Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>1</td>
<td>0001</td>
<td>0001</td>
</tr>
<tr>
<td>2</td>
<td>0010</td>
<td>0011</td>
</tr>
<tr>
<td>3</td>
<td>0011</td>
<td>0010</td>
</tr>
<tr>
<td>4</td>
<td>0100</td>
<td>0110</td>
</tr>
<tr>
<td>5</td>
<td>0101</td>
<td>0111</td>
</tr>
<tr>
<td>6</td>
<td>0110</td>
<td>0101</td>
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<tr>
<td>7</td>
<td>0111</td>
<td>0100</td>
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<tr>
<td>14</td>
<td>1110</td>
<td>1001</td>
</tr>
<tr>
<td>15</td>
<td>1111</td>
<td>1000</td>
</tr>
</tbody>
</table>
Gray Code Output ADC

Gray code output with respect to analog input $V_{in}$

G3

G2

G1

G0

Analog input $V_{in}$
Current-Mode Analog Encoder for G3, G2

SPICE simulation result

Analog input Vin
Current-Mode Analog Encoder for G3, G2

Vin

Only one comparator for each G3, G2

G3

Vin

G2

Vin
Current-Mode Analog Encoder for G1

SPICE simulation result

Analog input Vin
Current-Mode Analog Encoder for G1

Analog encoder

Only one comparator for G1

Vin
Current-Mode Analog Encoder for G1

Gray code analog encoder

⇒ Cross-coupling of NMOS pairs
Features of Analog Encoder

Current-mode analog encoder

● Effective for hardware reduction

● Suitable for bipolar circuit, thanks to its high current drivability

● Not suitable for CMOS circuit (operation is slow) due to its low current drivability
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Consideration of CMOS Folding ADC

● CMOS circuit advantages
  - MOS switch usage
  - Preamplifier saturation characteristics usage

● Nonlinear switched capacitor folding circuit with CMOS

● Avoid CMOS low current drivability
Charge-Domain Folding ADC
Operation of Charge-Domain Folding ADC for G3

SPICE simulation result
Operation of Charge-Domain Folding ADC for G2

**Phase 1**
- Preamplifier
- Comparator

**Phase 2**
- Preamplifier
- Comparator

SPICE simulation result

Analog input $V_{in}$
Operation of Charge-Domain Folding ADC for G1

**Phase 1**
- Vin
- Preamplifier
- Comparator
- G1
- $V_{clk'}$
- $V_{dd}$
- Gnd
- $1/8V_r$
- $3/8V_r$
- $5/8V_r$
- $7/8V_r$

**Phase 2**
- Vin
- Preamplifier
- Comparator
- G1
- $V_{clk'}$
- $V_{dd}$
- Gnd
- $1/8V_r$
- $3/8V_r$
- $5/8V_r$
- $7/8V_r$
Operation of Charge-Domain Folding ADC for G1

Vin

preamplifier

comparator

G1

SPICE simulation result

Analog input Vin
Preamplifier Circuit

Designed preamplifier circuit

SPICE simulation results

Vin+ - Vin-

Vout+ - Vout-

Analog input Vin+ - Vin-
Preamplifier Circuit

Designed preamplifier circuit

SPICE simulation results

Use saturation (nonlinearity) for charge-domain folding circuit
Preamplifier Circuit Gain vs Parameters (1)

Gain

Gain

\[(W/L) \text{ N} \]
Preamplifier Circuit Gain vs Parameters (2)

Gain vs (W/L) for p1 and p2 parameters.

- For p1, gain increases as (W/L) increases from 5/1 to 20/1.
- For p2, gain decreases as (W/L) increases from 1/20 to 1/160.

Diagram shows the circuit with indicated (W/L) p1 and (W/L) p2 parameters.
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Charge-domain folding ADC is proposed.

- Significant hardware reduction
- Suitable for CMOS implementation
  ⇒ Usage of MOS switch & capacitor
- Basic circuit topology, operation and SPICE simulation results are shown.
- Detailed performance evaluation is next work.
Thank you for listening

Folding Circuit

七転八起
• Question:
  Why the proposed charge-domain folding ADC is faster?

• Answer:
  It’s realization with the charge mode (switched capacitor method) is examined, and only one comparator is used for 1-bit to remove redundant operations. So it will be faster.