Charge-Domain Folding Analog-to-Digital Converter

電荷モード折り返しAD変換器

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OUTLINE

- Research Background and Objective
- Conventional High-Speed ADCs
  - Flash ADC
  - Current-Domain Folding ADC
- Proposed Charge-Domain Folding ADC
- Conclusions

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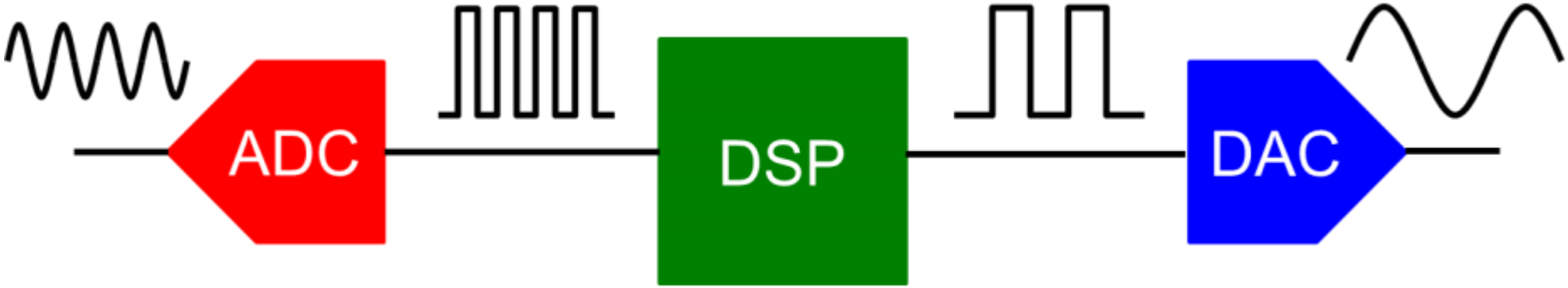
Research Background

Importance of ADC / DAC

- Rapid development of digital electronics technology
- A natural signal is analog



Research Objective

Objective:

Development of CMOS fast and small circuit ADC architecture.

Our Approach:

Folding ADC architecture

+

CMOS nonlinear switched capacitor circuit

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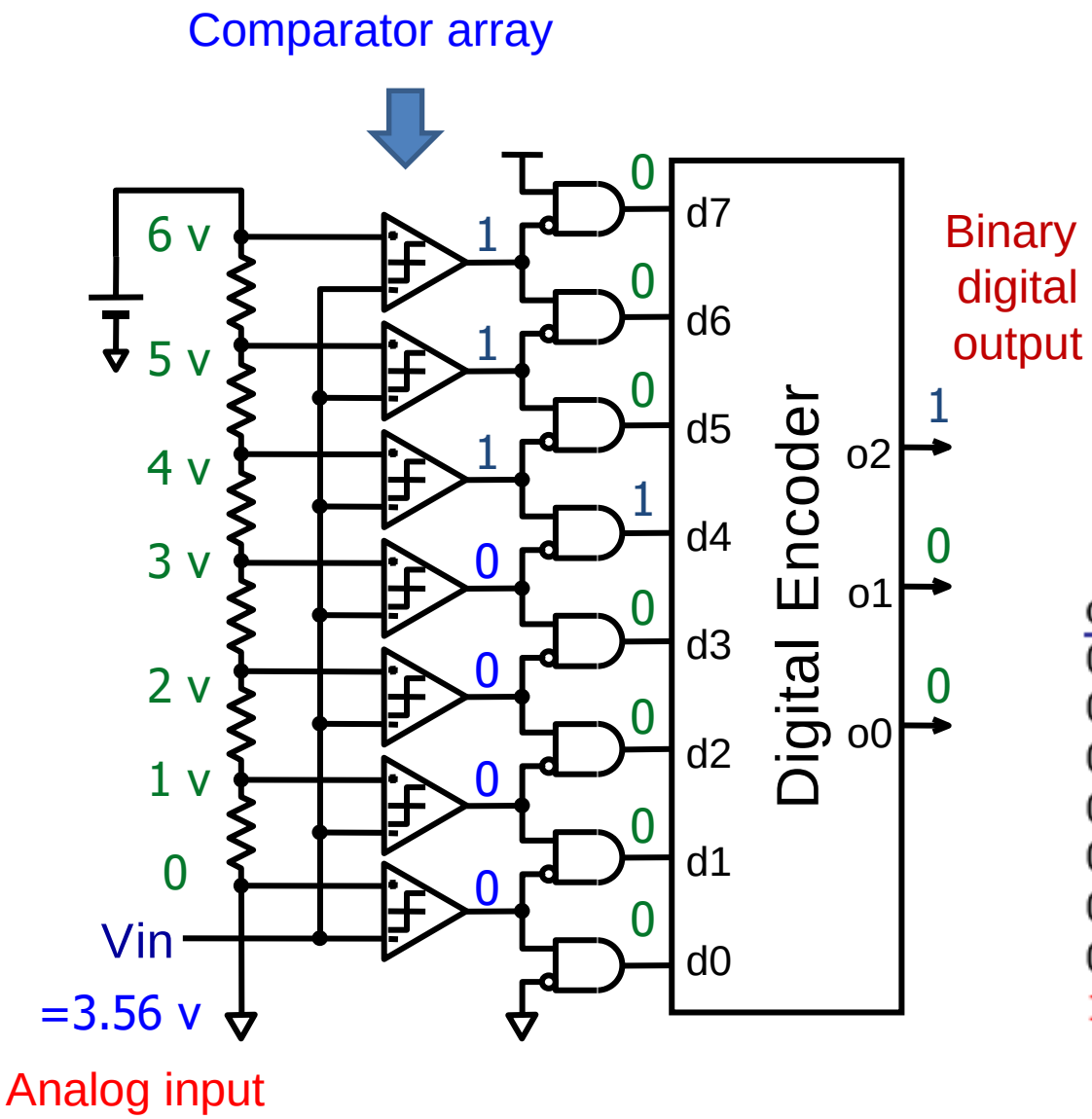
3-bit Flash ADC Configuration

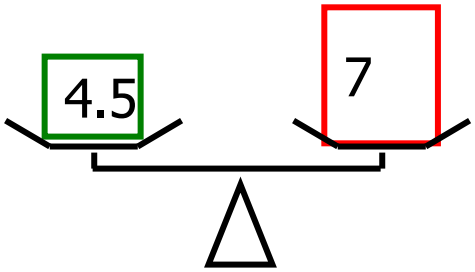


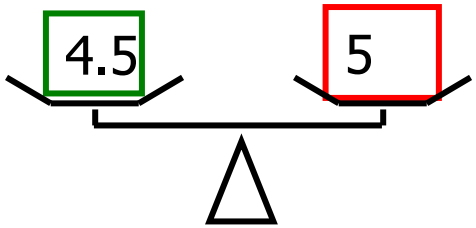
Truth table of digital encoder

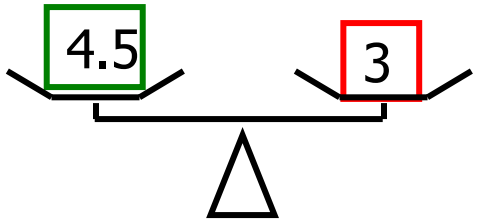
d7	d6	d5	d4	d3	d2	d1	d0	o2	o1	o0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

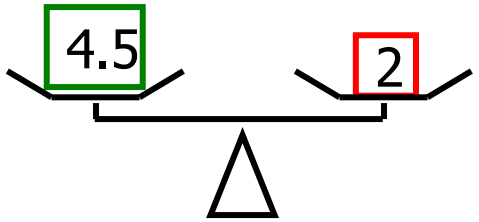
3-bit Flash ADC Operation

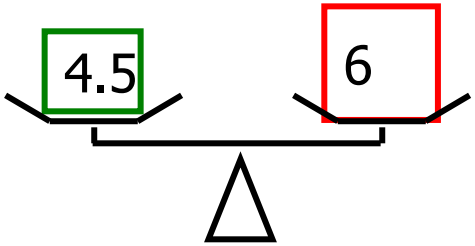
In case Vin =4.5 V

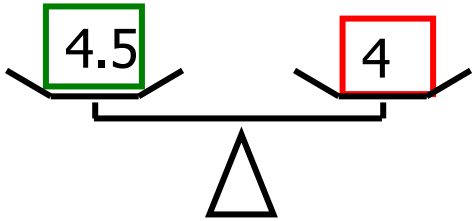


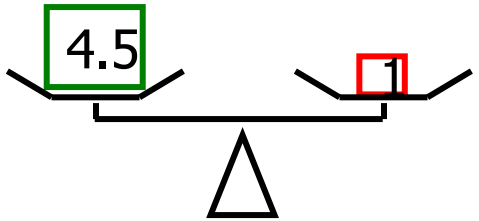






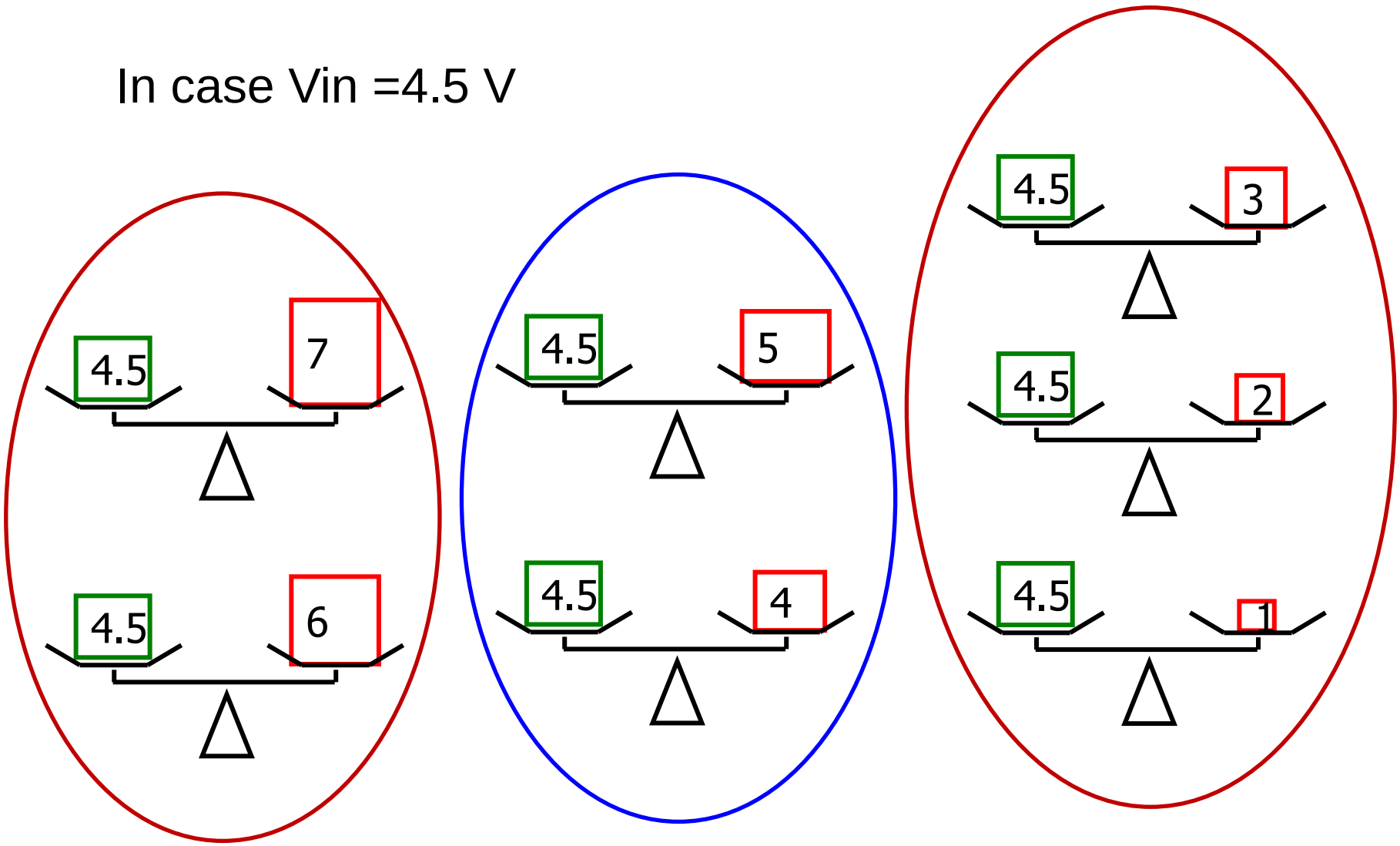






3-bit Flash ADC Operation

In case Vin =4.5 V



Redundant

Working effectively

Redundant

Features of Flash ADC

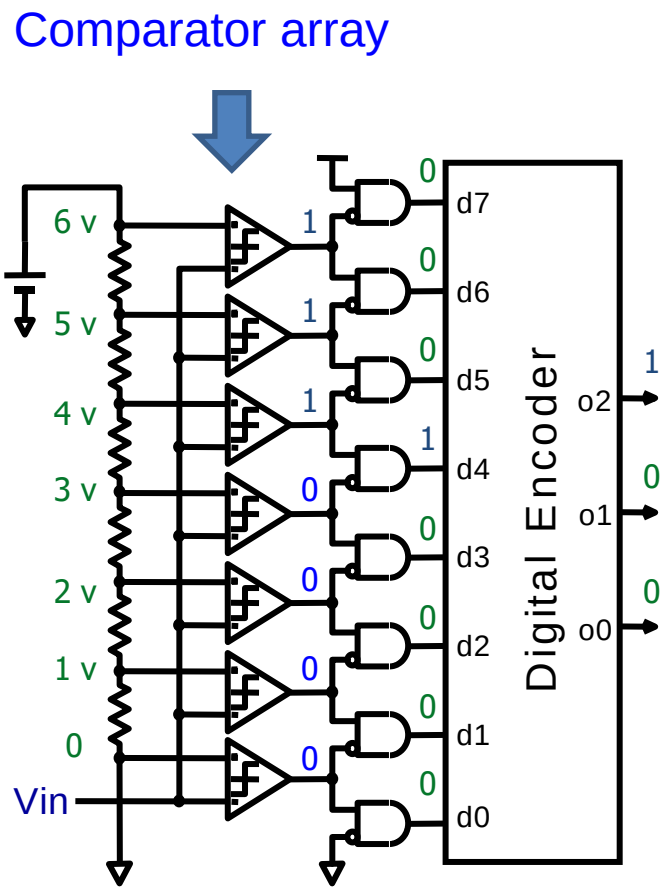
- Fastest ADC
- Large hardware

  N-bit Flash ADC

  ⇒ 2^N-1 comparators

  3-bit (N=3) case

  ⇒ 7 comparators



- In actual implementation, N is limited up-to 8.

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Features of Folding ADC

- Fastest ADC
- Usage of analog encoding circuit

  ⇒ Remove “redundancy of flash ADC”

- Small hardware

  N-bit folding ADC

  ⇒ N comparators

  3-bit (N=3) case

  ⇒ 3 comparators

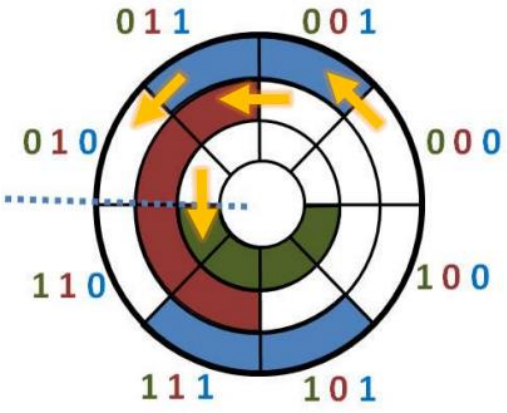
Gray Code

- Frank Gray at Bell Lab invented Gray code in 1947.

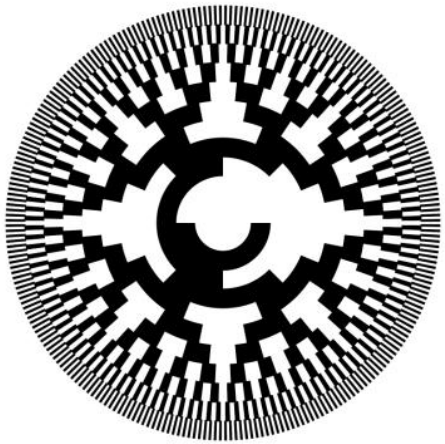
- Robust code compared to binary code.

- Often used in ADC.

FRANK GRAY and A. L. Johnsrud in television booth. Behind the glass panels at sides and top are the photo-electric cells.



$Q_2Q_1Q_0$
000
001
011
010
110
111
101
100



グレイコード：前後に隣接する符号間のハミング距離が必ず1

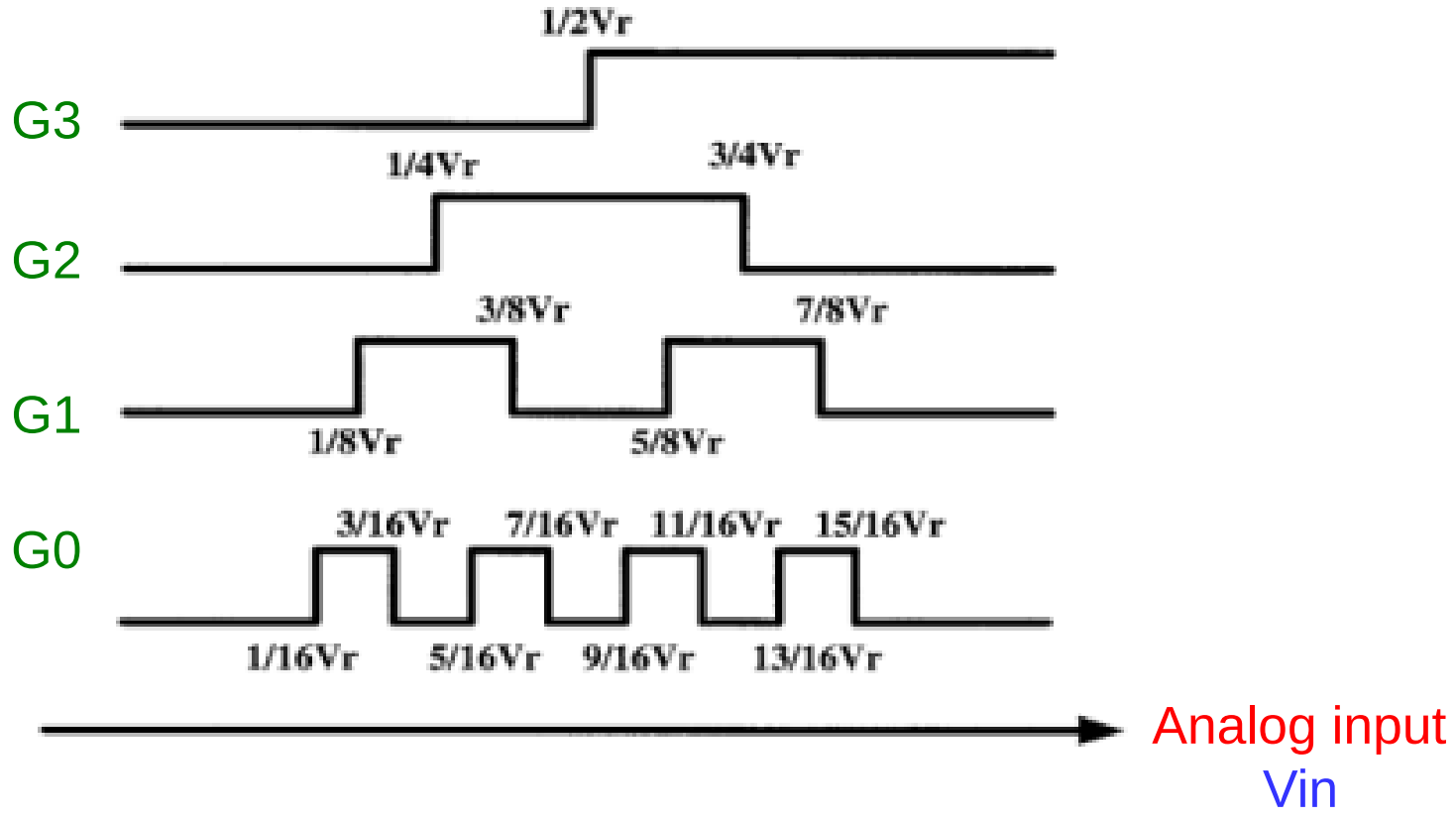
ベル研究所のフランク・グレイが1947年の特許出願書で最初に使用した。

Binary Code versus Gray Code

Decimal numbers	Binary Code	Gray Code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

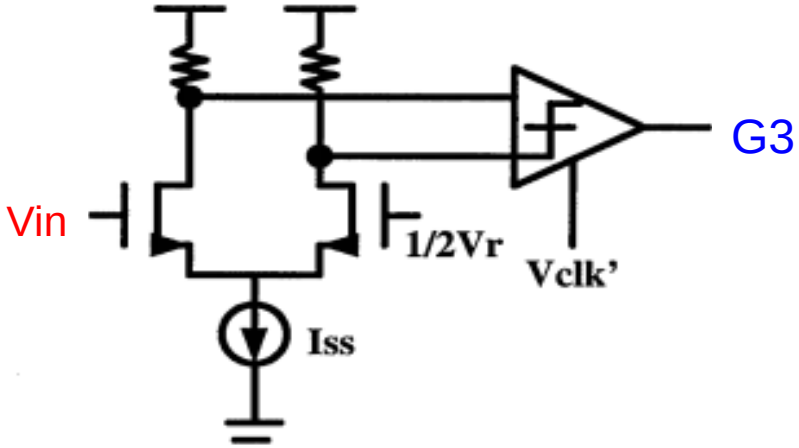
Gray Code Output ADC

Gray code output with respect to analog input Vin

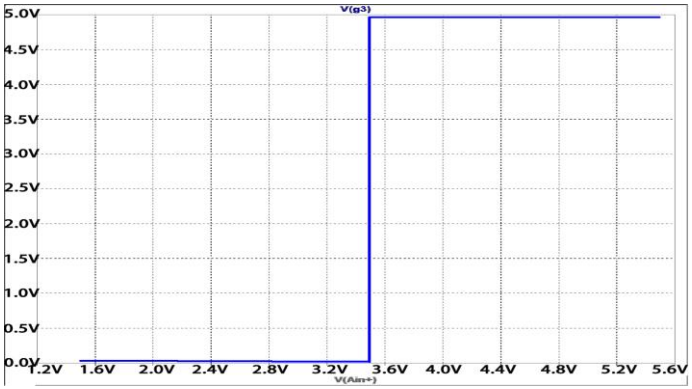


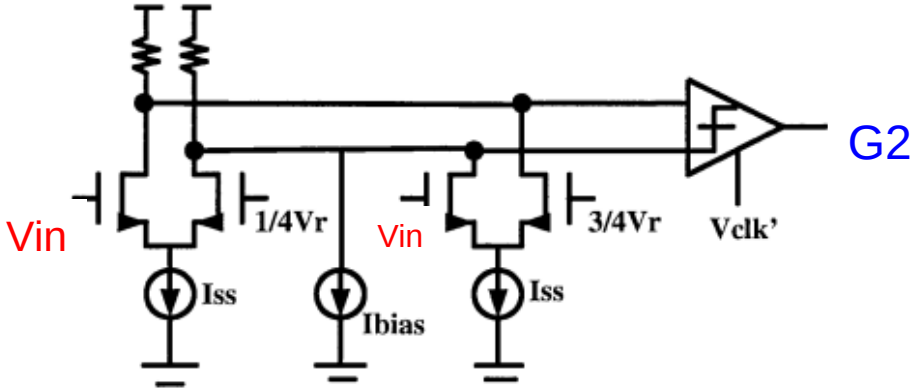
Current-Mode Analog Encoder for G3, G2

SPICE simulation result

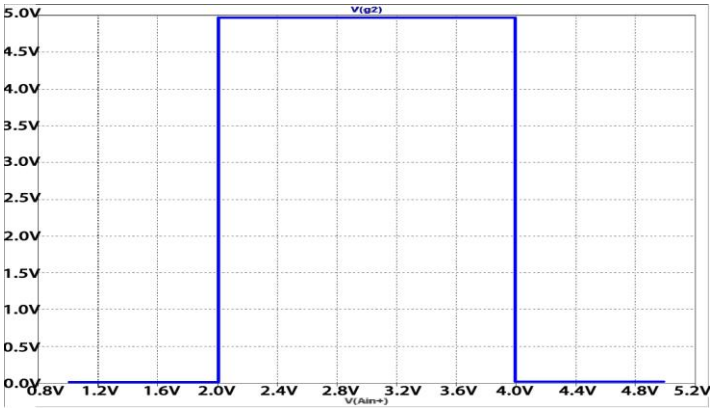


G3



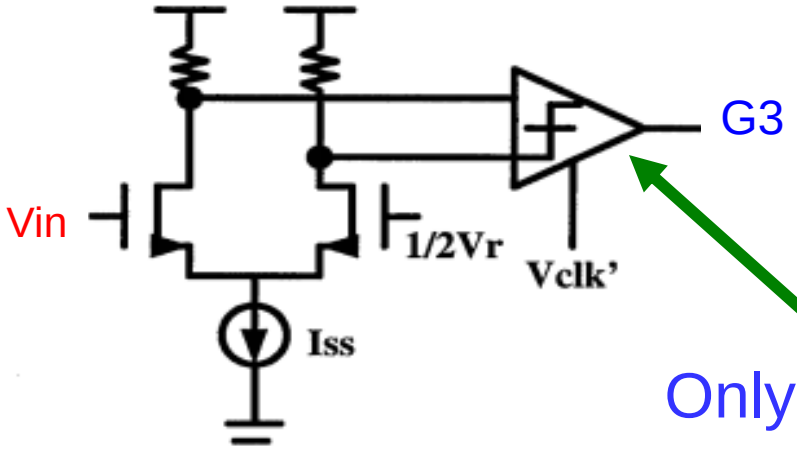


G2

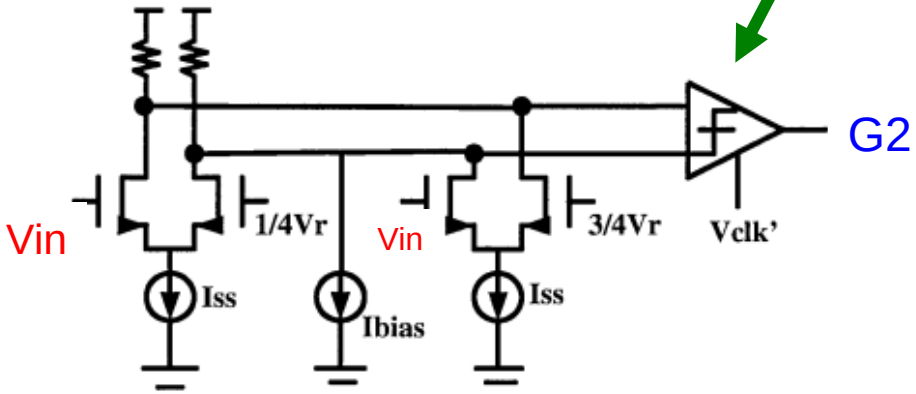


Analog input Vin

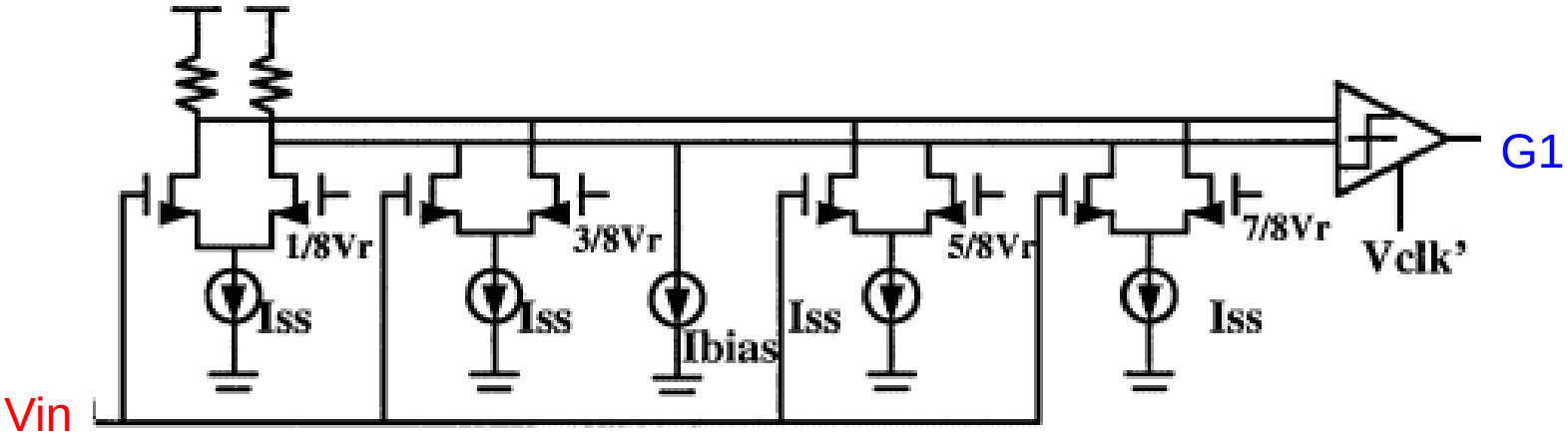
Current-Mode Analog Encoder for G3, G2



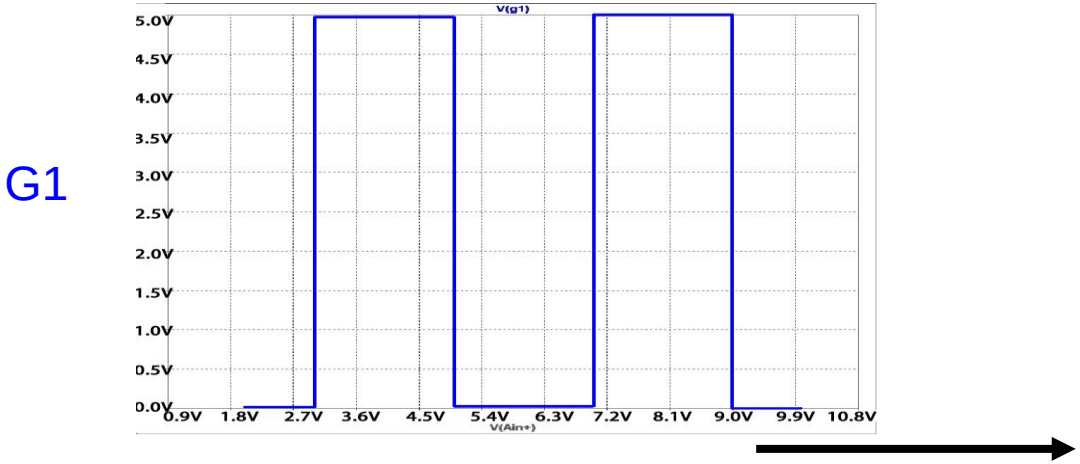
Only one comparator for each G3, G2



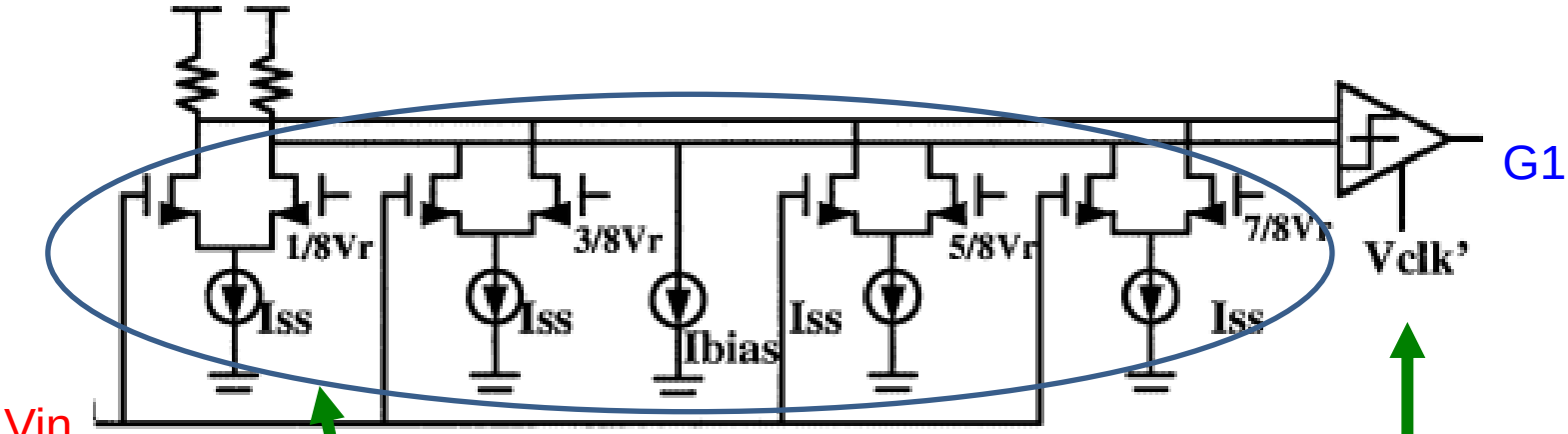
Current-Mode Analog Encoder for G1



SPICE simulation result



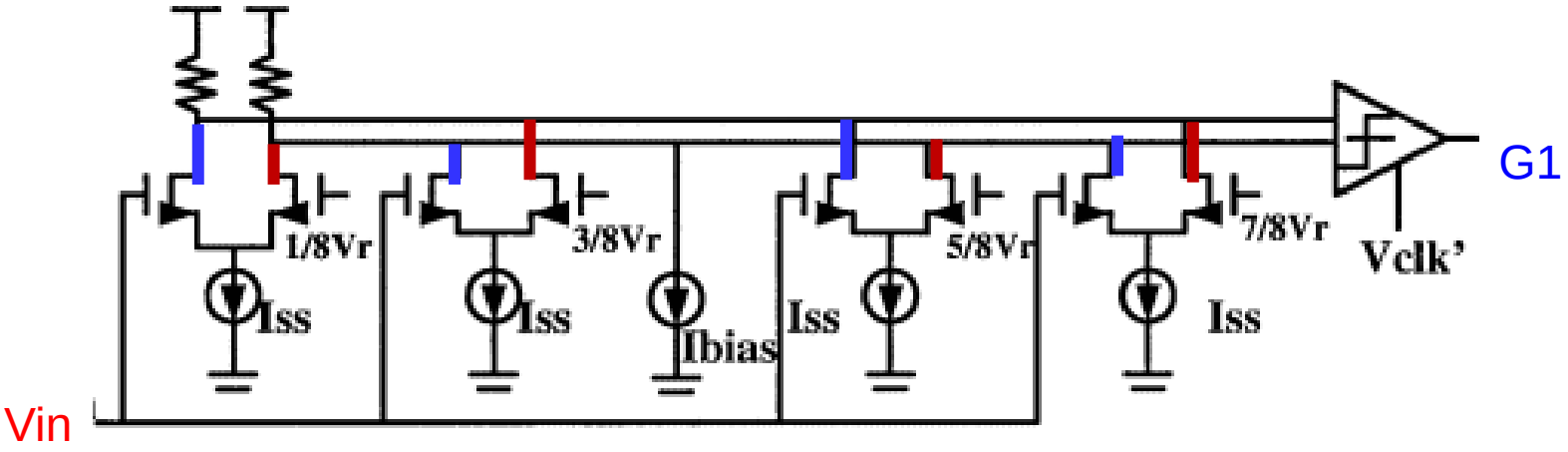
Current-Mode Analog Encoder for G1



Analog encoder

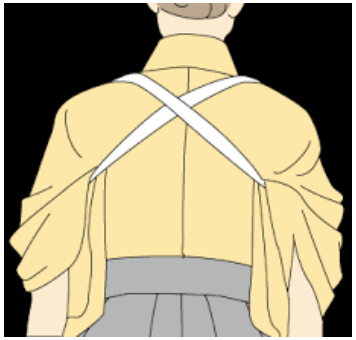
Only one comparator for G1

Current-Mode Analog Encoder for G1



Gray code analog encoder

⇒ Cross-coupling of NMOS pairs



Features of Analog Encoder

Current-mode analog encoder

- Effective for hardware reduction
- Suitable for bipolar circuit,
  thanks to its high current drivability
- Not suitable for CMOS circuit
  (operation is slow)
  due to its low current drivability

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Consideration of CMOS Folding ADC

- CMOS circuit advantages

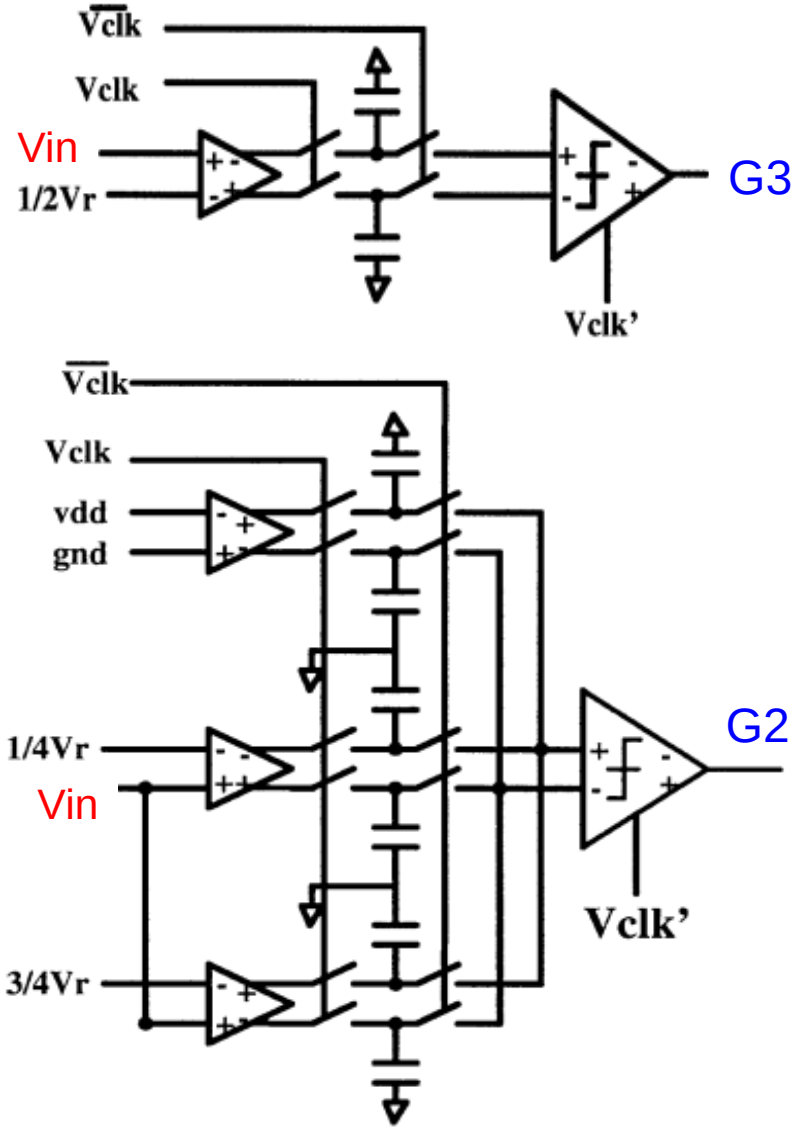
  - MOS switch usage

  - Preamplifier saturation characteristics usage

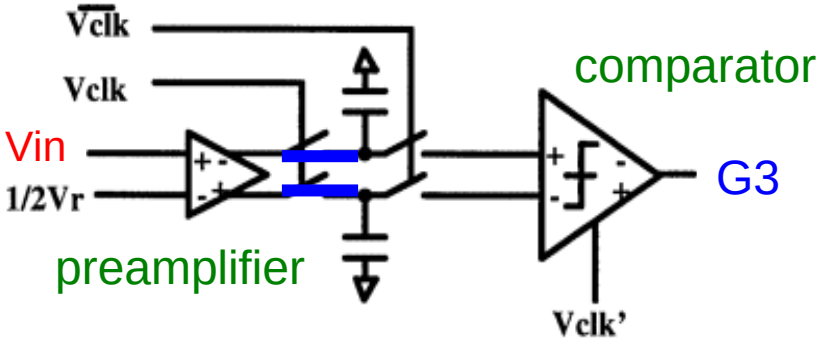
- Nonlinear switched capacitor folding circuit with CMOS

- Avoid CMOS low current drivability

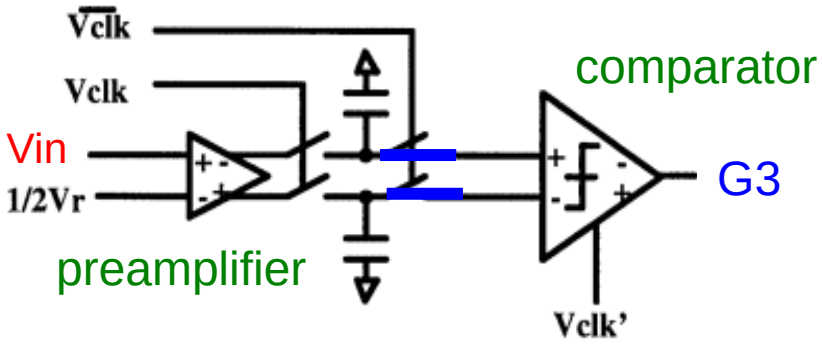
Charge-Domain Folding ADC



Operation of Charge-Domain Folding ADC for G3



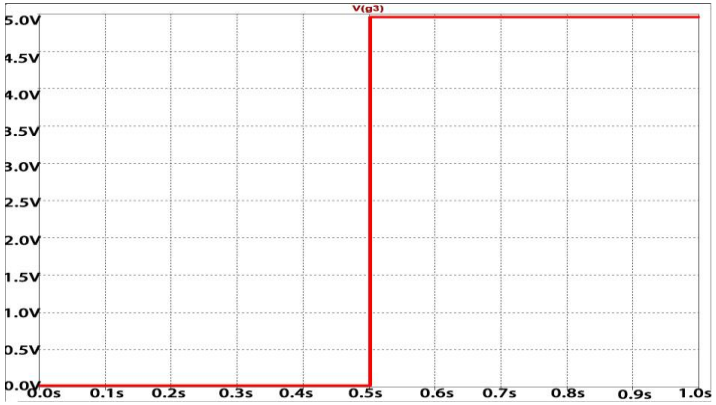
Phase 1



Phase 2

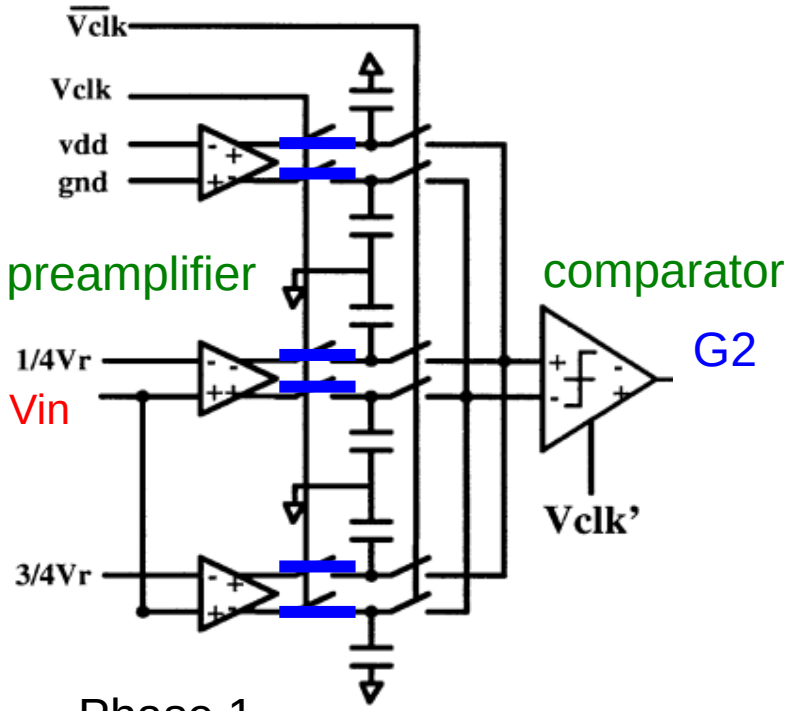
SPICE simulation result

G3

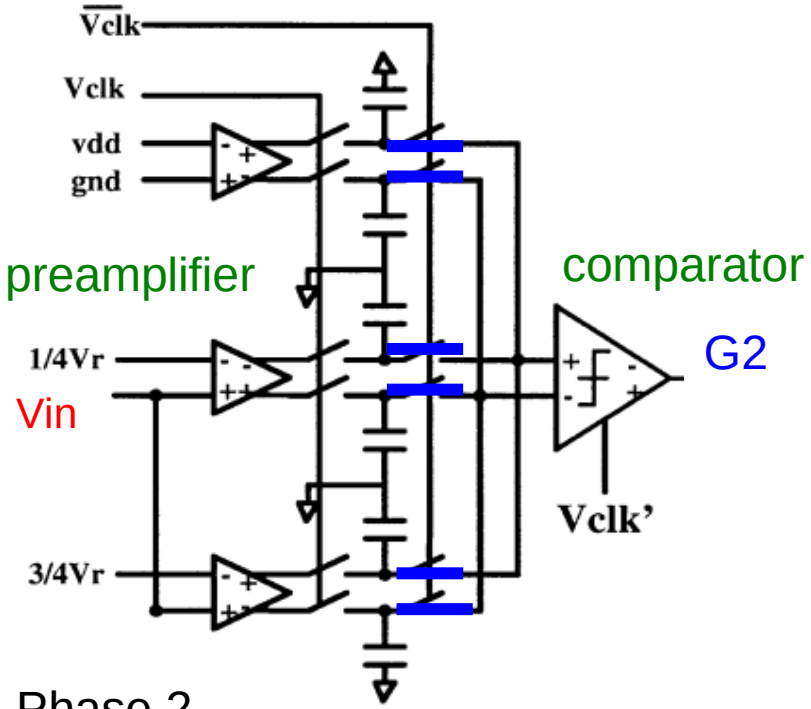


Analog input Vin

Operation of Charge-Domain Folding ADC for G2



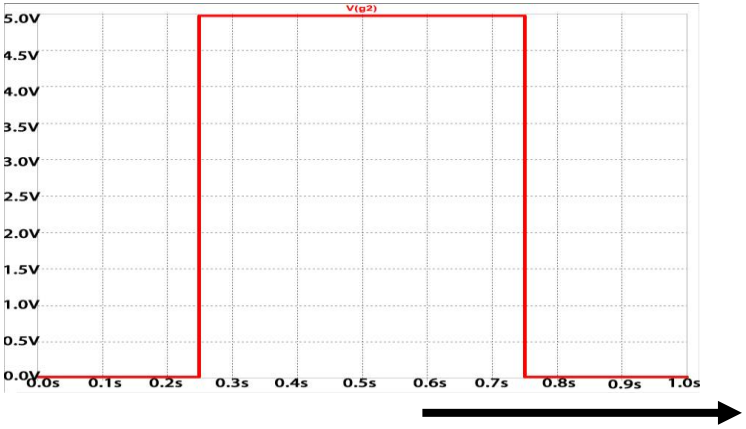
Phase 1



Phase 2

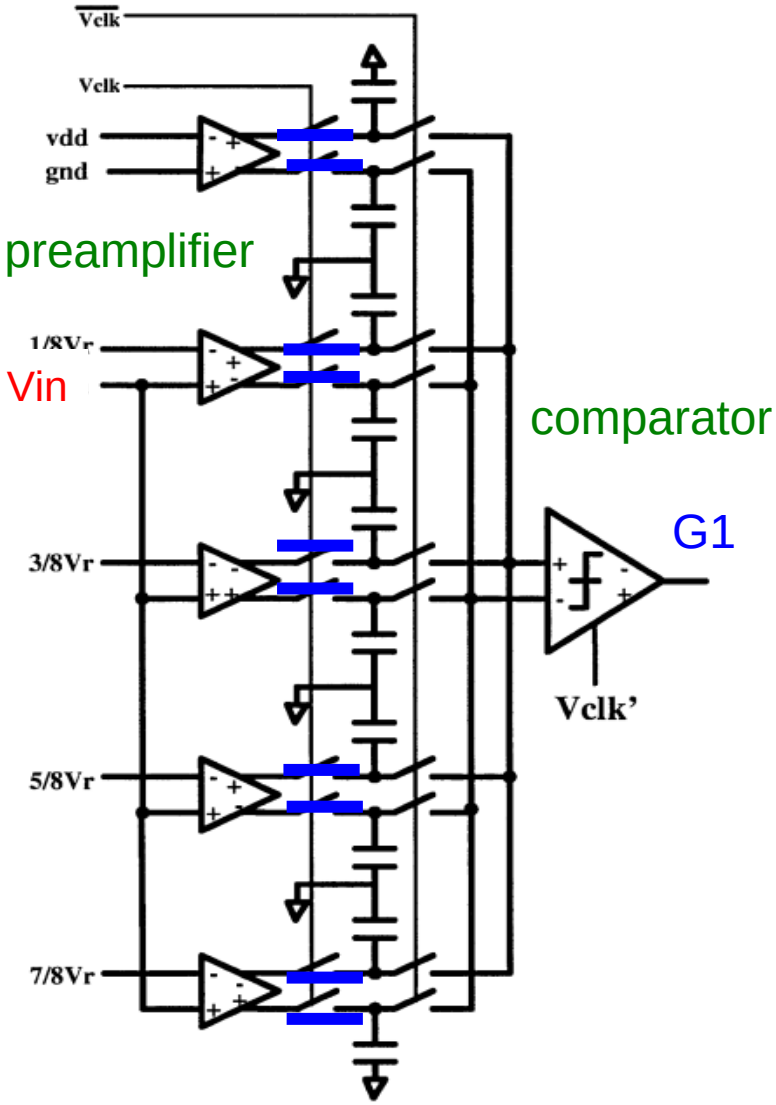
SPICE simulation result

G2

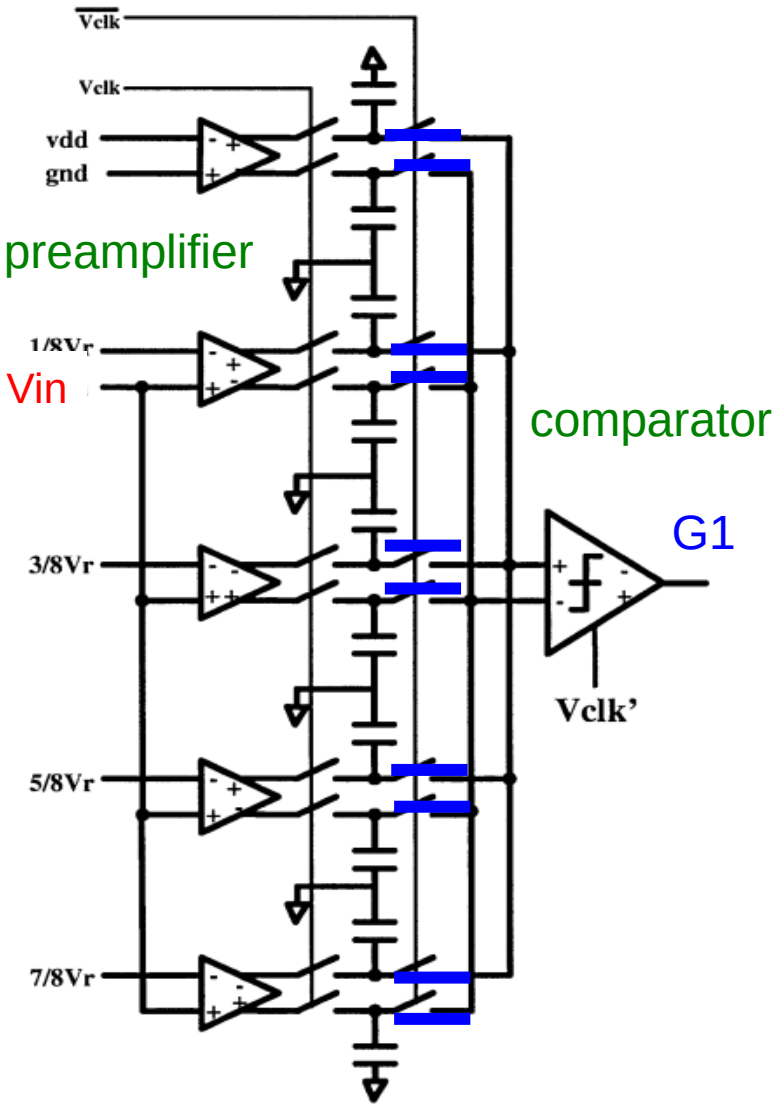


Analog input Vin

Operation of Charge-Domain Folding ADC for G1

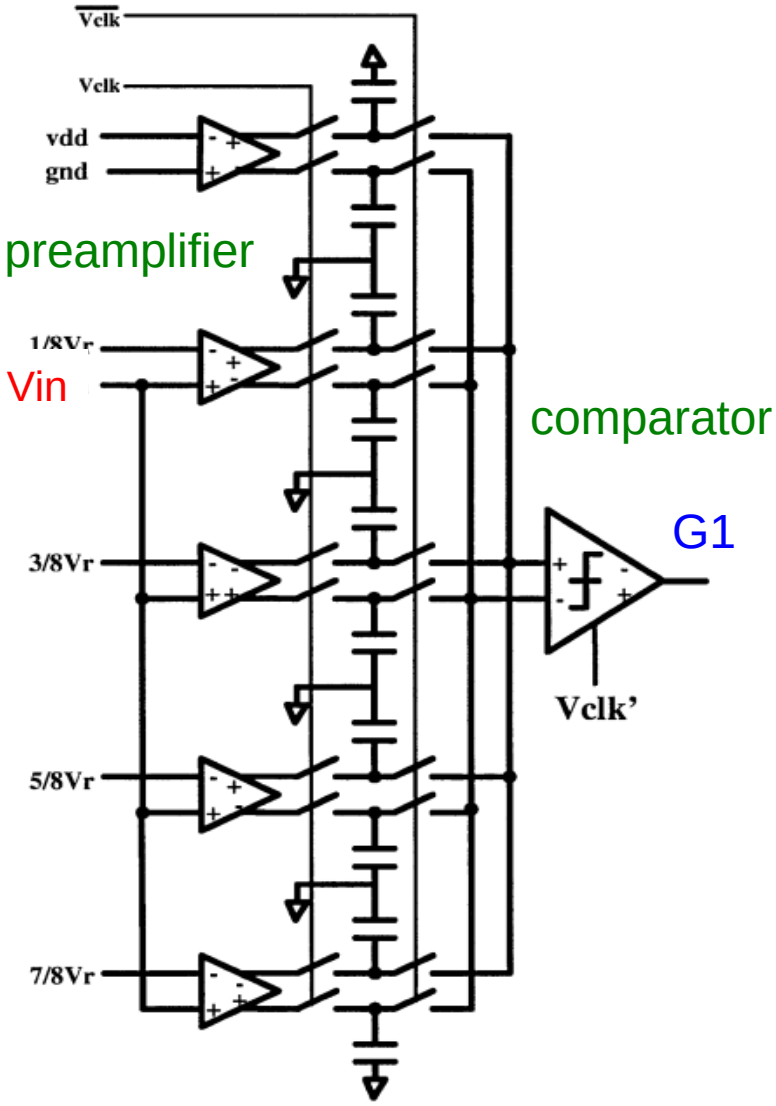


Phase 1



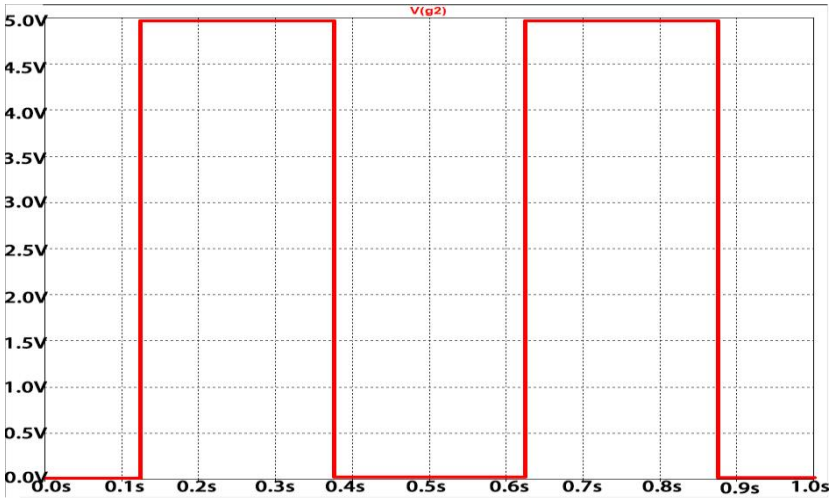
Phase 2

Operation of Charge-Domain Folding ADC for G1



SPICE simulation result

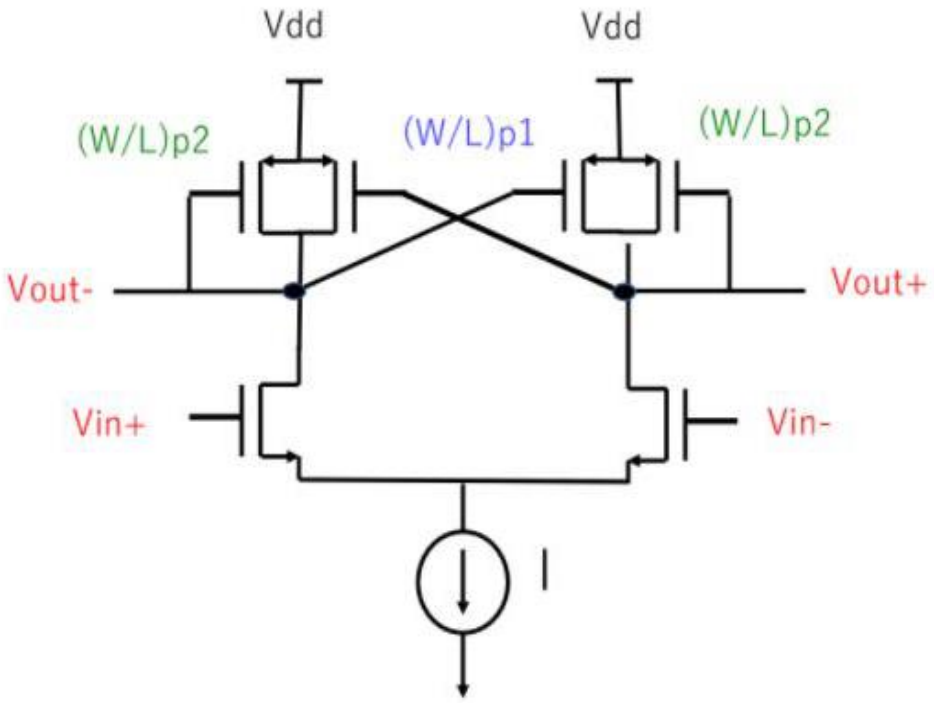
G1



Analog input Vin

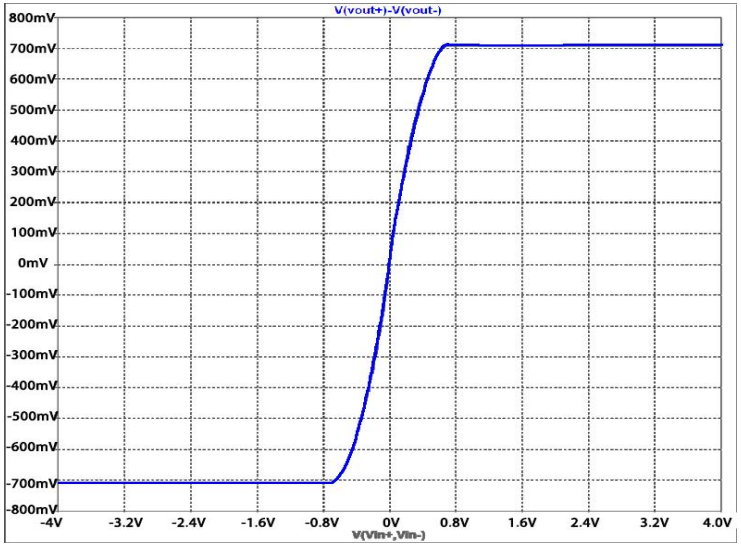
Preamplifier Circuit

Designed preamplifier circuit



SPICE simulation results

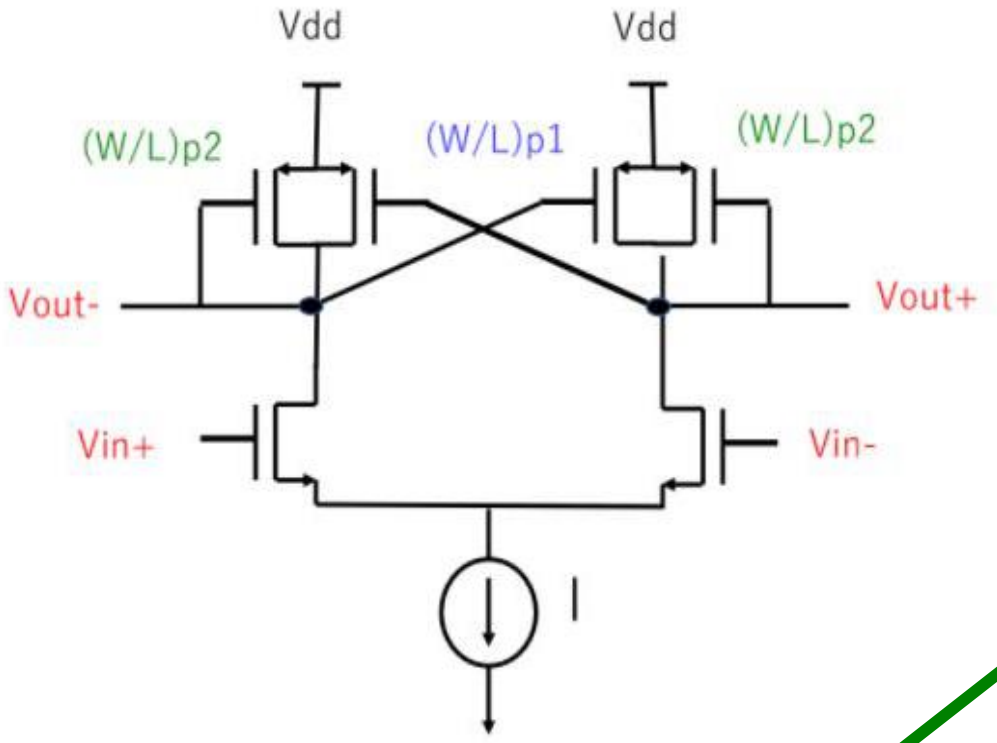
Vout+ - Vout-



Analog input Vin+ - Vin-

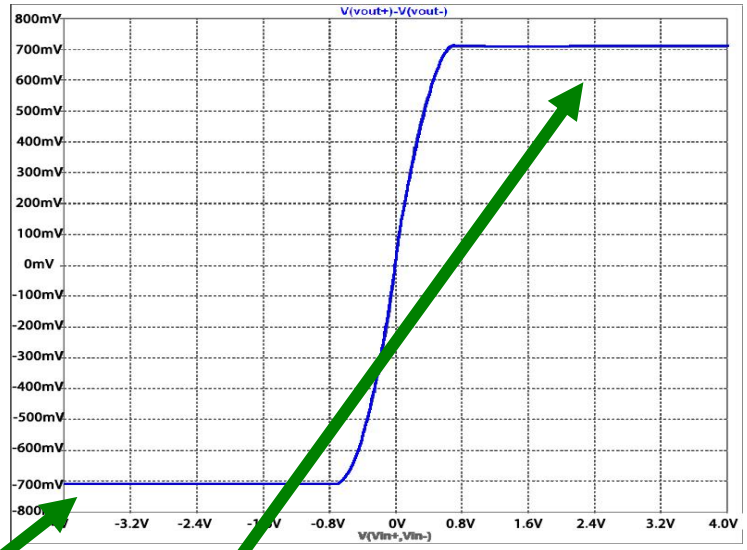
Preamplifier Circuit

Designed preamplifier circuit



SPICE simulation results

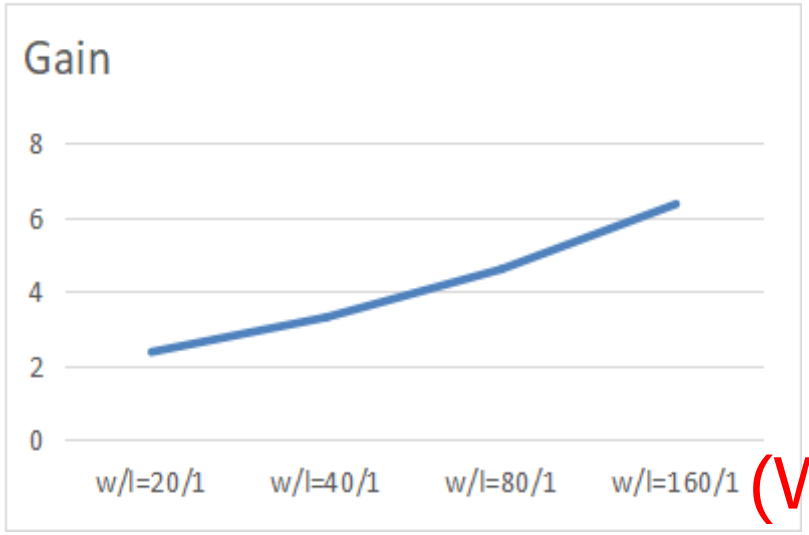
Vout+ - Vout-



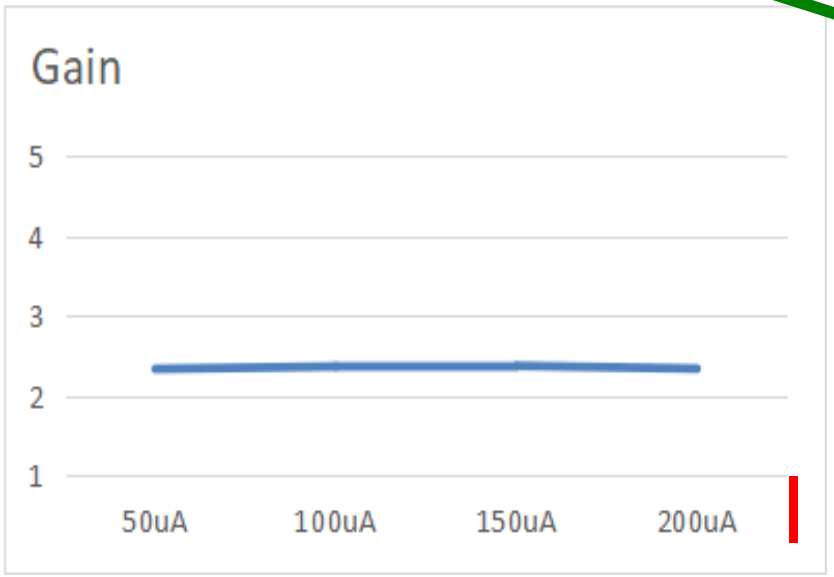
Analog input Vin+ - Vin-

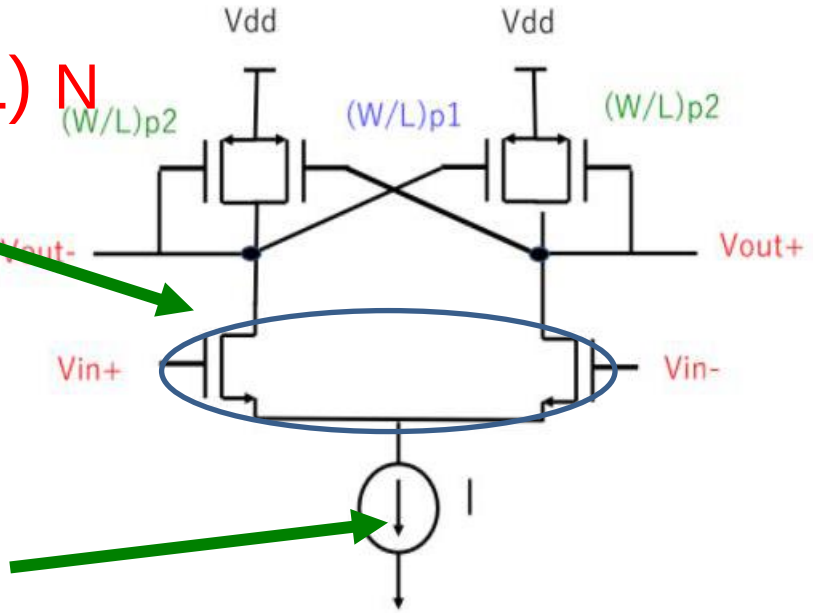
Use saturation (nonlinearity) for charge-domain folding circuit

Preamplifier Circuit Gain vs Parameters (1)

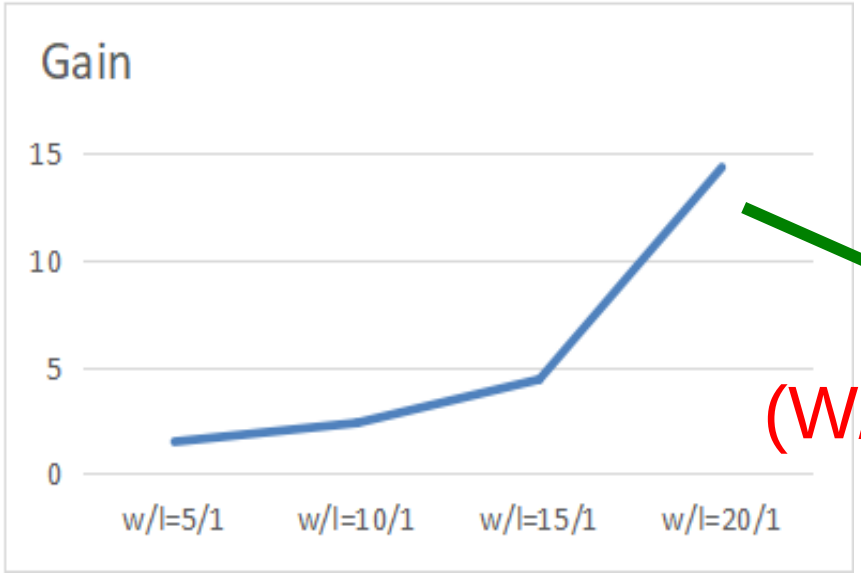


(W/L) N

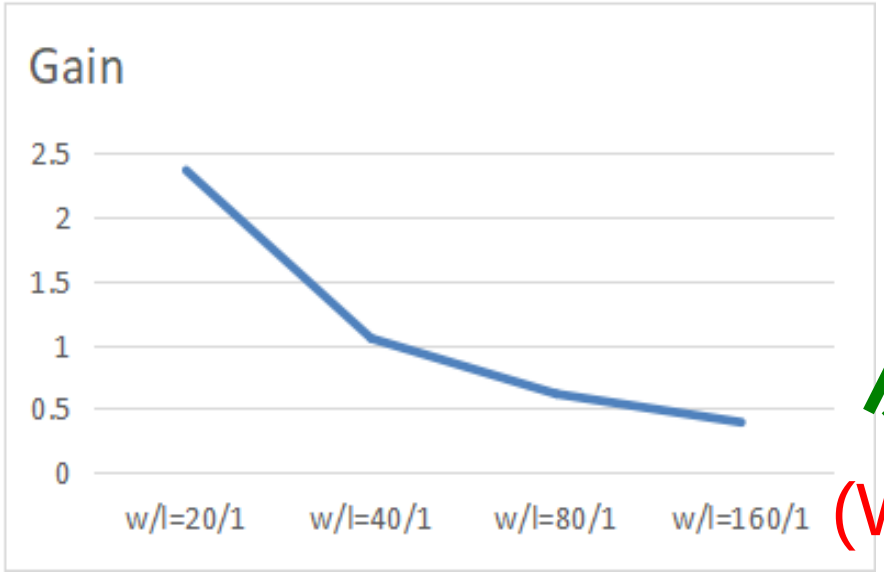




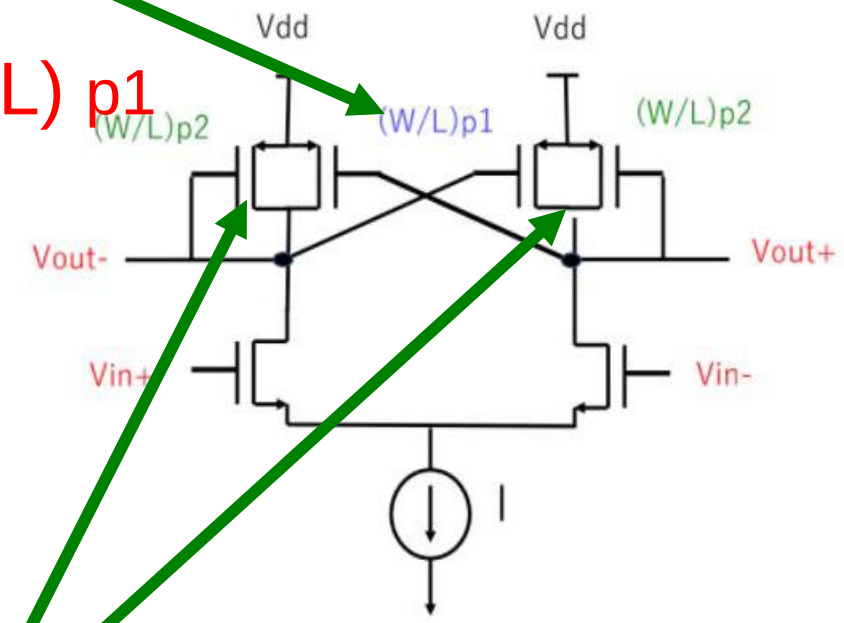
Preamplifier Circuit Gain vs Parameters (2)



(W/L) p1



(W/L) p2



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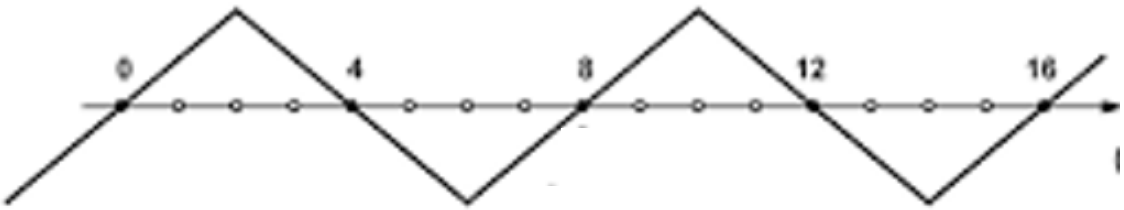
Conclusion

Charge-domain folding ADC is proposed.

- Significant hardware reduction
- Suitable for CMOS implementation
  ⇒ Usage of MOS switch & capacitor
- Basic circuit topology, operation and SPICE simulation results are shown.
- Detailed performance evaluation is next work.

Thank you for listening

Folding Circuit



七転八起

Q&A

- Question:

  Why the proposed charge-domain folding ADC is faster ?

- Answer:

  It’s realization with the charge mode (switched capacitor method) is examined, and only one comparator is used for 1-bit to remove redundant operations.

  So it will be faster.