Ph. D. Dissertation Title:

Histogram Method for Efficient ADC Linearity Test: Input Signal for Code Selection and Ratio of Input and Sampling Frequencies

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Ph. D. Dissertation Summary

Background:

In recent years, Internet of Things (IoT) has attracted much attention, and the testing of IoT-related ADC in short time with high quality has become more important at mass production shipping for the IoT system reliability. However, its linearity testing takes long time, and therefore it is often omitted at mass production shipping, even though it is an important performance index.

Target & Objective:

Our research target is to develop the ADC linearity testing technology using the histogram method in short time and with good testing accuracy.

Approach:

We have revisited the mature histogram method for the ADC linearity test in Fig.1 to meet these two demands and obtained the following results:

(i) A two-tone input signal with appropriate ratio of two frequencies for code selective ADC linearity test is proposed, by considering the ADC output codes where nonlinearity is likely to occur due to the ADC under test own configuration such as an internal DAC circuit [1, 4]. This signal can be synthesized using an arbitrary waveform generator (AWG),

(ii) We have investigated the optimal relationship of the input and sampling frequencies ratio for the saw input histogram minimum error [2,3].

Simulation Verification:

(i) We observe that the gentler the slope of the input signal waveform is, the more samples at the corresponding amplitude positions (codes) in the obtained ADC output histogram are. Therefore, we consider to reduce the input signal slope at the corresponding amplitude positions by combining sine waves [4]; in Fig.2 and Fig.3, we have focused the histogram on specific codes (256, 768) by synthesizing two sine waves.

(ii) In Fig.4, we consider a saw input signal and introduce the root-mean-square (RMS) error between the ideal and sampled histograms. If the RMS error is small, the ADC linearity can be measured with the small number of the samples. This is based on our another research for the waveform acquisition efficiency using the equivalent-time sampling [5]. In Fig.5, we have obtained the RMS error comparison of the histogram formed by adjusting the frequency ratio of the input and sampling signals. We found that the metallic ratios (Table 1) are effective.

Conclusion:

We successfully focused the histogram on specific codes by using a simple method to synthesize a two-tone sine wave. The simulation results verified the effectiveness of the proposed code selective histogram method. As the second research, we set several ratios between the input saw signal sampling frequencies, and evaluated the obtained histogram with the ideal one. To our knowledge, the histogram RMS error concept is new. These results can be used to obtain the better ADC linearity testing accuracy with small number of samples using the histogram method.

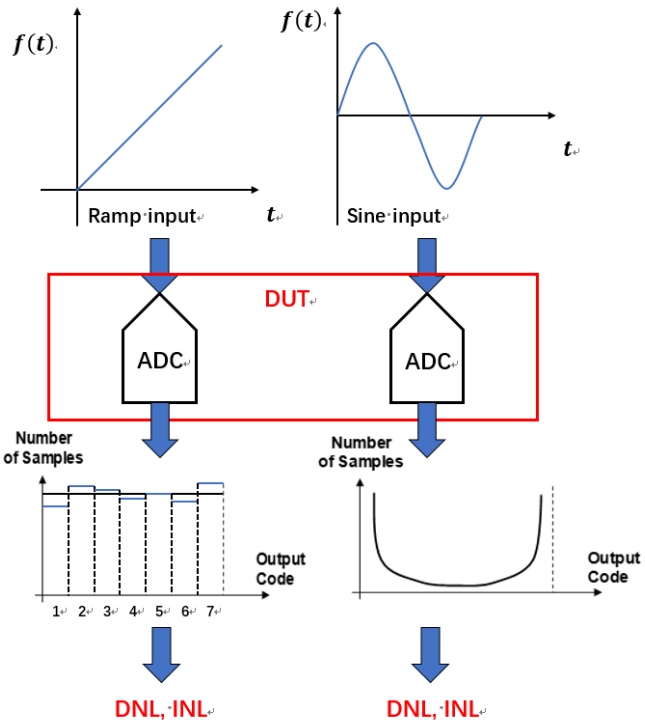

Fig.1. ADC test signals (ramp and sine) and histograms for the linearity test.

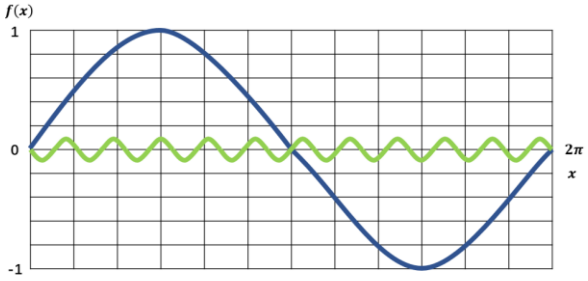

Fig.2. $f_{11}(x) = \sin(x)$ in blue and $f(x) = -\frac{\sin(11x)}{11}$ in green

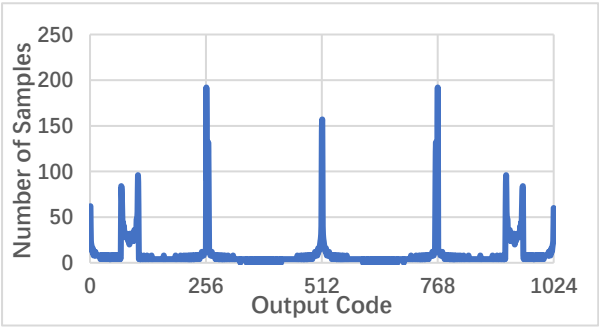

Fig.3. ADC output histogram for the input of $f_{11}(x) = \sin(x) - \frac{\sin(11x)}{11}$.

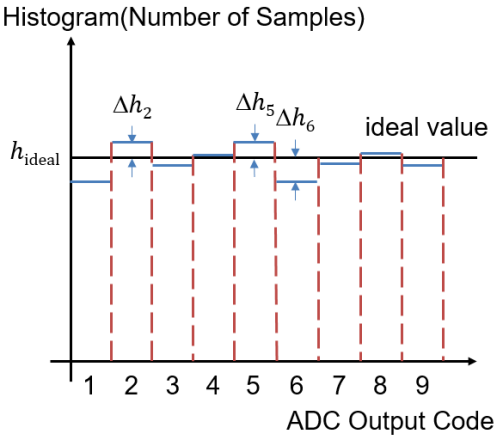

Fig.4. ADC output histogram for the ramp input in case that the ADC under test has non-linearity

Table.1. The n-th metallic ratios

n	Ratio	Decimal expansion	Nickname
1	$(1+\sqrt{5})/2$	1.6180339887…	Golden ratio
2	$1+\sqrt{2}$	2.4142135623…	Silver ratio
3	$(3+\sqrt{13})/2$	3.3027756377…	Bronze ratio
…	…		
n	$(n+\sqrt{n^2+4})/2$		

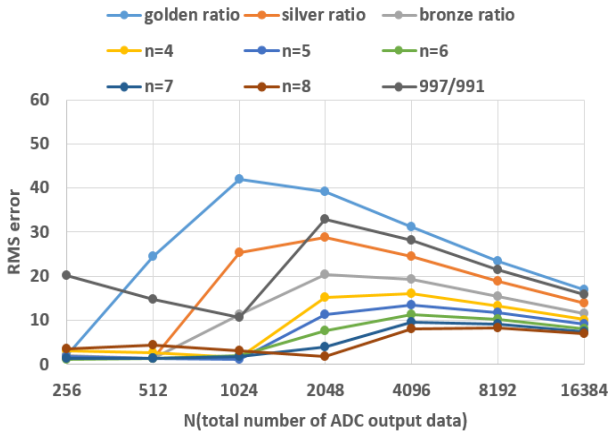

Fig.5. Histogram RMS error comparison for the ideal ADC for several ratios of the ramp input and sampling frequencies.

Published papers:

[1] Y. Zhao, A. Kuwana, Y. Du, Y. Ozawa, Y. Sasaki, H. Kobayashi, T. Nakatani, K. Hatayama, K. Sato, T. Ishida, T. Okamoto, T. Ichikawa, "Consideration on Input Signal for ADC Histogram Test in Short Time", Advanced Engineering Forum, Vol. 38, Nov. 2020.

[2] Y. Zhao, A. Kuwana, S. Yamamoto, Y. Sasaki, H. Kobayashi, T. Nakatani, K. Hatayama, K. Sato, T. Ishida, T. Okamoto, T. Ichikawa, "Efficient Histogram Testing Condition with Histogram Method", 4th International Conference on Technology and Social Science (ICTSS), Kiryu, Gunma, Dec.2020.

[3] Y. Zhao, A. Kuwana, S. Yamamoto, Y. Sasaki, H. Kobayashi, T. Tran, T. Nakatani, K. Hatayama, K. Sato, T. Ishida, T. Okamoto, T. Ichikawa, J. Wei, S. Katayama, "Input Signal and Sampling Frequencies Requirements for Efficient ADC Testing with Histogram Method", 36th International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC), Jeju, Korea, June 2021.

[4] Y. Zhao, A. Kuwana, S. Katayama, J. Wei, H. Kobayashi, T. Nakatani, K. Hatayama, K. Sato, T. Ishida, T. Okamoto, T. Ichikawa, "Code Selective Histogram Method: Two-Tone Signal for ADC Linearity Test Time Reduction", International Conference on Analog VLSI Circuits (AVIC), Bordeaux, France, Oct. 2021.

[5] S. Yamamoto, Y. Sasaki, Y. Zhao, J. Wei, A. Kuwana, K. Sato, T. Ishida, T. Okamoto, T. Ichikawa, T. Nakatani, T. Tran, S. Katayama, K. Hatayama, H. Kobayashi, "Metallic Ratio Equivalent-Time Sampling: A Highly Efficient Waveform Acquisition Method", 27th IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS), Virtual Event, June 2021.