Invited Paper

Classical Mathematics and Analog / Mixed-Signal IC Design

Haruo Kobayashi, X. Bai, Y. Zhao, S. Yamamoto, D. Yao

M. Hirai, J. Wei, S. Katayama, A. Kuwana

Division of Electronics and Informatics
Gunma University

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[1] (invited) H. Kobayashi, Y. Sasaki, H. Arai, D. Yao, Y. Zhao, X. Bai, A. Kuwana,
"Unified Methodology of Analog/Mixed- Signal IC Design Based on Number Theory",
IEEE 14th International Conference on Solid-State and Integrated Circuit Technology, Qingdao, China (Nov. 2018).
[2] (Invited) H. Kobayashi, H. Lin,
"Analog / Mixed-Signal Circuit Design Based on Mathematics",
IEEE 13th International Conference on Solid-State and Integrated Circuit Technology, Hangzhou, China (Oct. 2016).

Our Statement

Beautiful mathematics

⇨ good analog/mixed-signal circuit

Besides transistor level design

- Integer theory
- Coding theory
- Control theory
- Statistics
- Modulation
- Signal processing algorithm

⇩

Enhance analog/mixed-signal circuit performance

Integer Theory and Electronic Circuit Design

Many interesting properties of Integers

Currently
No Link

Electronic circuit designs

Our research here makes their links !

Carolus Fridericus Gauss
(1777-1855)

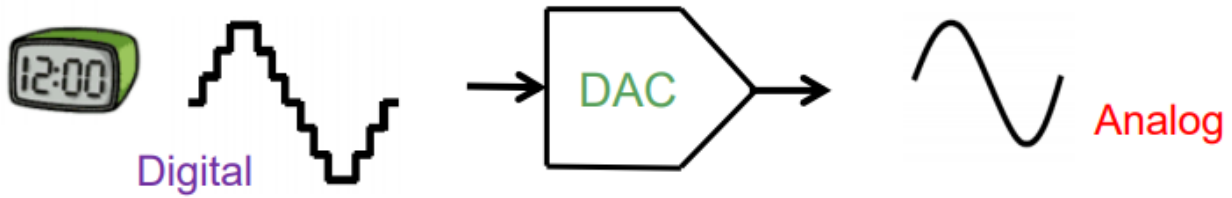
Integer theory is
Queen of Mathematics

Contents

[3] X. Bai, D. Yao, Y. Du, M. T. Tran, A. Kuwana, H. Kobayashi, K. Kubo,
"Design of Digital-to-Analog Converter Architectures Based on Polygonal Numbers”,
International Conference on Analog VLSI Circuits, Bordeaux, France (Oct. 2021)

[4] Y. Du, X. Bai, M. Hirai, S. Yamamoto, A. Kuwana, H. Kobayashi, K. Kubo,
"Digital-to-Analog Converter Architectures Based on Polygonal and Prime Numbers",
17th International SOC Design Conference, Yeosu, Korea (Oct. 2020)

DACs are Everywhere !



Communication equipment

Electronic measuring instrument

Audio systems

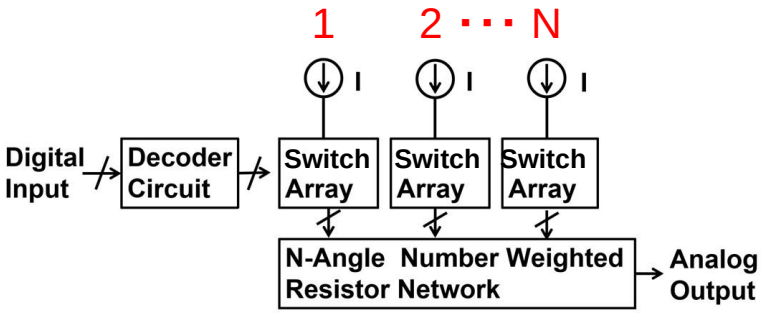
Research Objective

- **Interesting properties of polygonal numbers**

- **New configurations of DAC**

Polygonal number DAC

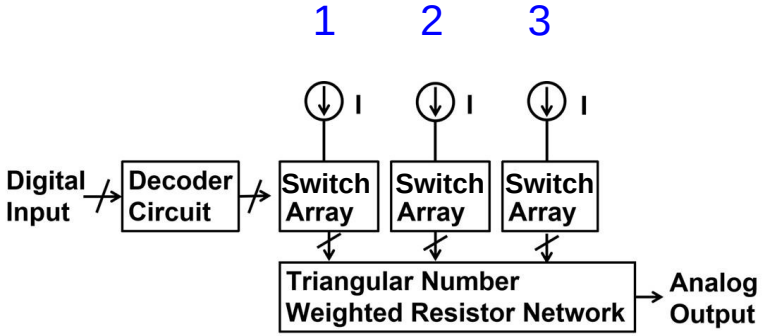
N current sources
N switch arrays



N=3, 4, 5, ….

Triangular number DAC

3 current sources
3 switch arrays

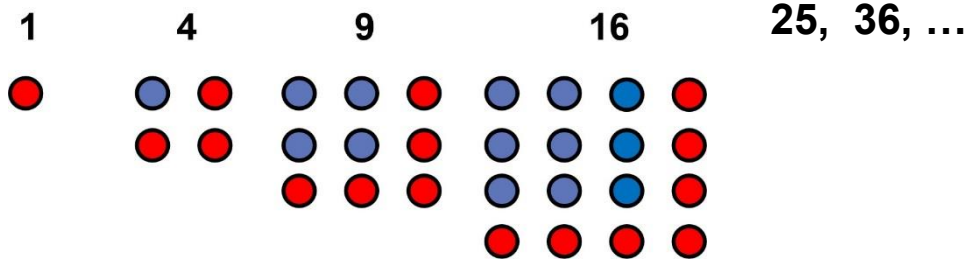


What is Polygonal Number ?

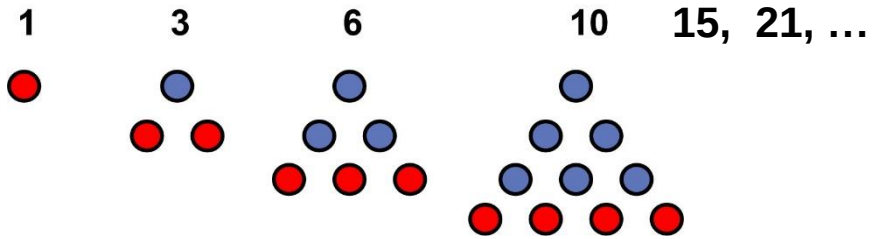
Polygonal Number

Represented as dots arranged in regular polygon shaper.

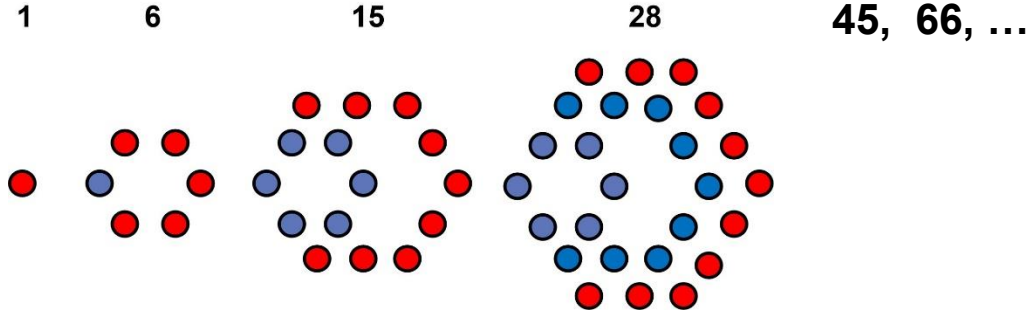
Square numbers.



Triangular numbers.



Hexagonal numbers.



Fermat Polygonal Number Theorem

Any natural number

⬇ **expressed by**

Sum of N N-angular numbers

French mathematicians

Conjecture

Pierre de Fermat
1607 – 1665

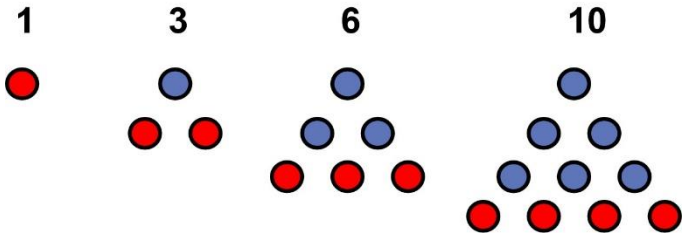
Augustin-Louis Cauchy
1789 –1857

Proved in 1813

Triangular Number Case

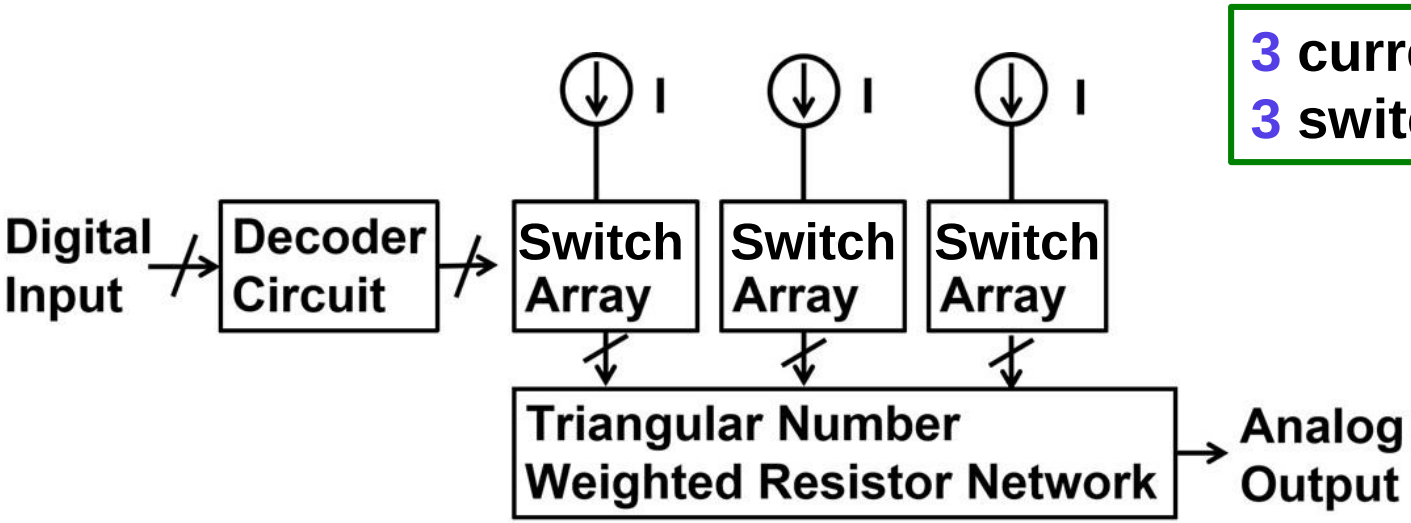
Any natural number ➡ Sum of 3 triangular numbers

expressed by



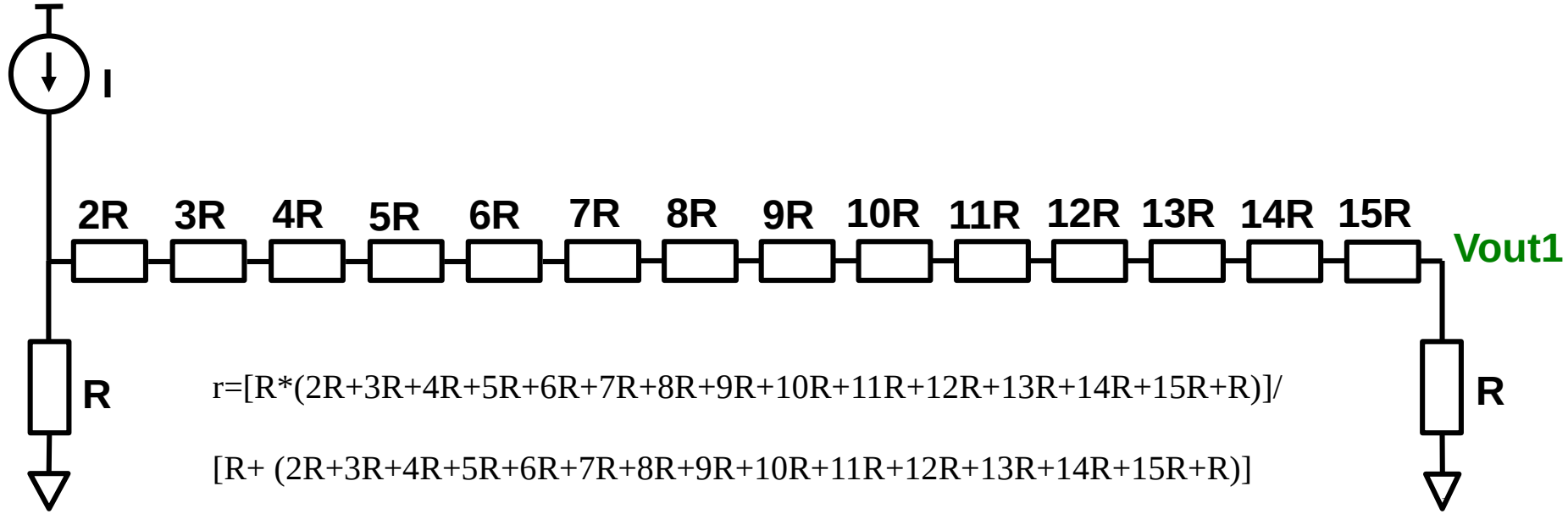
1:	1
2:	1+1
3:	3
4:	1+3
5:	1+1+3
6:	6
7:	1+6
8:	1+1+6
9:	3+6
10:	10
11:	1+10
12:	1+1+10
13:	3+10
14:	1+3+10
15:	15
16:	1+15
17:	1+1+15
18:	3+15
19:	1+3+15
20:	10+10
21:	21
22:	1+21
23:	1+1+21
24:	3+21
25:	1+3+21
26:	1+10+15
27:	6+21
28:	28
29:	1+28
30:	1+1+28
31:	3+28
32:	1+3+28
33:	6+6+21
34:	6+28
35:	1+6+28
36:	36
37:	1+36
38:	1+1+36
39:	3+36
40:	1+3+36
41:	3+10+28
42:	6+36
43:	1+6+36
44:	6+10+28
45:	45
46:	1+45
47:	1+1+45
48:	3+45
49:	1+3+45
50:	1+21+28
51:	15+36
52:	1+6+45
53:	10+15+28
54:	3+6+45
55:	55
56:	1+55
57:	1+1+55
58:	3+55
59:	1+3+55
60:	15+45

Proposed Triangular Number DAC



Triangular Number DAC Input 1

Triangular Number : 1, 3, 6, 10, 15, 21, 28, 36, 45, 55, 66, 78, 91, ..n(n+1)/2



r=[R*(2R+3R+4R+5R+6R+7R+8R+9R+10R+11R+12R+13R+14R+15R+R)]/

[R+ (2R+3R+4R+5R+6R+7R+8R+9R+10R+11R+12R+13R+14R+15R+R)]

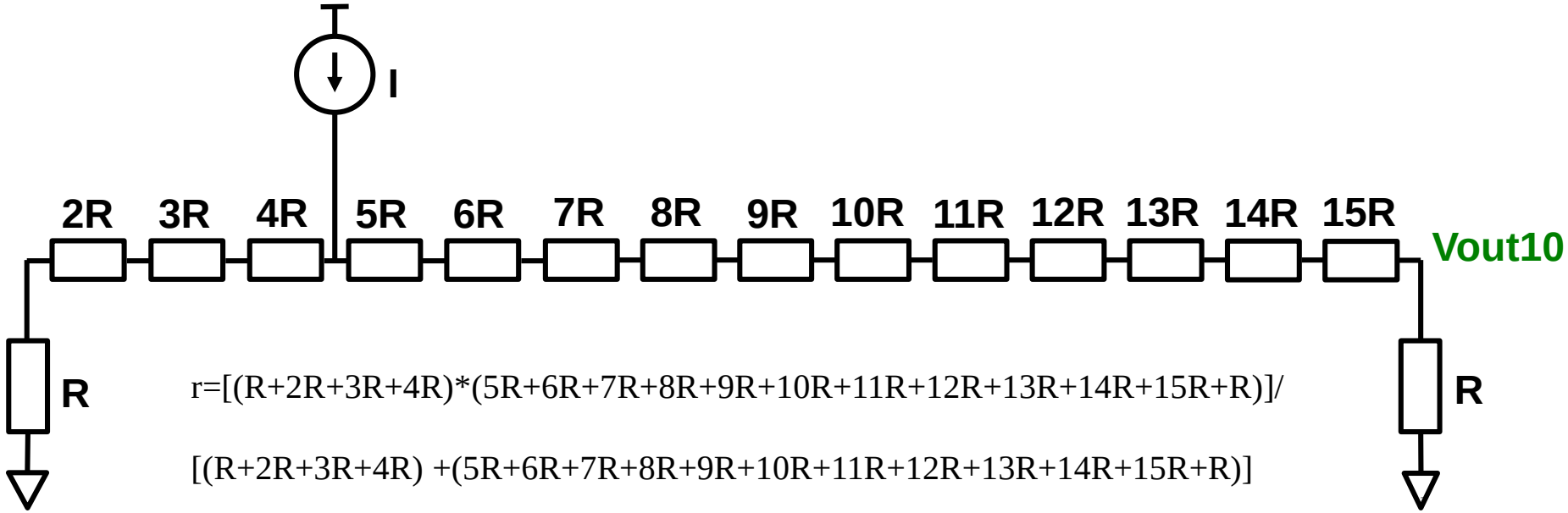
V=I*r

Vout1/V=R/(2R+3R+4R+5R+6R+7R+8R+9R+10R+11R+12R+13R+14R+15R+R)

Vout1=I*R/121

Triangular Number DAC Input 10

Triangular Number : 1, 3, 6, 10, 15, 21, 28, 36, 45, 55, 66, 78, 91, ..n(n+1)/2



r=[(R+2R+3R+4R)*(5R+6R+7R+8R+9R+10R+11R+12R+13R+14R+15R+R)]/

[(R+2R+3R+4R) +(5R+6R+7R+8R+9R+10R+11R+12R+13R+14R+15R+R)]

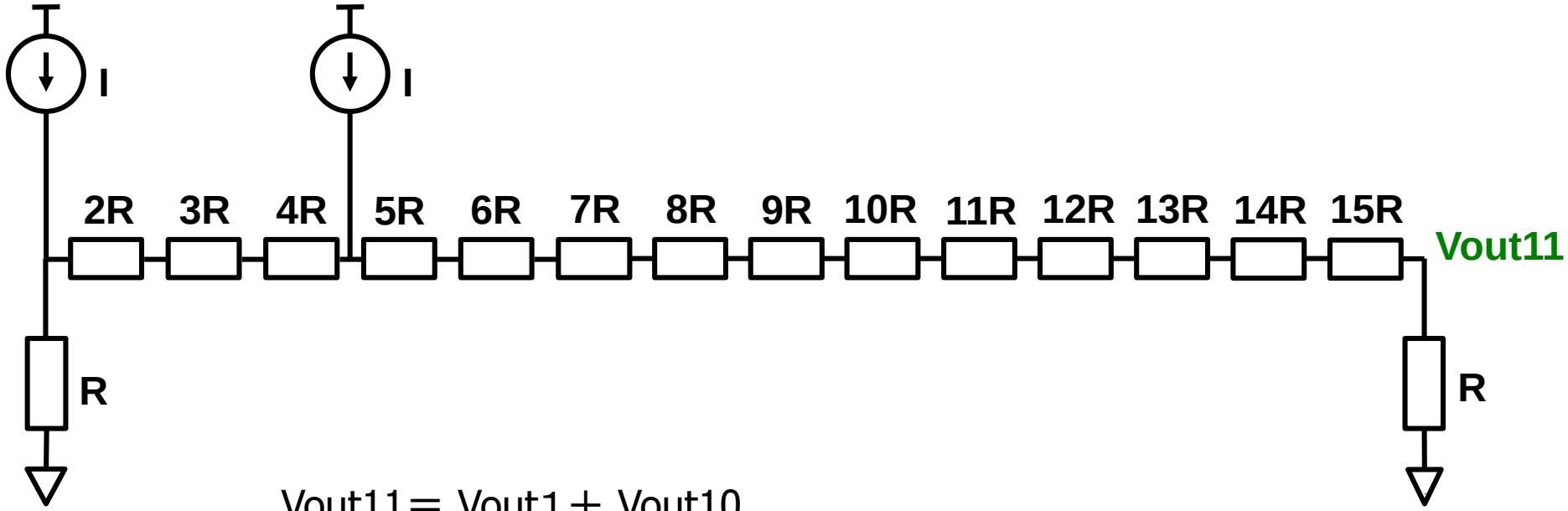
V=I*r

Vout10/V=R/(5R+6R+7R+8R+9R+10R+11R+12R+13R+14R+15R+R)

Vout10=10I*R/121

Triangular Number DAC Input 11

Triangular Number : 1, 3, 6, 10, 15, 21, 28, 36, 45, 55, 66, 78, 91, ..n(n+1)/2



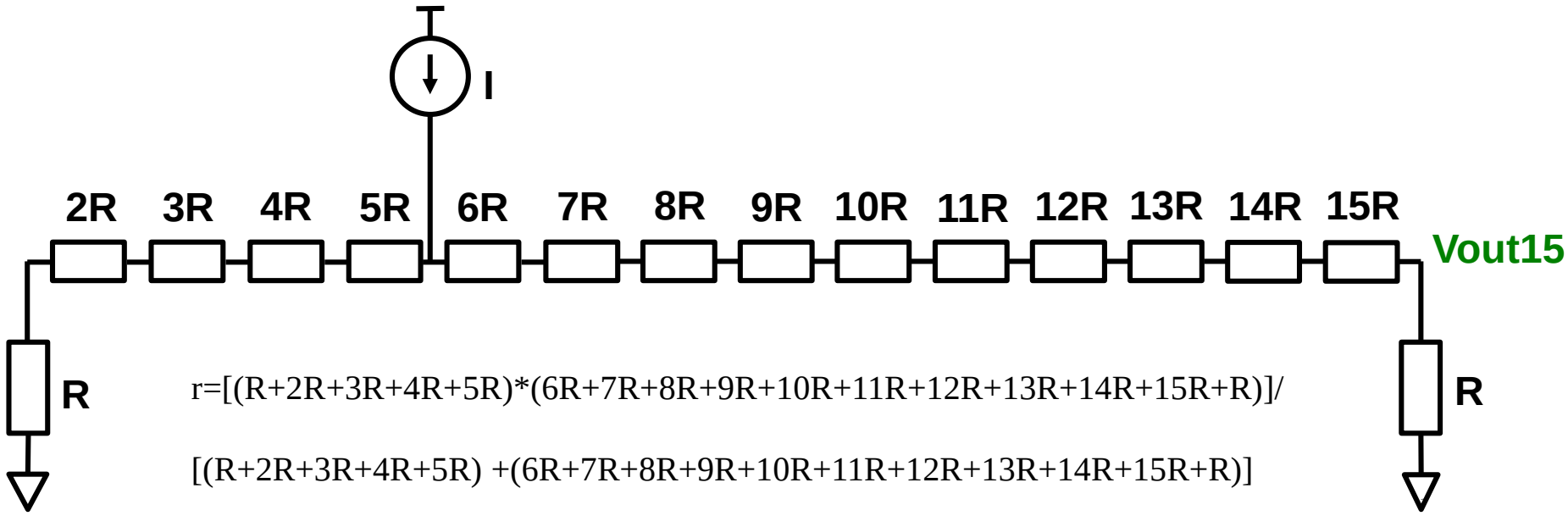
$$Vout11 = Vout1 + Vout10$$

$$= I*R/121 + 10I*R/121$$

$$= 11I*R/121$$

Triangular Number DAC Input 15

Triangular Number : 1, 3, 6, 10, 15, 21, 28, 36, 45, 55, 66, 78, 91, ..n(n+1)/2



r=[(R+2R+3R+4R+5R)*(6R+7R+8R+9R+10R+11R+12R+13R+14R+15R+R)]/

[(R+2R+3R+4R+5R) +(6R+7R+8R+9R+10R+11R+12R+13R+14R+15R+R)]

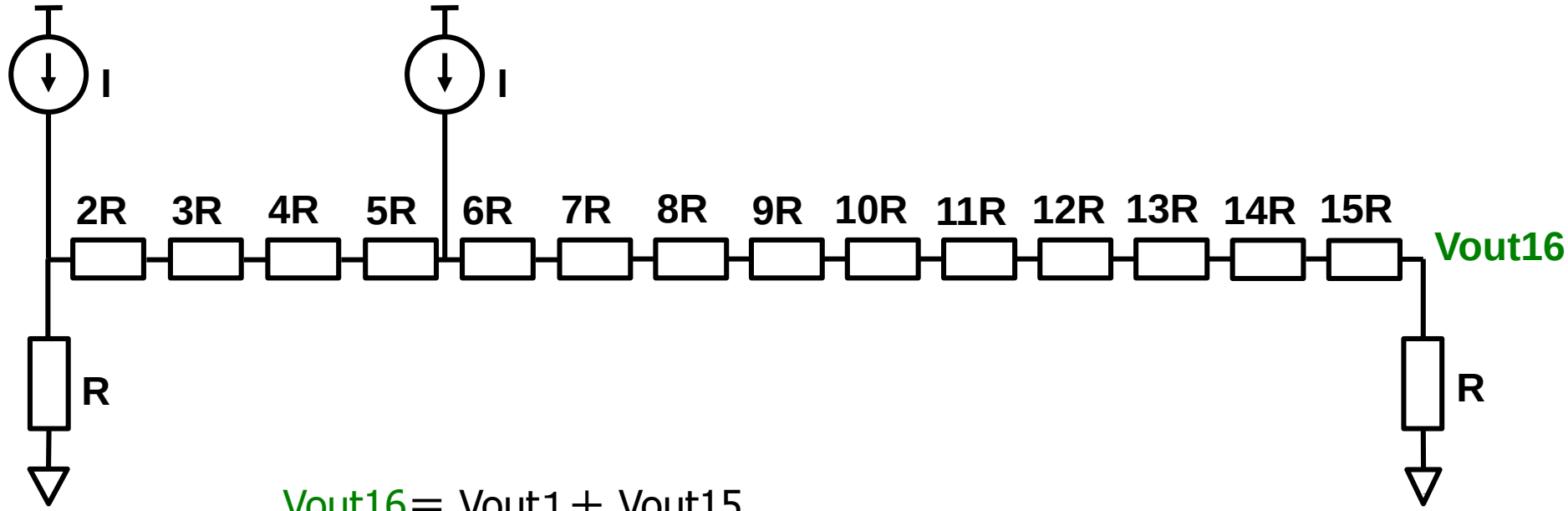
V=I*r

Vout15/V=R/(6R+7R+8R+9R+10R+11R+12R+13R+14R+15R+R)

Vout15=15I*R/121

Triangular Number DAC Input 16

Triangular Number : 1, 3, 6, 10, 15, 21, 28, 36, 45, 55, 66, 78, 91, ..n(n+1)/2



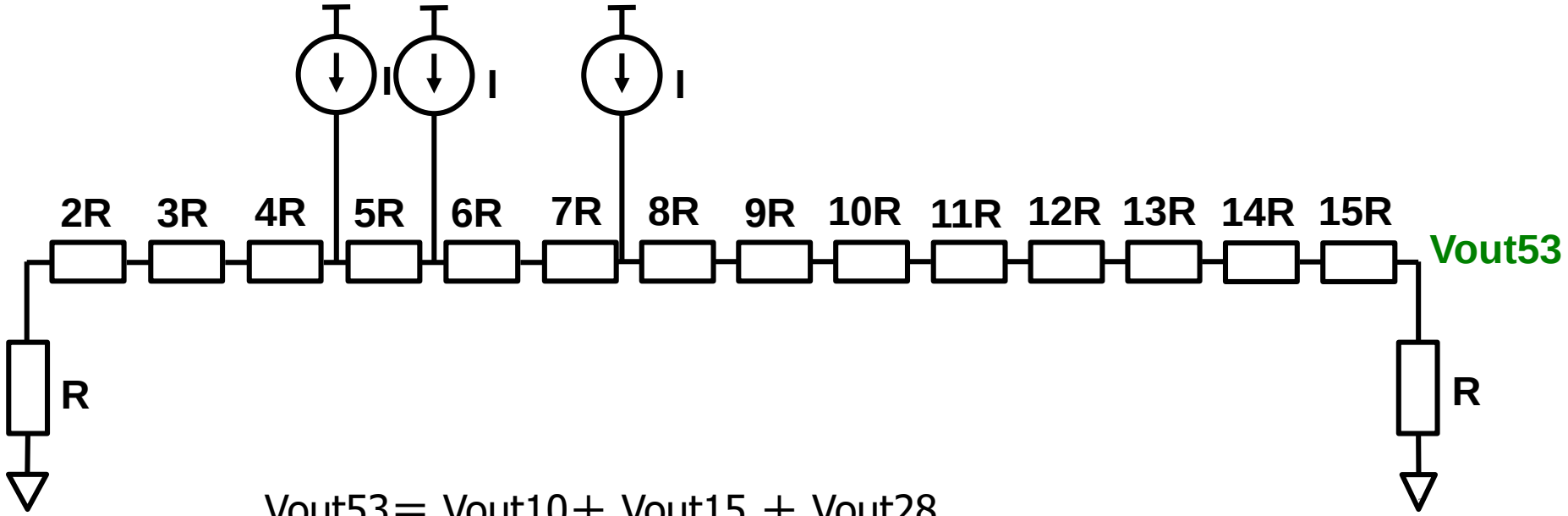
Vout16 = Vout1 + Vout15

= I*R/121 + 15I*R/121

= 16I*R/121

Triangular Number DAC Input 53

Triangular Number : 1, 3, 6, 10, 15, 21, 28, 36, 45, 55, 66, 78, 91, ..n(n+1)/2

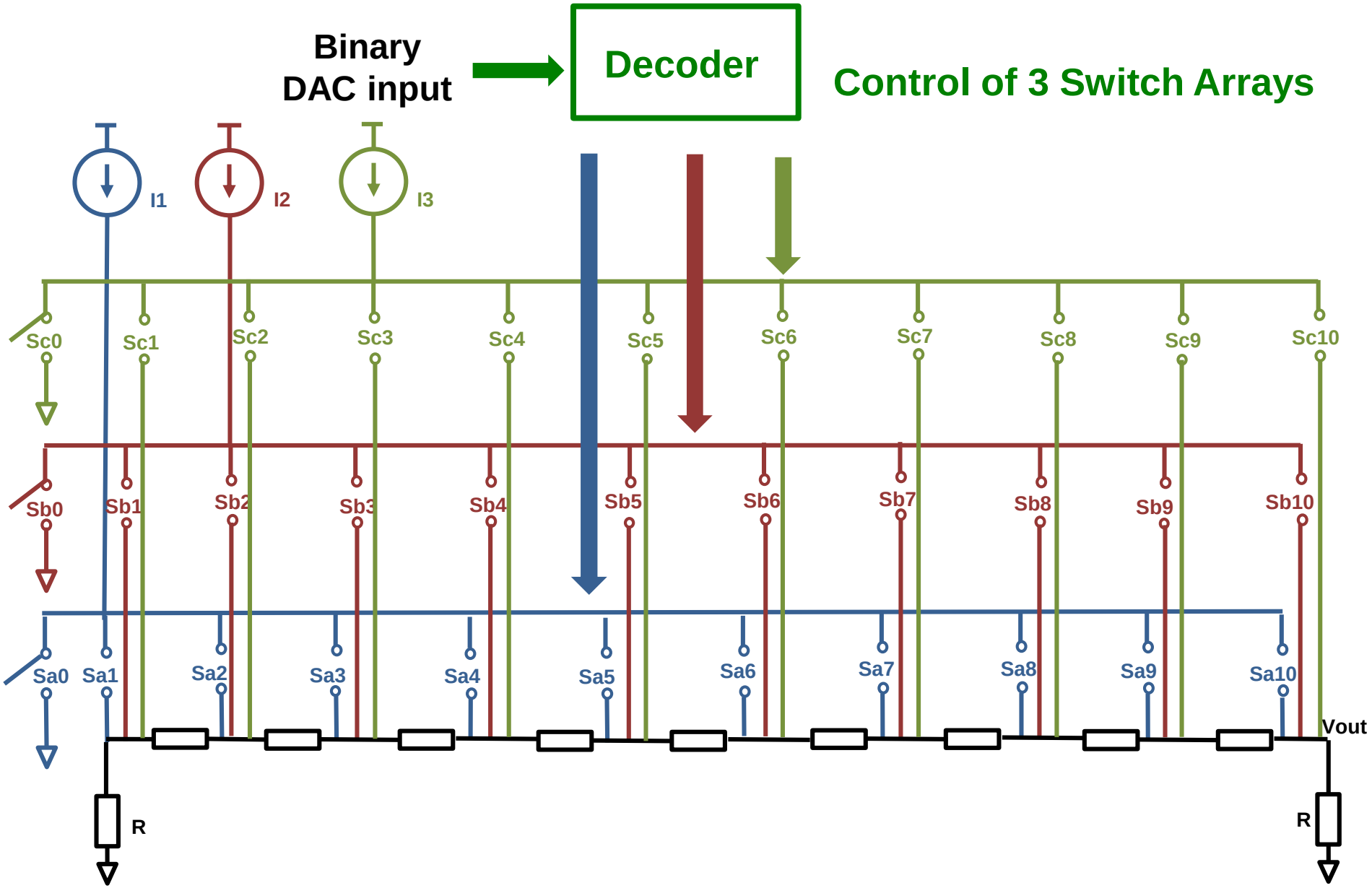


Vout53= Vout10+ Vout15 + Vout28

= 10I*R/121 +15I*R/121 +28I*R/121

=53I*R/121

Three Switch Arrays and Decoder

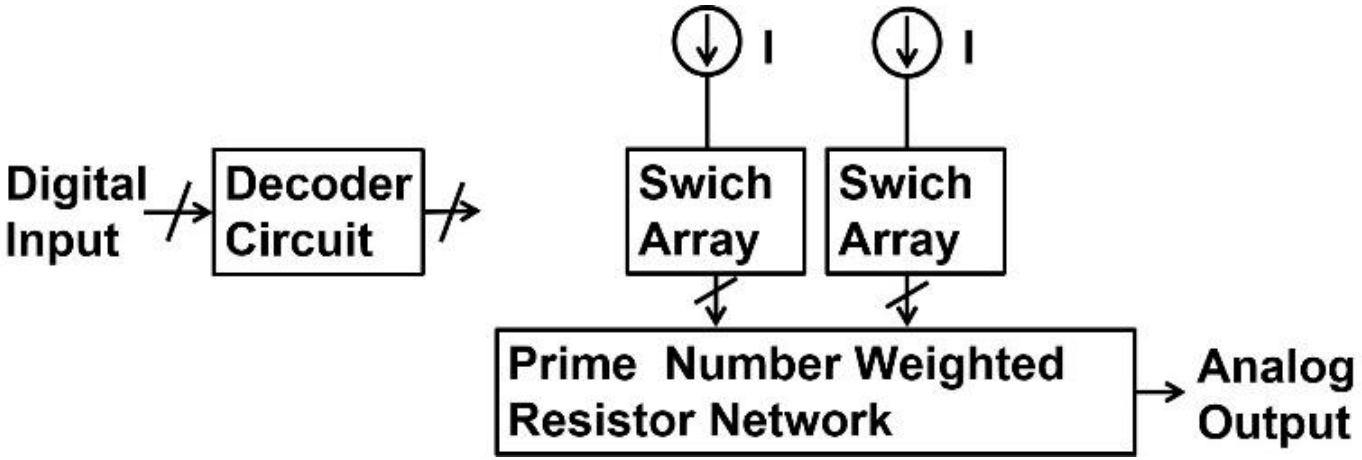


Contents

[5] X. Bai, Y. Du, M. T. Tran, A. Kuwana, H. Kobayashi,
"Digital-to-Analog Converter Architectures Based on Goldbach Conjecture for Prime Numbers in Mixed-Signal ULSI",
30th International Workshop on Post-Binary ULSI Systems (May 2021).

Research Objective

- Prime number DAC architecture
  with only 2 current sources (minimum analog circuitry)
  for any resolution
  ⇒ Suitable for advanced digital-oriented CMOS ULSI.
- Composed of a prime number weighted resistor network,
  2 current sources, 2 switch arrays, a decoder.



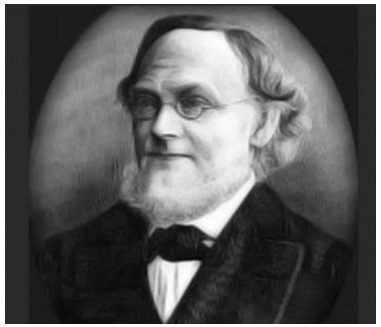
Goldbach's Conjecture

All even numbers can be represented by sum of two prime numbers.

+	2	3	5	7	11	13	17	19
2	4	5	7	9	13	15	19	21
3	5	6	8	10	14	16	20	22
5	7	8	10	12	16	18	22	24
7	9	10	12	14	18	20	24	26
11	13	14	16	18	22	24	28	30
13	15	16	18	20	24	26	30	32
17	19	20	22	24	28	30	34	36
19	21	22	24	26	30	32	36	38

Prime number

Prime number



Christian Goldbach
1690-1764

Not proven yet !

Prime Numbers and Even Numbers

Prime numbers:

2, 3, 5, 7, 11, 13, 17, 19, 23, 29, ……

All even numbers are represented by two prime numbers

2:	**2**
4:	**2+2**
6:	**3+3**
8:	**3+5**
10:	**3+7**
12:	**5+7**
14:	**7+7**
16:	**5+11**
18:	**7+11**
20:	**7+13**
22:	**11+11**
24:	**11+13**
26:	**13+13**
28:	**11+17**
30:	**13+17**
32:	**13+19**
34:	**17+17**
36:	**17+19**
38:	**19+19**
40:	**17+23**
42:	**19+23**
44:	**13+31**
46:	**23+23**
48:	**19+29**
50:	**19+31**
52:	**23+29**
54:	**23+31**
56:	**19+37**
58:	**29+29**
60:	**29+31**

Digital Input with Sum of 2 Prime Numbers

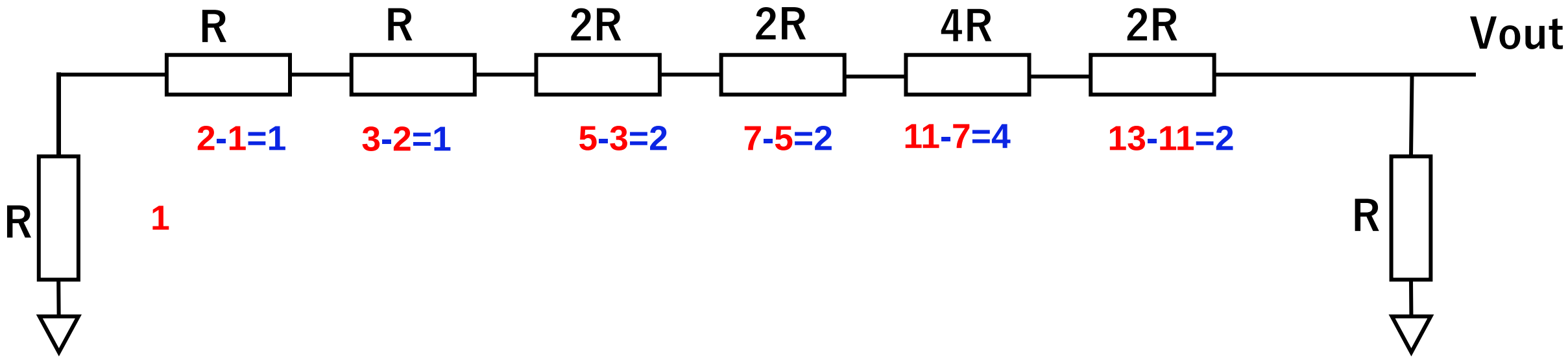
- All the digital inputs of DAC can correspond to an even number by sum of two prime numbers.

DAC input

0:0=0+0	16:32=13+19→16	32:64=23+41→32	48:96=43+53→48
1:2=2+0→1	17:34=17+17→17	33:66=23+43→33	49:98=31+67→49
2:4=1+3→2	18:36=17+19→18	34:68=31+37→34	50:100=41+59→50
3:6=3+3→3	19:38=19+19→19	35:70=29+41→35	51:102=43+59→51
4:8=3+5→4	20:40=17+23→20	36:72=29+43→36	52:104=43+61→52
5:10=3+7→5	21:42=19+23→21	37:74=31+43→37	53:106=53+53→53
6:12=5+7→6	22:44=13+31→22	38:76=29+47→38	54:108=47+61→54
7:14=7+7→7	23:46=23+23→23	39:78=31+47→39	55:110=43+67→55
8:16=5+11→8	24:48=19+29→24	40:80=19+61→40	56:112=53+59→56
9:18=7+11→9	25:50=19+31→25	41:82=41+41→41	57:114=53+61→57
10:20=7+13→10	26:52=23+29→26	42:84=41+43→42	58:116=43+73→58
11:22=11+11→11	27:54=23+31→27	43:86=43+43→43	59:118=47+71→59
12:24=11+13→12	28:56=19+37→28	44:88=41+47→44	60:120=59+61→60
13:26=13+13→13	29:58=29+29→29	45:90=43+47→45	61:122=61+61→61
14:28=11+17→14	30:60=29+31→30	46:92=31+61→46	62:124=53+71→62
15:30=13+17→15	31:62=31+31→31	47:94=41+53→47	63:126=53+73→63

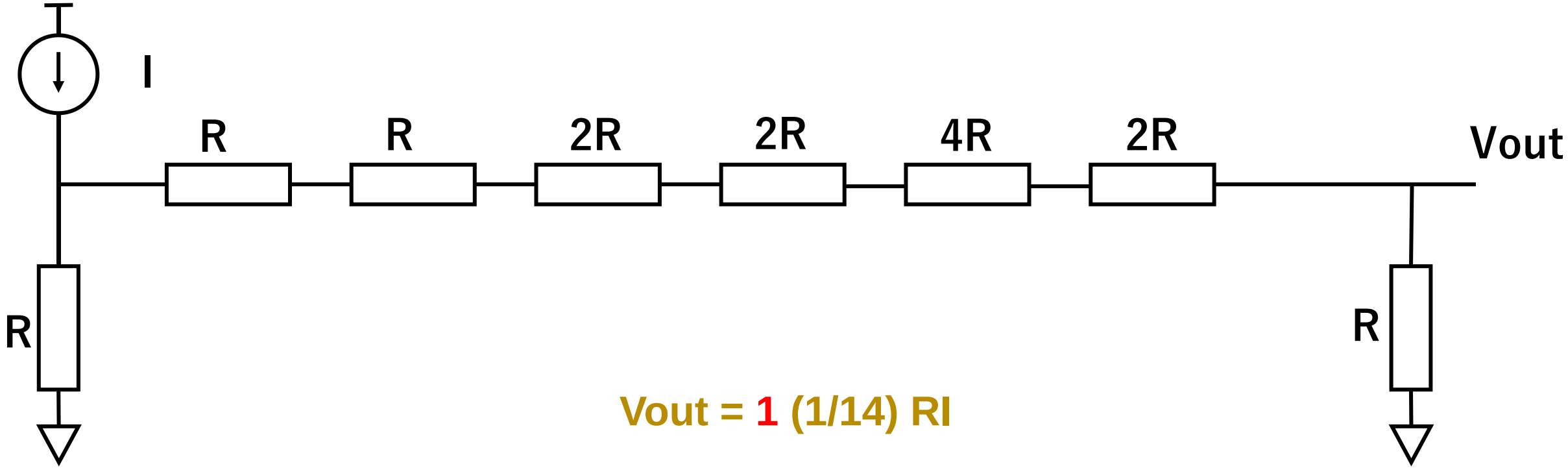
Prime Number Weighted Resistor Network

Prime numbers: 1, 2, 3, 5, 7, 11, 13, 17, 19, 23, 29, ……



Proposed Prime Number DAC Operation (1)

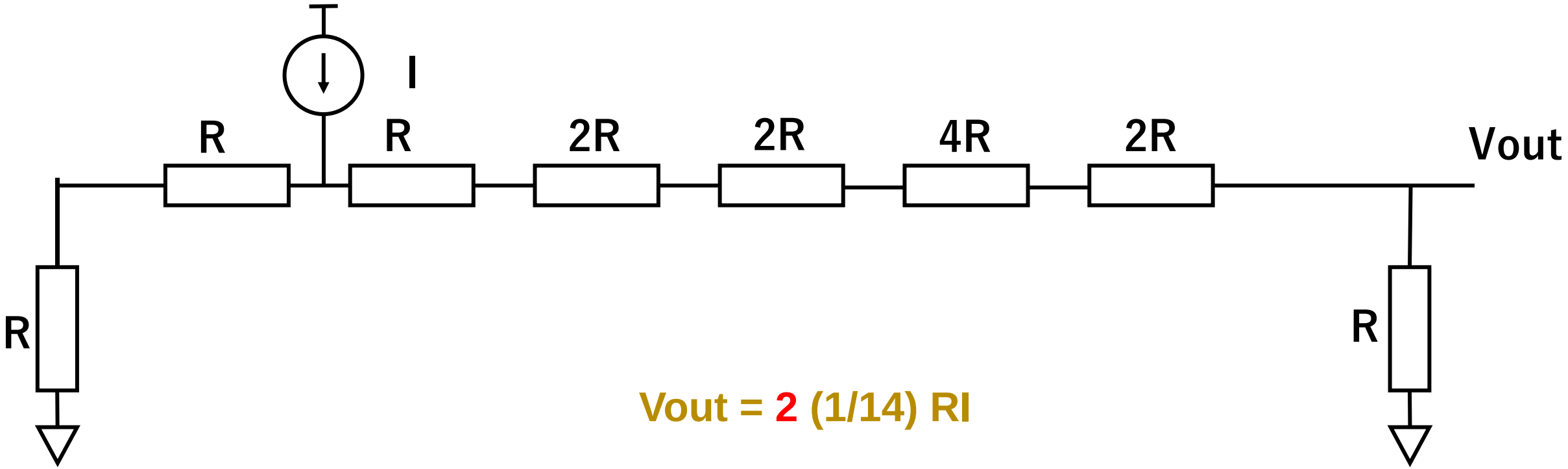
Prime numbers: 1, 2, 3, 5, 7, 11, 13, 17, 19, 23, 29, ……



Vout = 1 (1/14) RI

Proposed Prime Number DAC Operation (2)

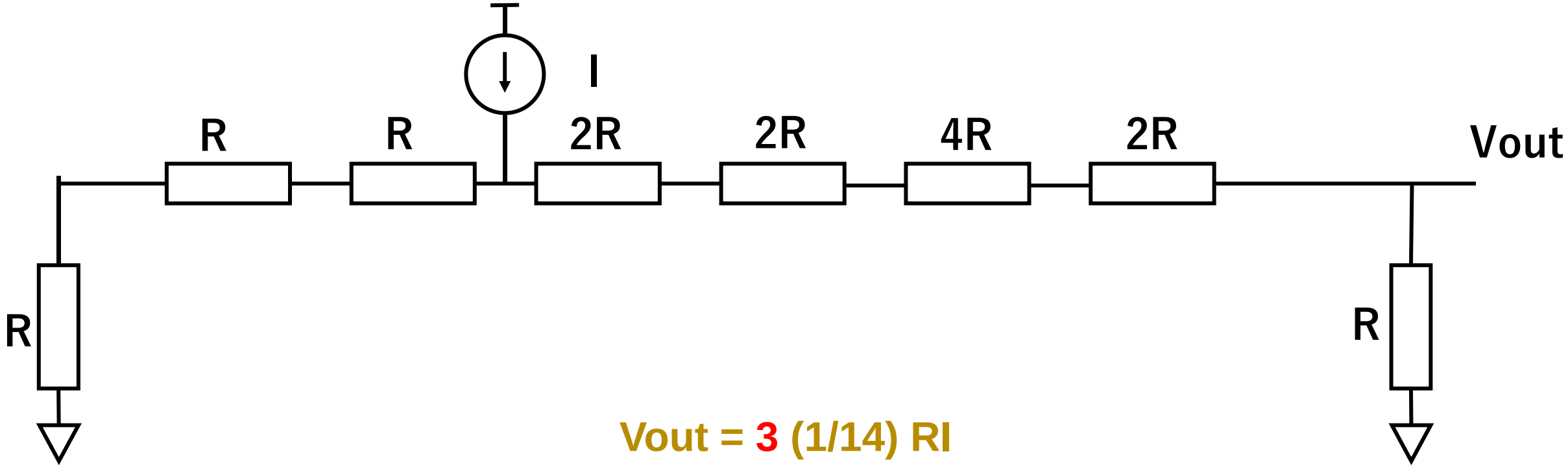
Prime numbers: 1, 2, 3, 5, 7, 11, 13, 17, 19, 23, 29, ……



Vout = 2 (1/14) RI

Proposed Prime Number DAC Operation (3)

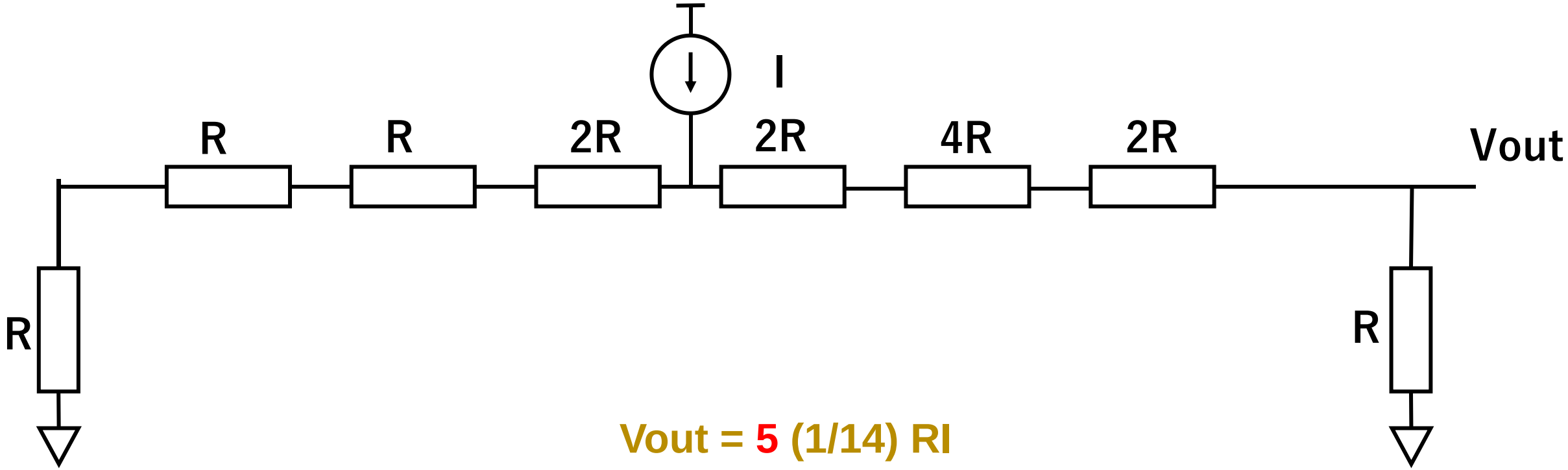
Prime numbers: 1, 2, 3, 5, 7, 11, 13, 17, 19, 23, 29, ……



Vout = 3 (1/14) RI

Proposed Prime Number DAC Operation (4)

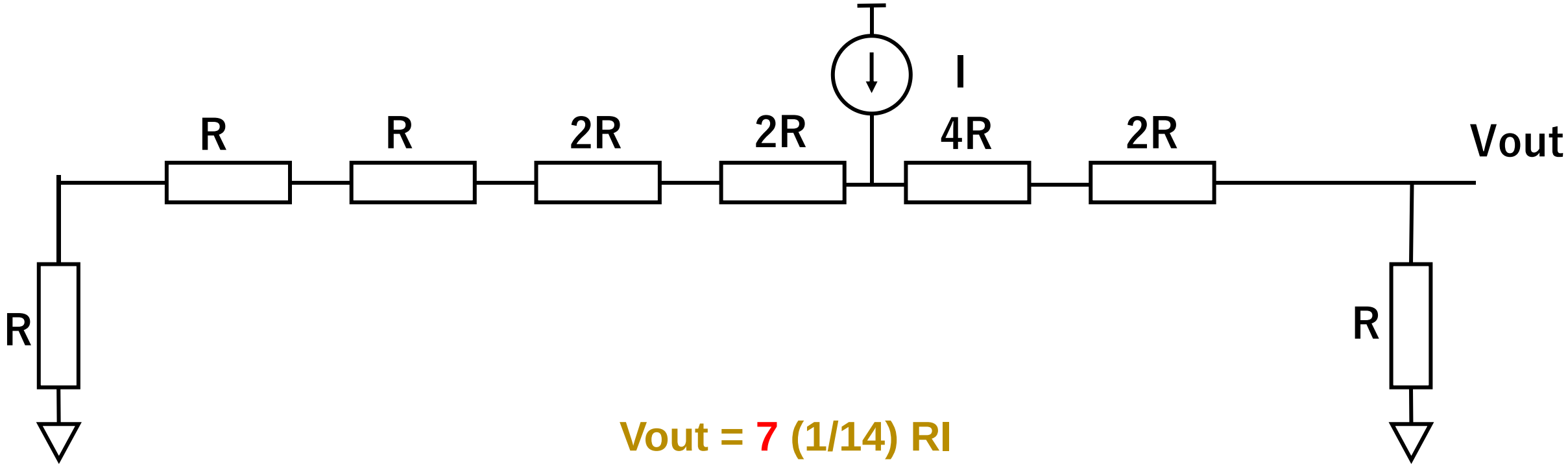
Prime numbers: 1, 2, 3, 5, 7, 11, 13, 17, 19, 23, 29, ……



Vout = 5 (1/14) RI

Proposed Prime Number DAC Operation (5)

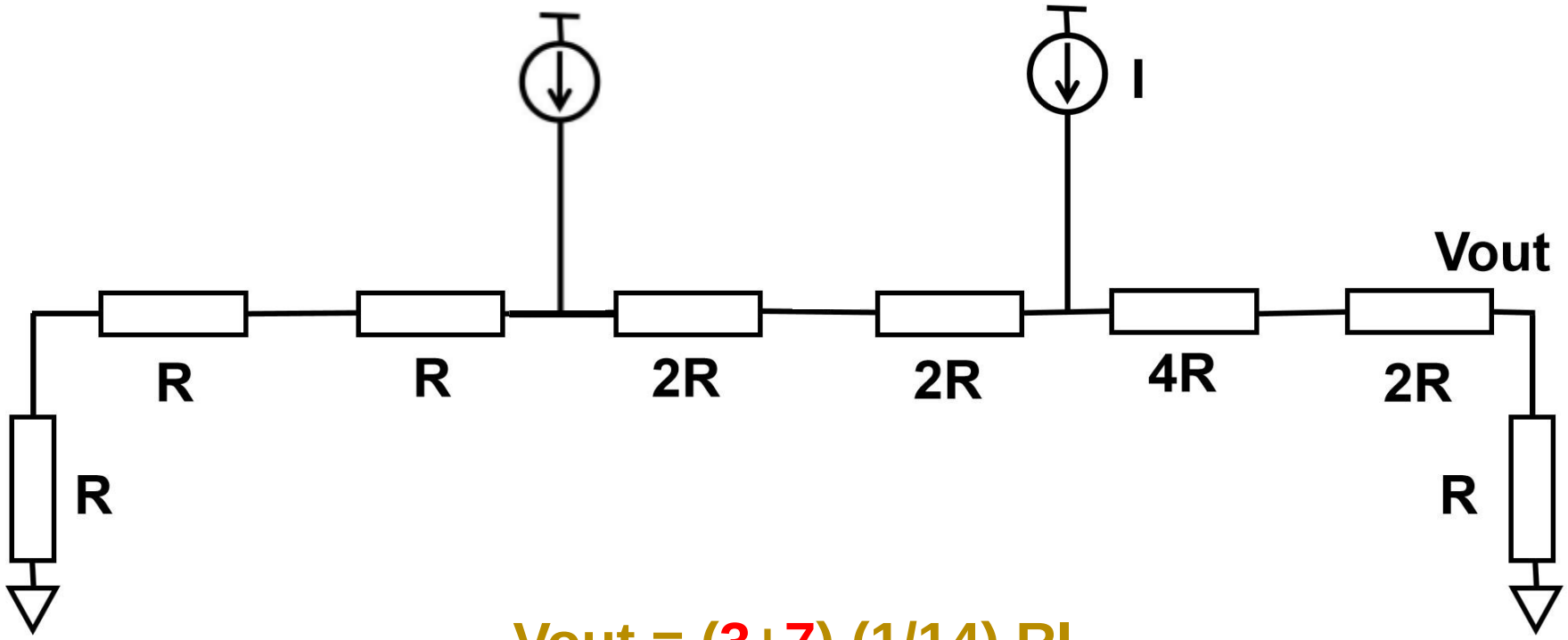
Prime numbers: 1, 2, 3, 5, 7, 11, 13, 17, 19, 23, 29, ……



Vout = 7 (1/14) RI

Prime Number DAC Operation for digital input = 5

Prime numbers: 1, 2, 3, 5, 7, 11, 13, 17, 19, 23, 29, ……

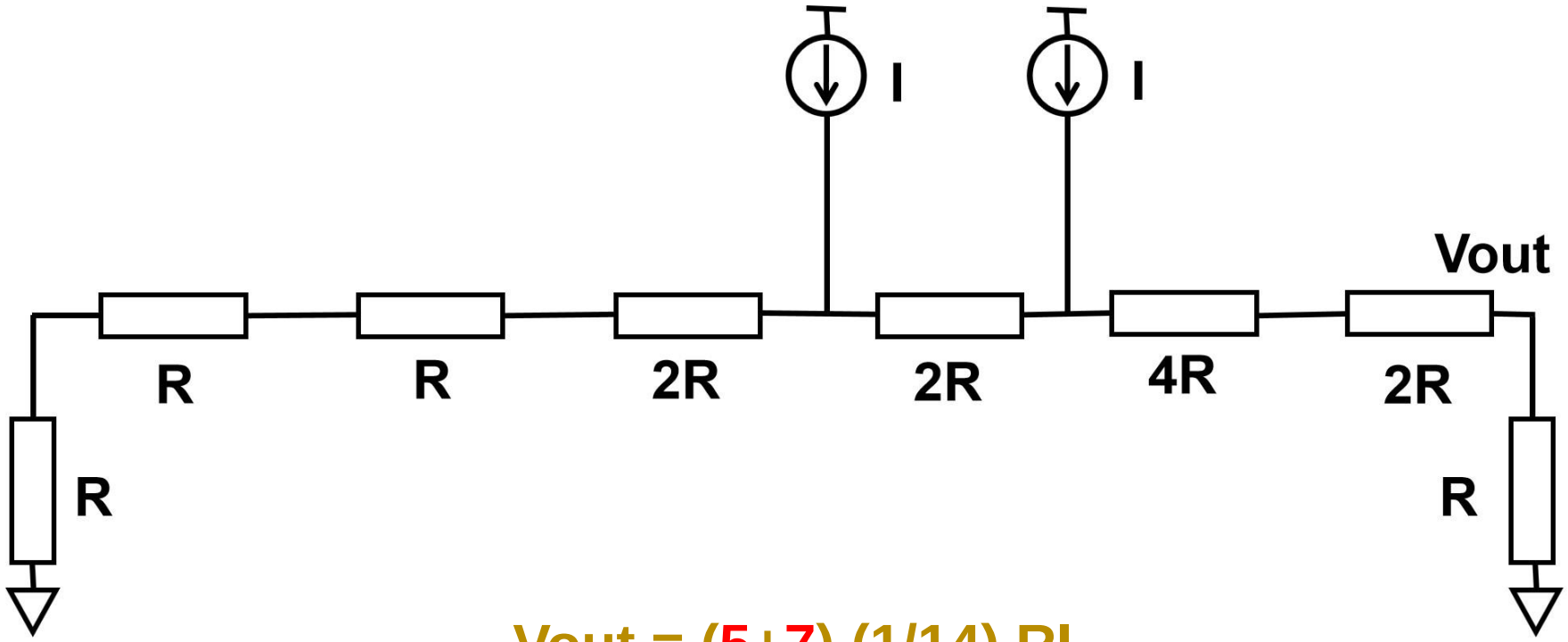


Vout = (3+7) (1/14) RI

= 5 (1/7) RI

Prime Number DAC Operation for digital input = 6

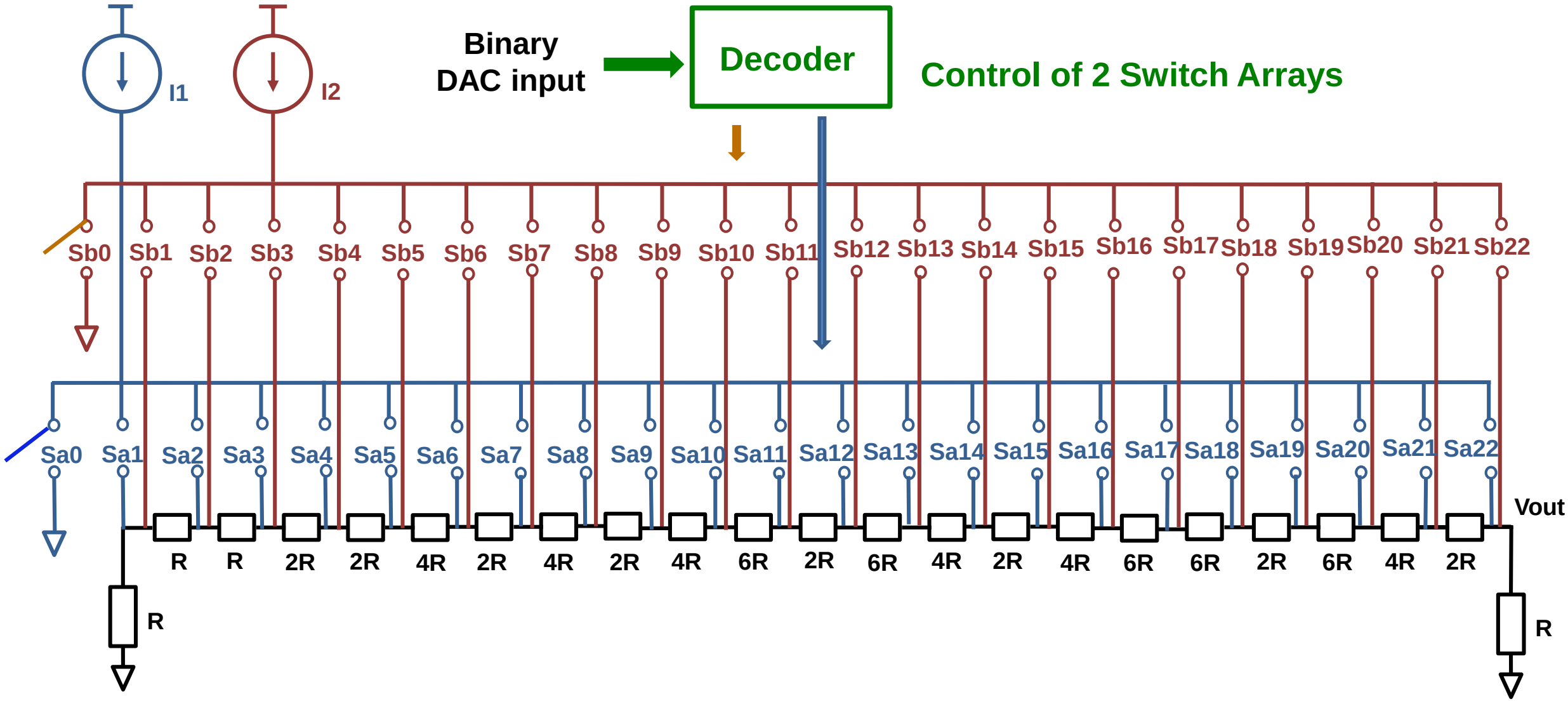
Prime numbers: 1, 2, 3, 5, 7, 11, 13, 17, 19, 23, 29, ……



Vout = (5+7) (1/14) RI

= 6 (1/7) RI

Two Switch Arrays and Decoder



Lesson from Integer Theory DACs

We could come up with
completely new DAC architectures
based on integer theory.

Polygonal numbers, Prime numbers

Euclid

Leonhard Euler
1707 - 1783

Srinivasa Aiyangar Ramanujan
1887 - 1920

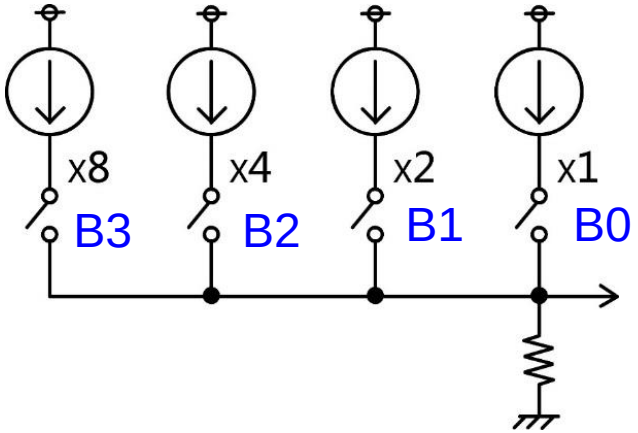
Contents

[9] R. Jiang, G. Adhikari, Y. Sun, D. Yao, R. Takahashi, Y. Ozawa, N. Tsukiji, H. Kobayashi, R. Shiota,
"Gray-code Input DAC Architecture for Clean Signal Generation",
IEEE International Symposium on Intelligent Signal Processing and Communication Systems, Xiamen, China (Nov. 2017)

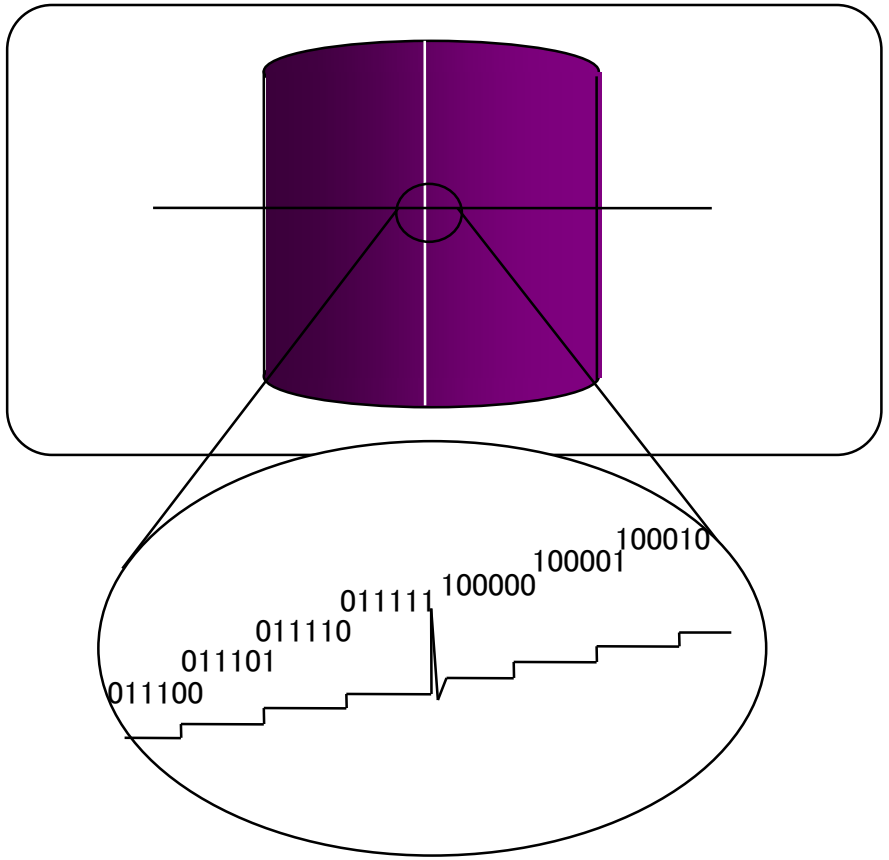
[10] G. Adhikari, R. Jiang, H. Kobayashi,
"Study of Gray Code Input DAC Using MOSFETs for Glitch Reduction",
IEEE 13th International Conference on Solid-State and Integrated Circuit Technology, Hangzhou, China (Oct 2016)

Research Background

Binary-Weighted Current-Steering DAC



Graphic display driven by DAC



Switches are driven with binary code

→ glitch

Research Objective

Objective

- DAC architecture for clean signal generation

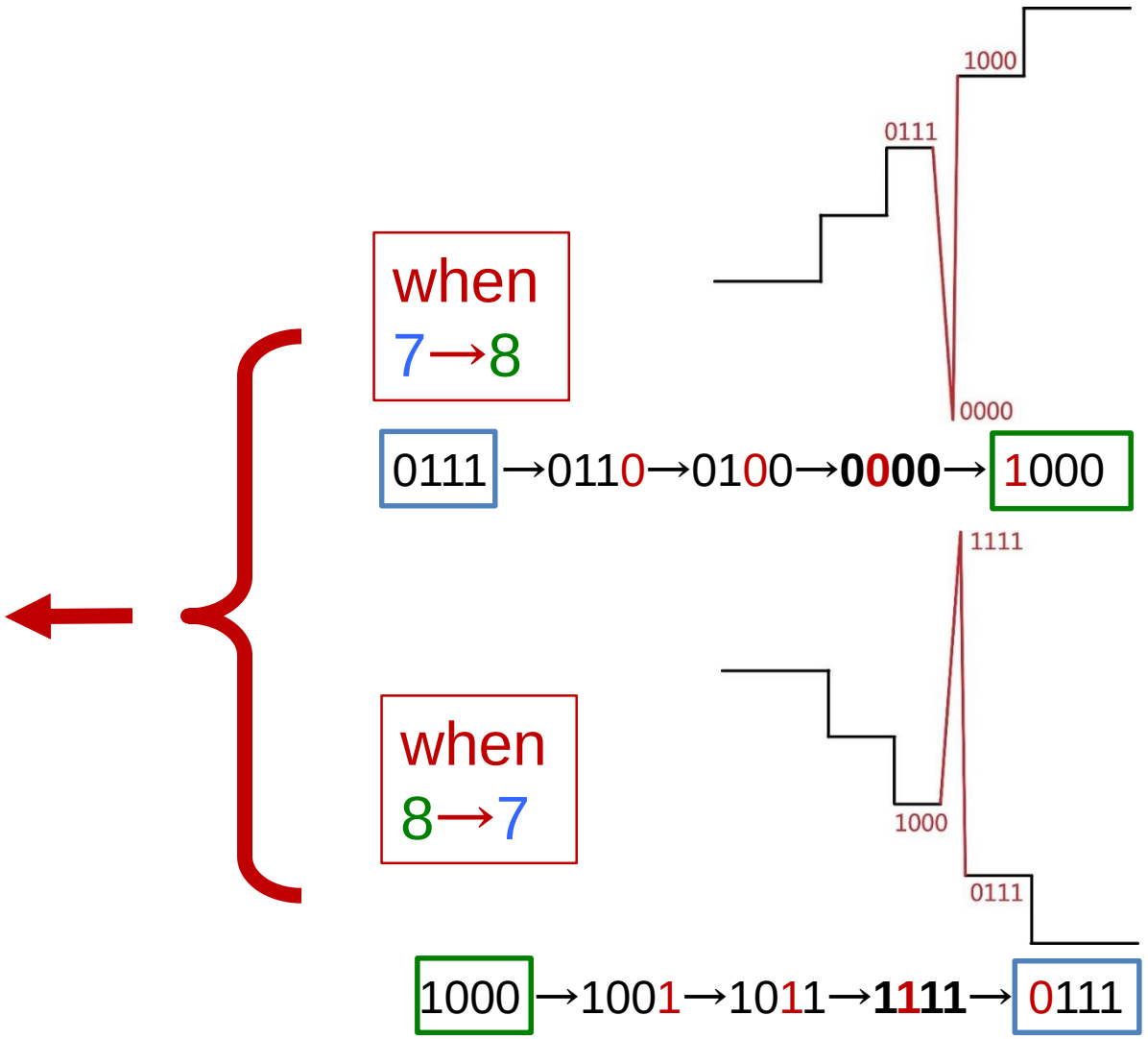
Approach

- Glitch reduction with Gray-code input topology

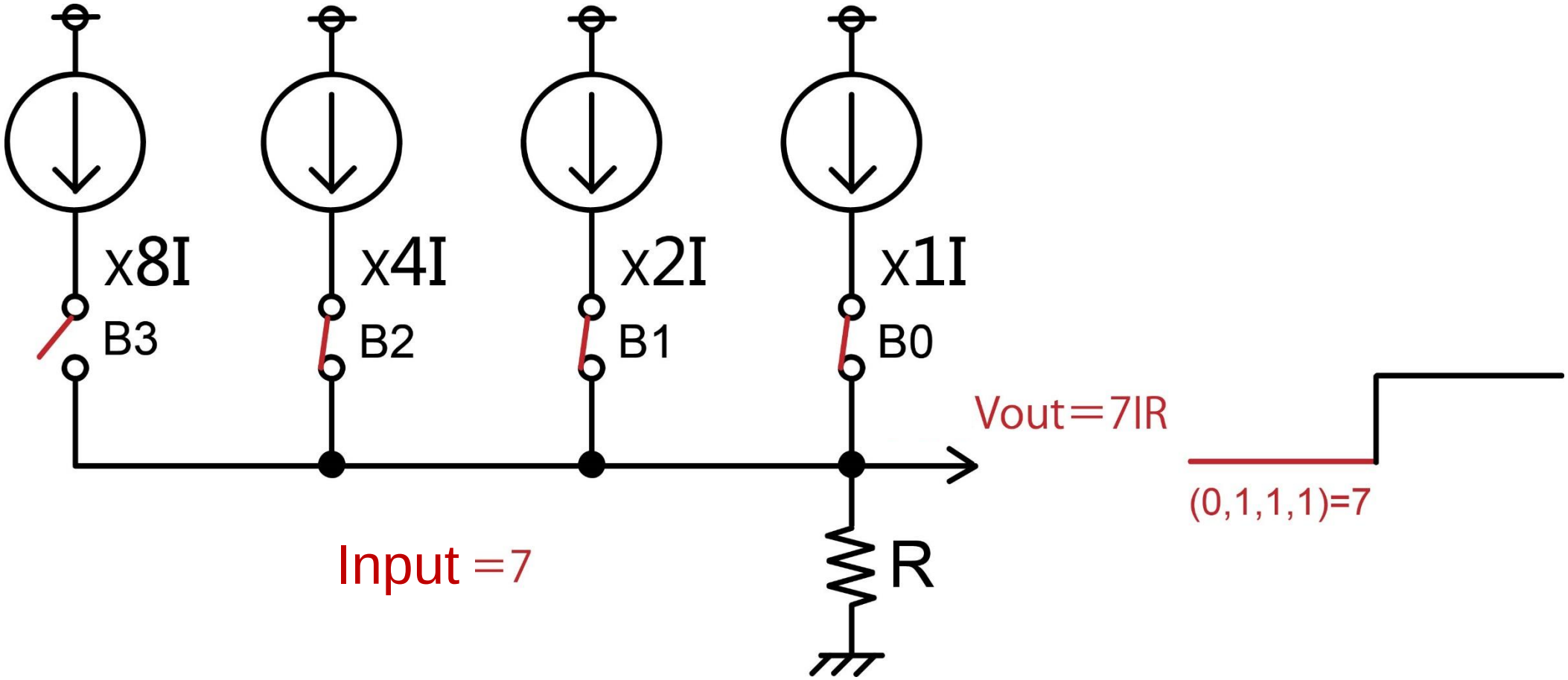
What is Glitch ?

- Output voltage spike
- Reason for glitch

Decimal numbers	Natural Binary code
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
10	1 0 1 0
11	1 0 1 1
12	1 1 0 0
13	1 1 0 1
14	1 1 1 0
15	1 1 1 1

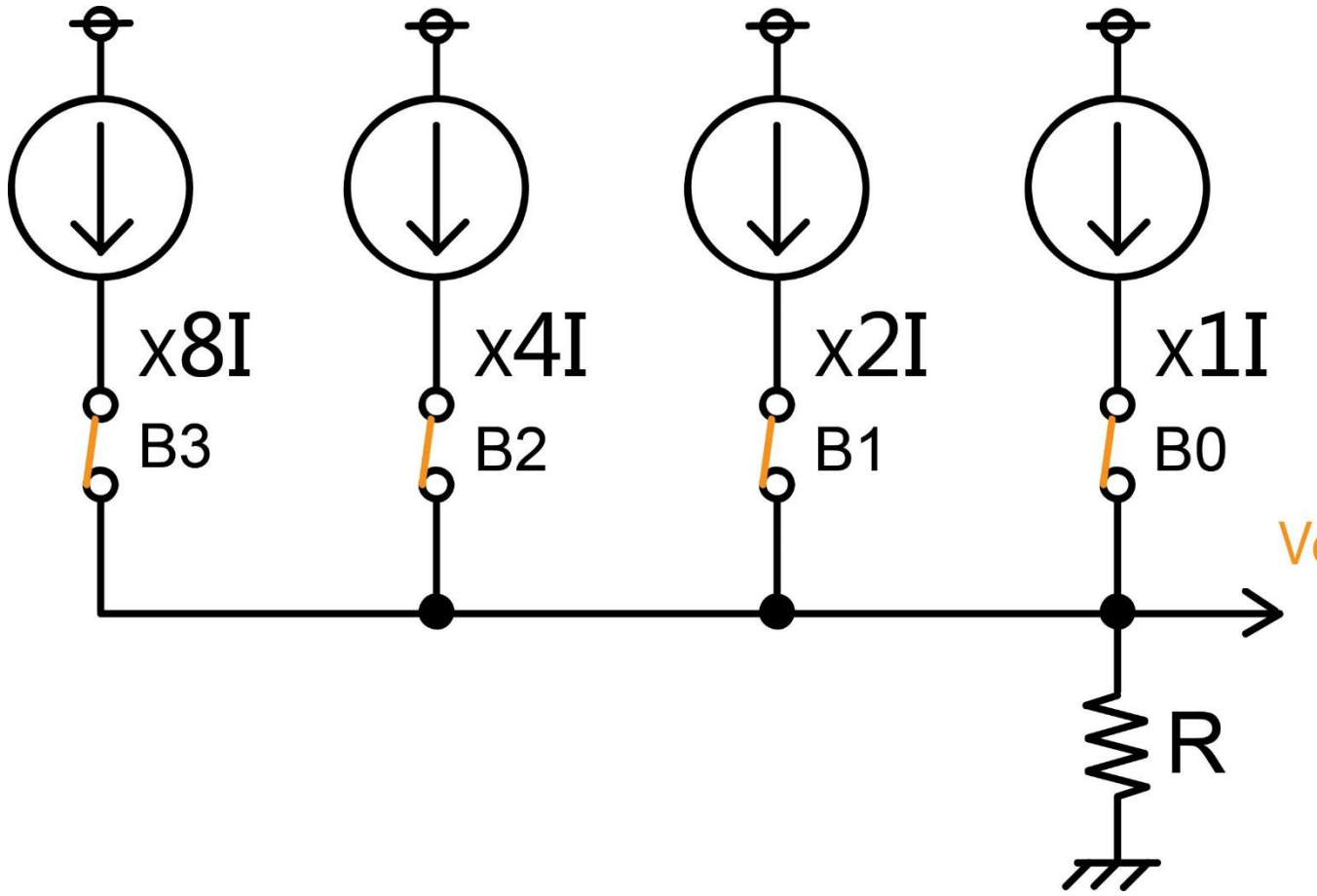


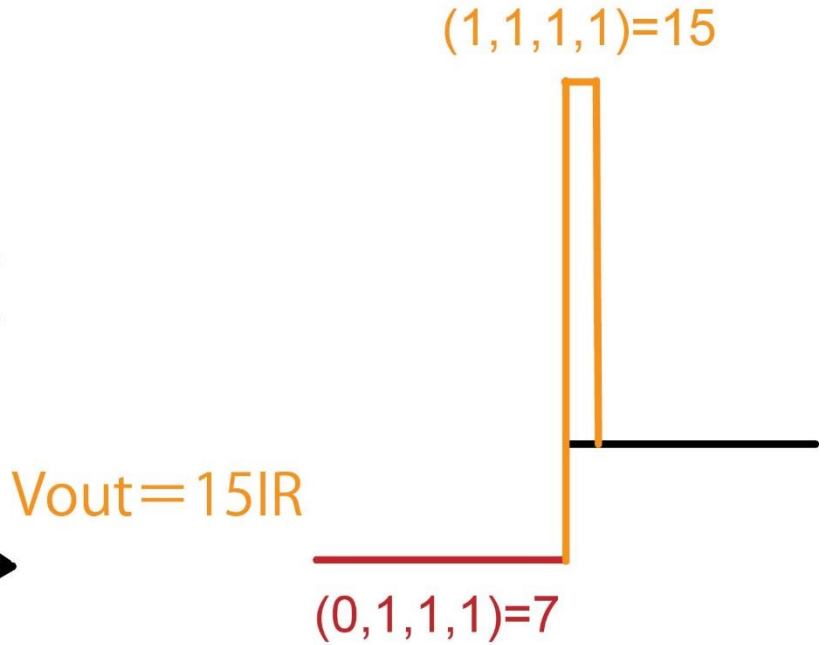
Generation of Glitch at Switching Time (7)



When the input changes 7 →8

Generation of Glitch at Switching Time (15)

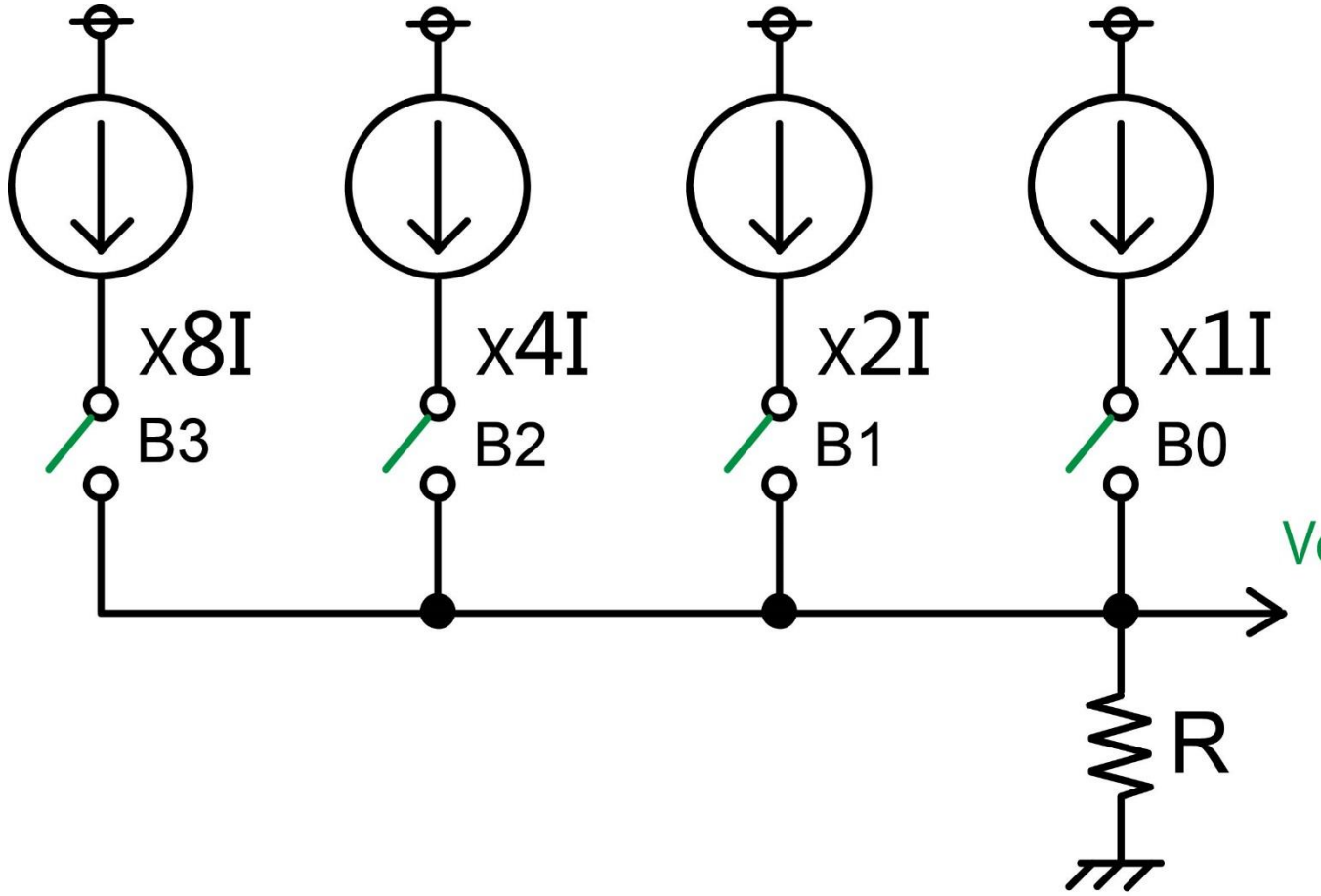




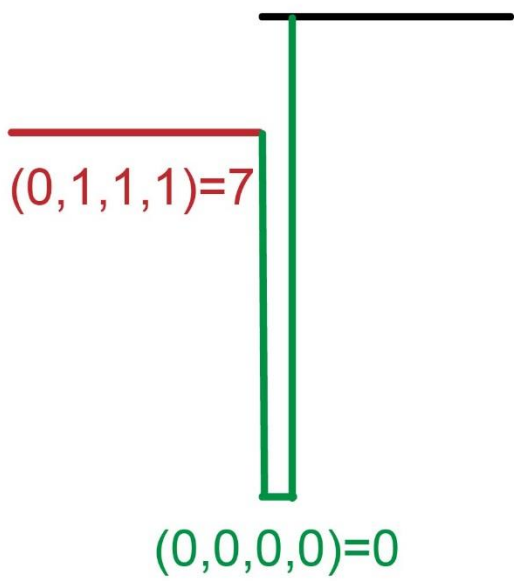
A big upward spike arises.

When B3 switches first

Generation of Glitch at Switching Time (0)

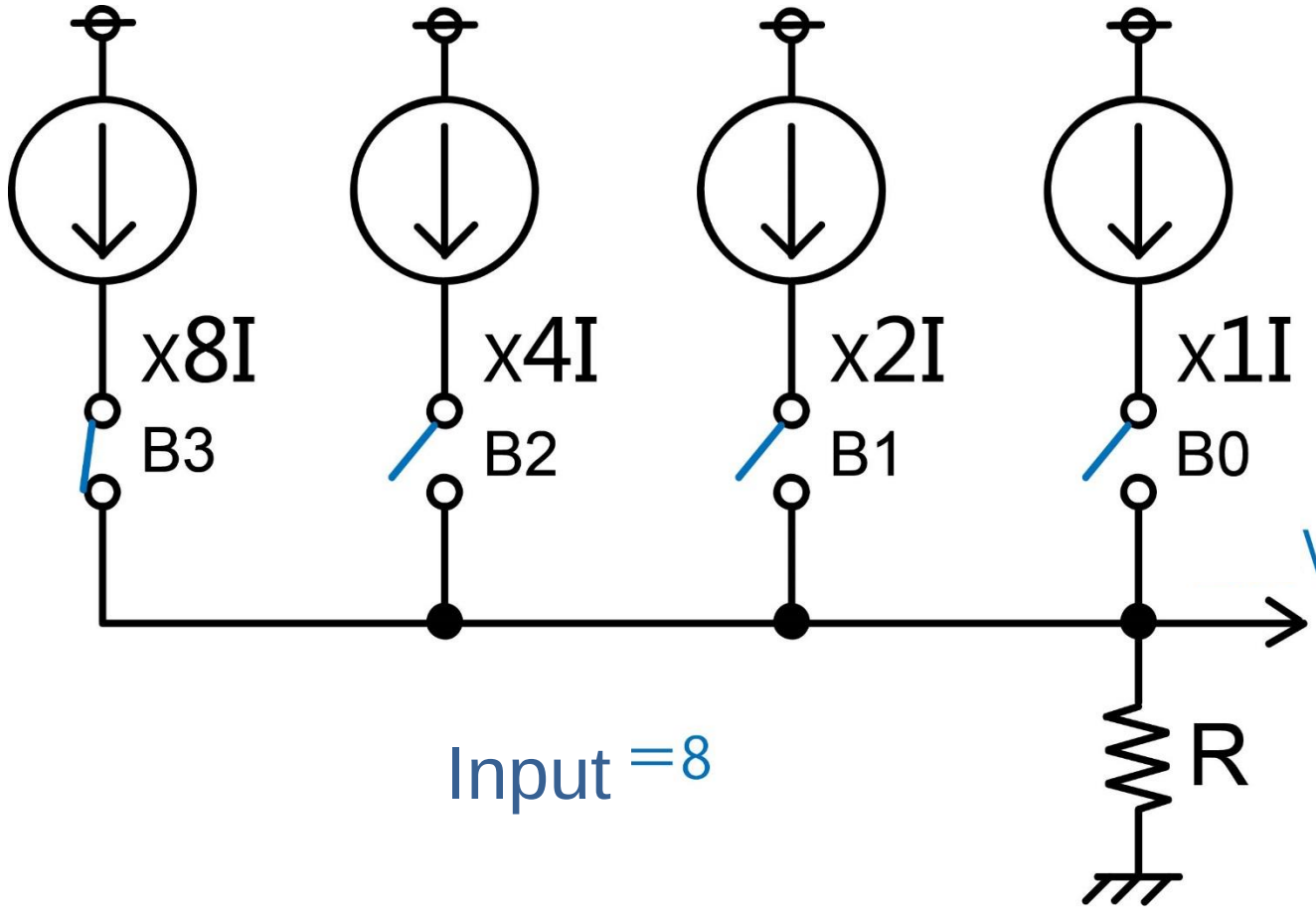


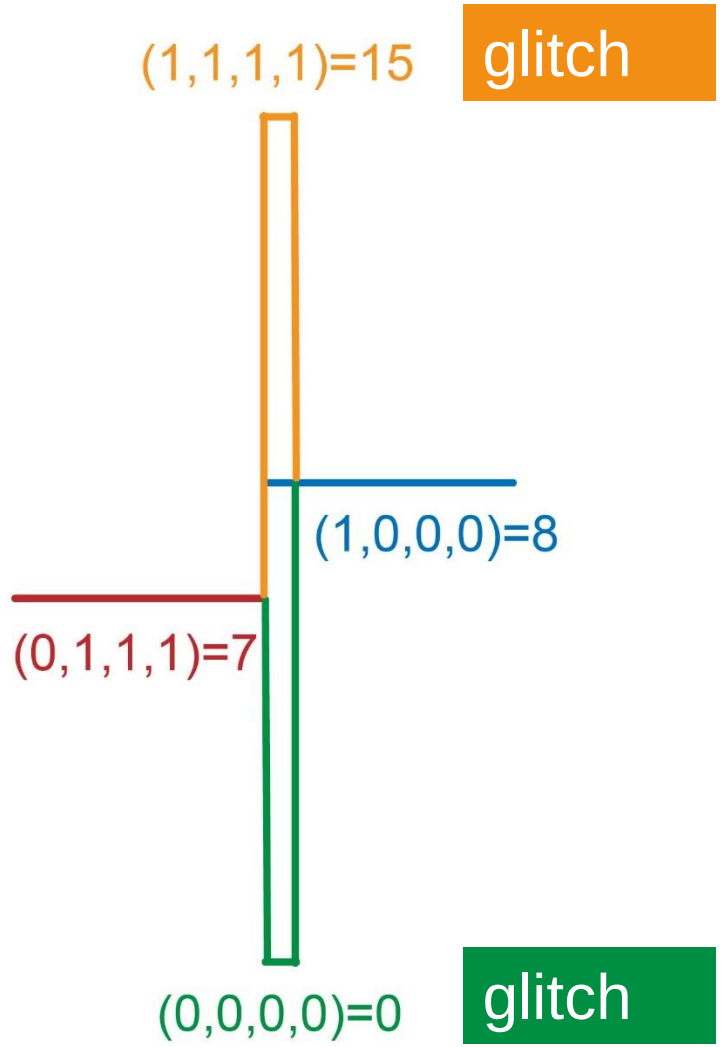
A big downward spike occurs.



When B3 switches last

Generation of Glitch at Switching Time (8)

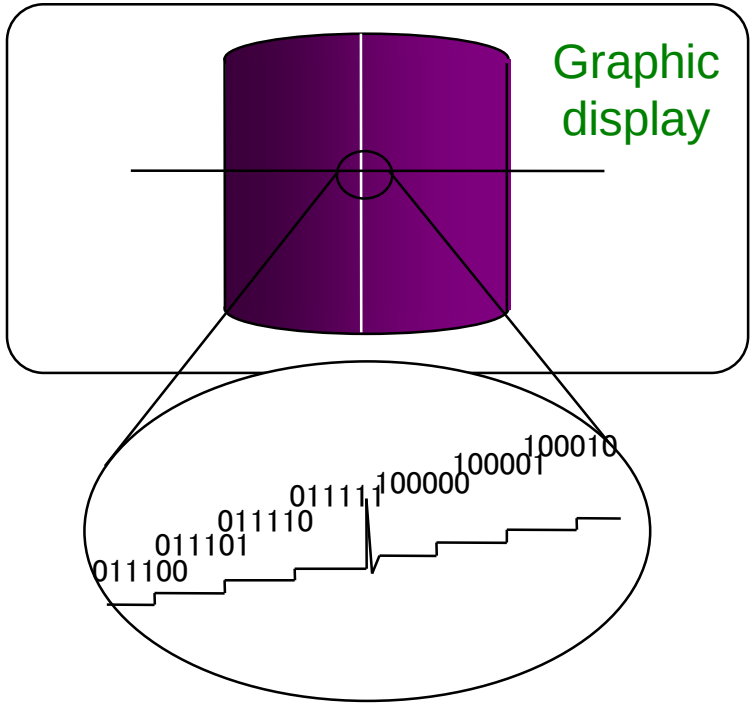




Glitch Problem and Remedy

Glitch

Serious deterioration of
graphic display and video applications



Remedy

- High-order reconstruction filter
- Track/hold circuitry at the DAC output

} Extra chip area & power

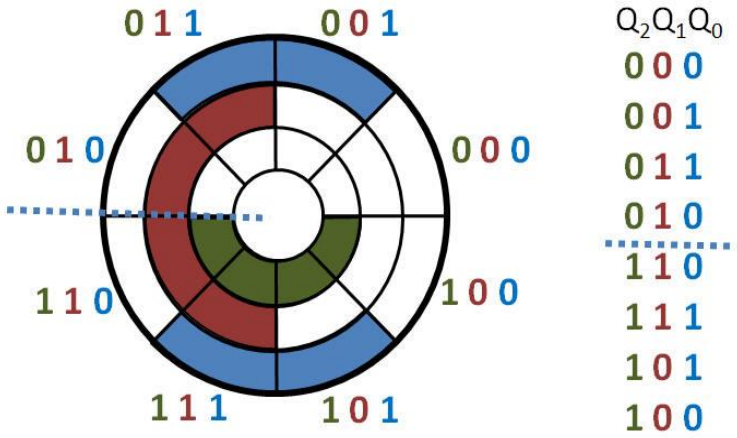
- Gray-code input DAC topology

What is Gray code ?

Gray code is a binary numeral system
where two successive values differ in only one bit.

4-bit Gray code vs. 4-bit Natural Binary Code

Decimal numbers	Natural Binary Code	4-bit Gray Code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000



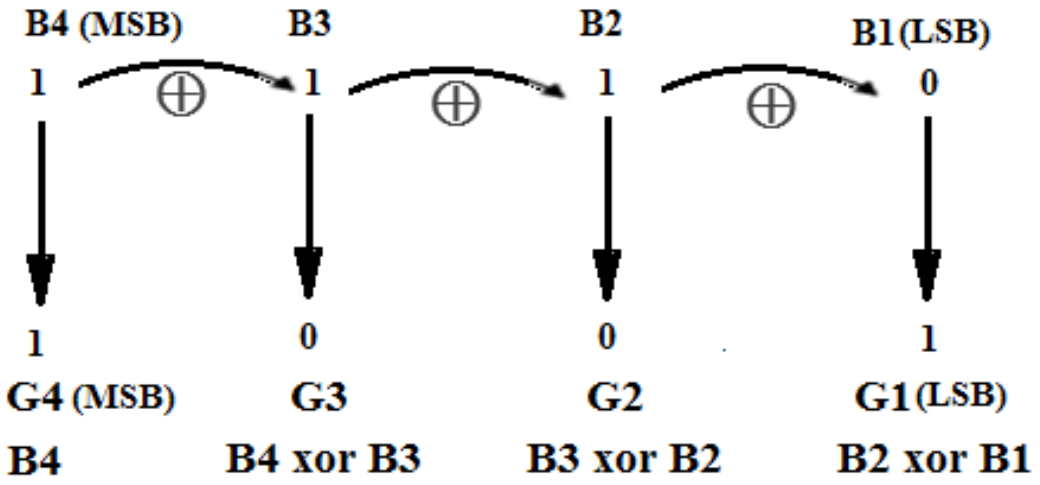
Frank Gray and A. L. Johnsrud in television booth. Behind the glass panels at sides and top are the photo-electric cells.

Gray code was invented by Frank Gray at Bell Lab in 1947.

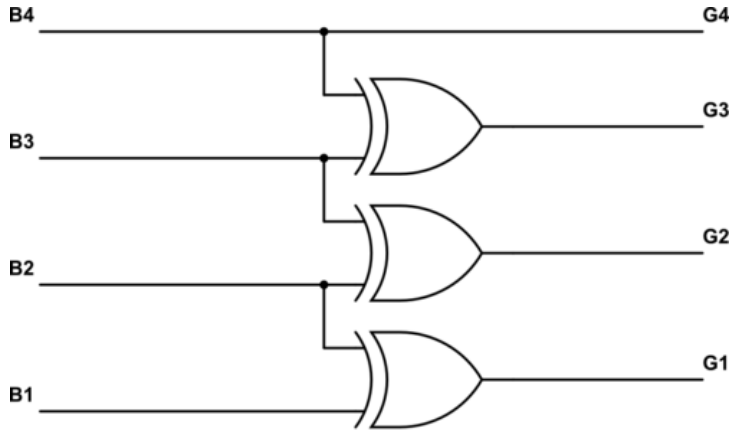
Conversion between Binary and Gray Codes

Binary to Gray code conversion

$$G_n = B_{n+1} \oplus B_n$$

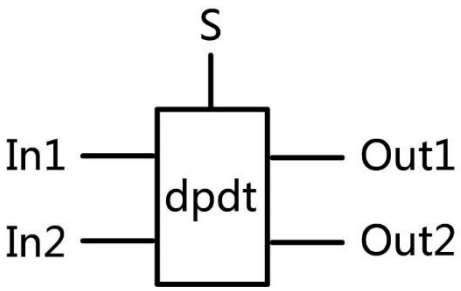


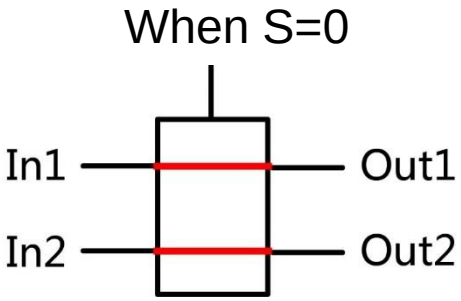
Binary to Gray code converter



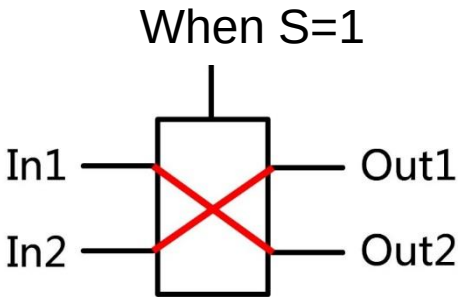
Conversion with XOR

Current/Voltage Switch Matrix

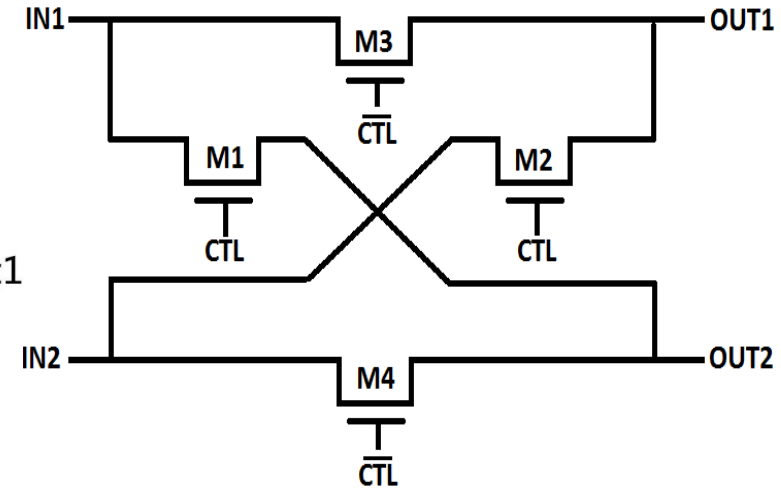


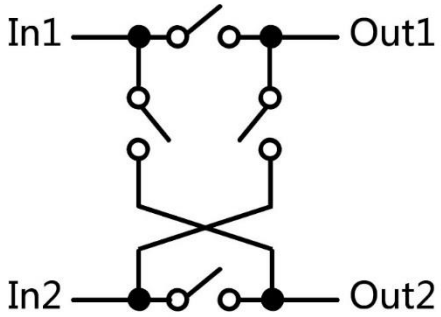


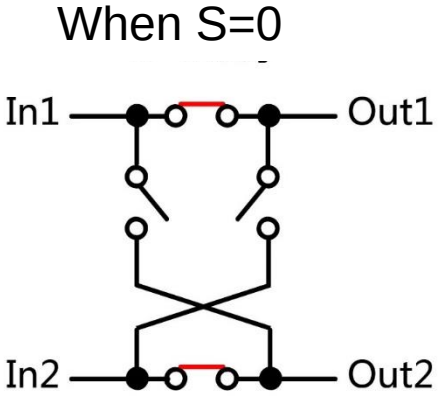
Parallel connection

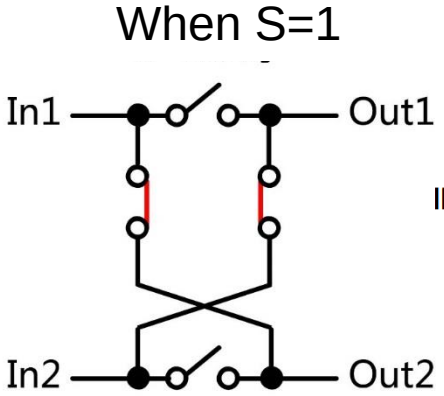


Cross connection



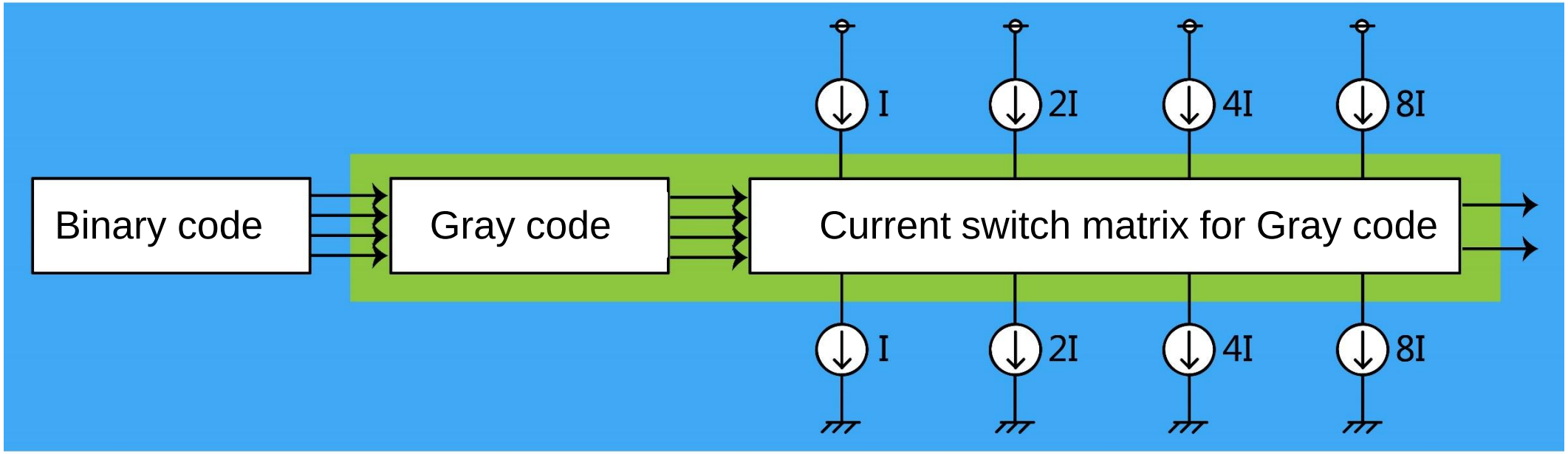






DPDT (Double-Pole Double-Throw) Switch

Proposed DAC Architecture

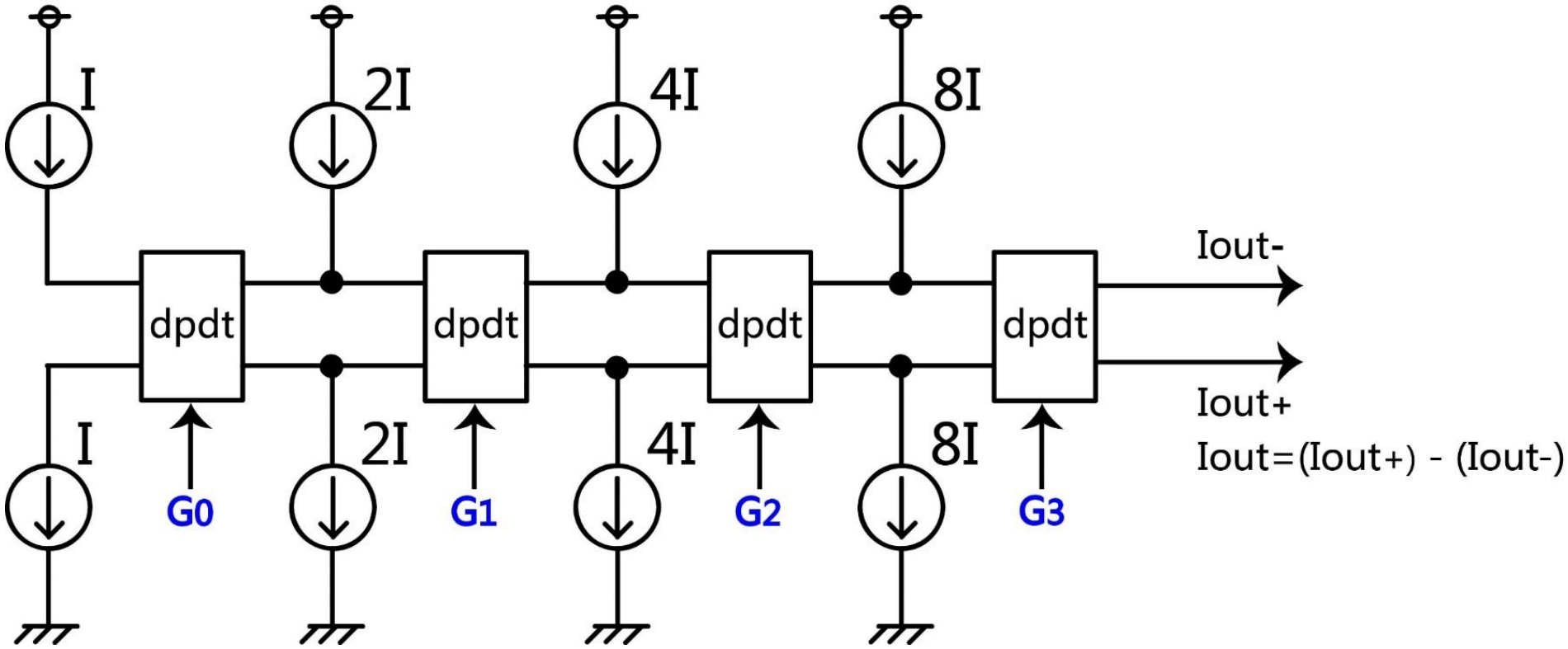


Binary code domain

Gray code domain

A long time ago, an analog IC design authority said,
“There is no Gray-code input DAC.”

Proposed Gray-code Input Current-Steering DAC

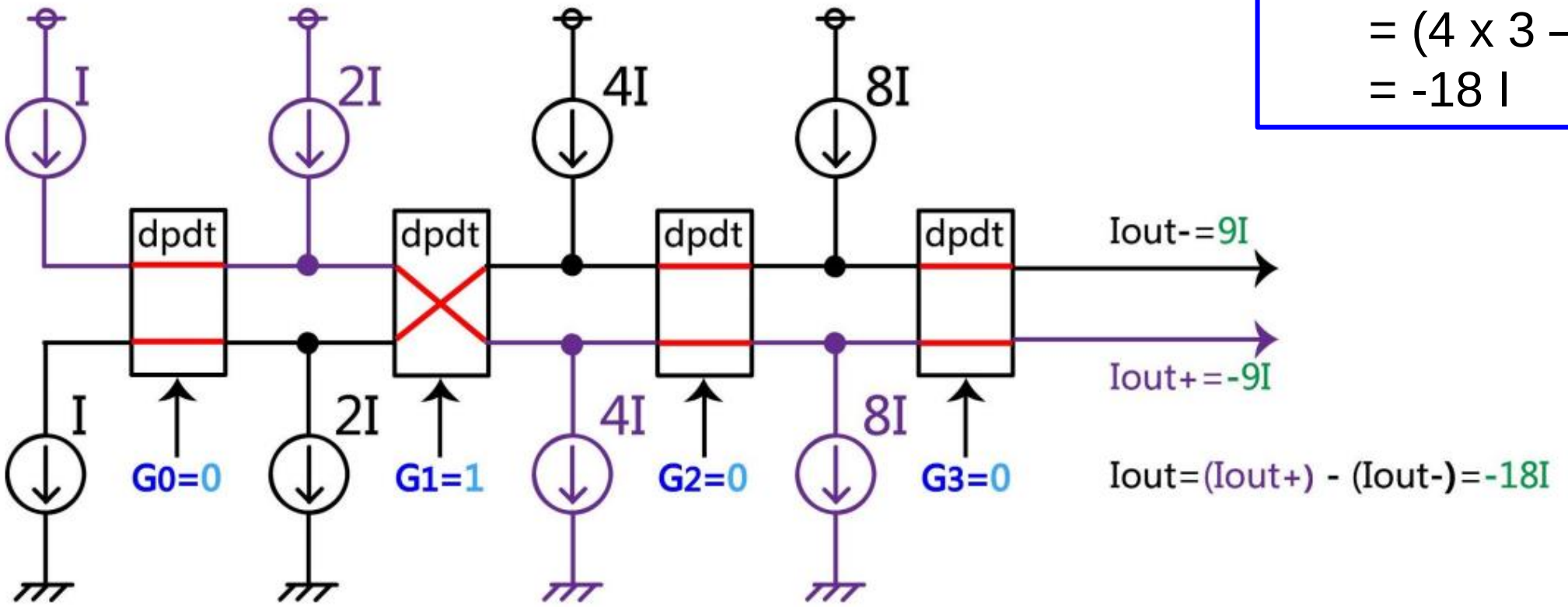


DPDT (Double-Pole Double-Throw) Switch

Gray-code Input Current-Steering DAC (Data=3)

eg. Data=3

Iout = (4 Data – 30) I
= (4 x 3 – 30) I
= -18 I



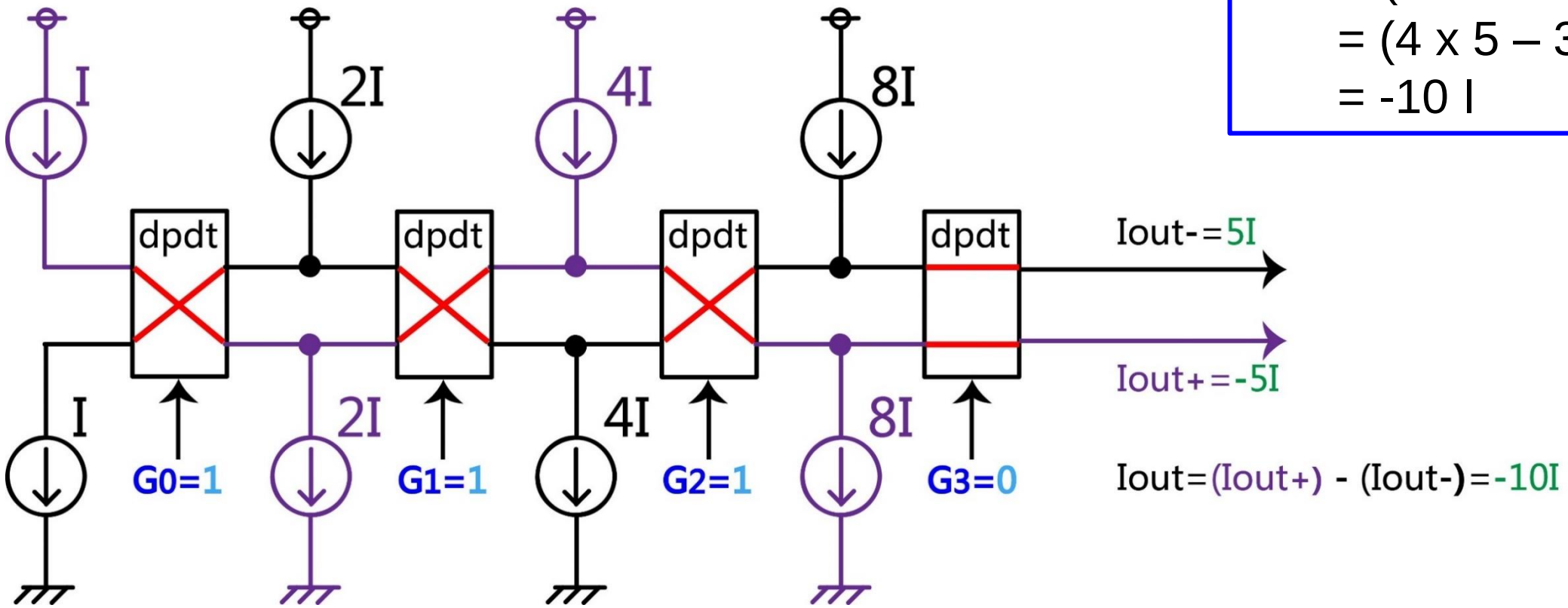
$$I_{out-} = -I - 2I + 4I + 8I = +9I$$

$$I_{out+} = +I + 2I - 4I - 8I = -9I$$

Gray-code Input Current-Steering DAC (Data=5)

eg. Data=5

Iout = (4 Data – 30) I
= (4 x 5 – 30) I
= -10 I

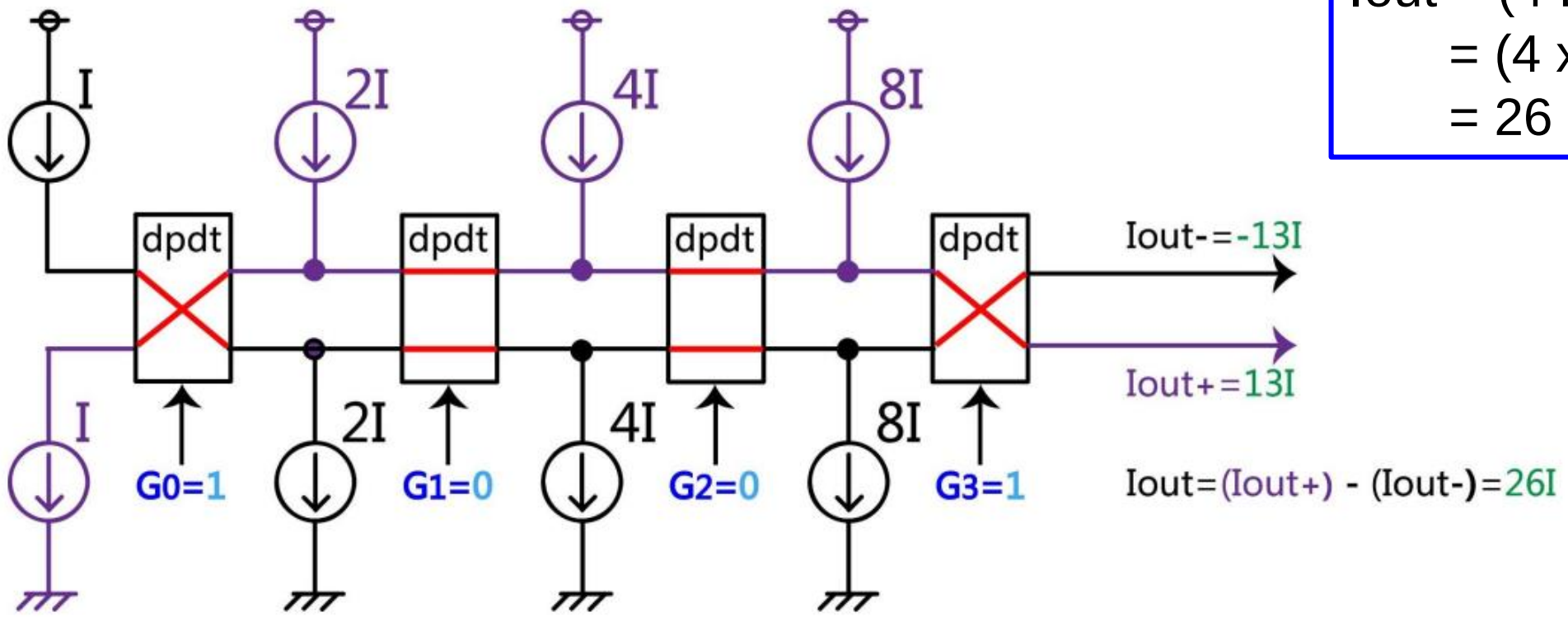


$$I_{out-} = -I + 2I - 4I + 8I = +5I$$

$$I_{out+} = -I - 2I + 4I - 8I = -5I$$

Gray-code Input Current-Steering DAC (Data=14)

eg. Data=14

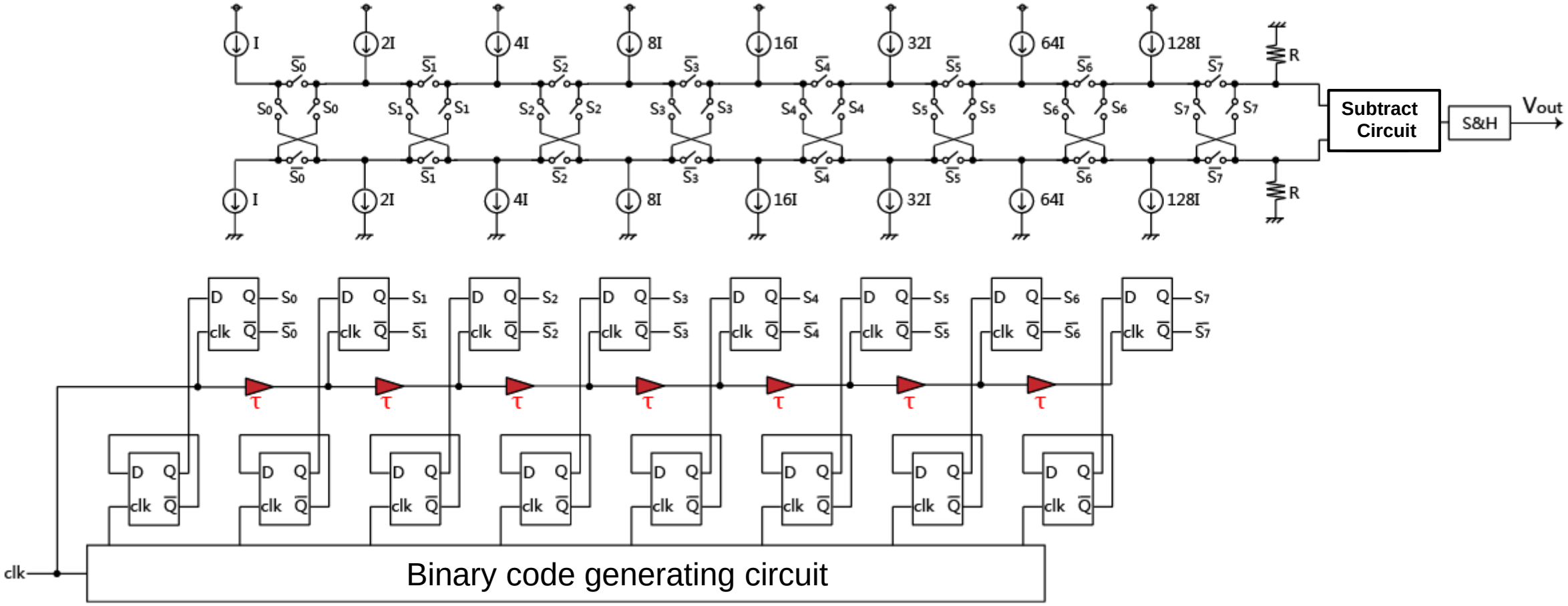


Iout = (4 Data – 30) I
= (4 x 14 – 30) I
= 26 I

$$I_{out-} = +I - 2I - 4I - 8I = -13I$$

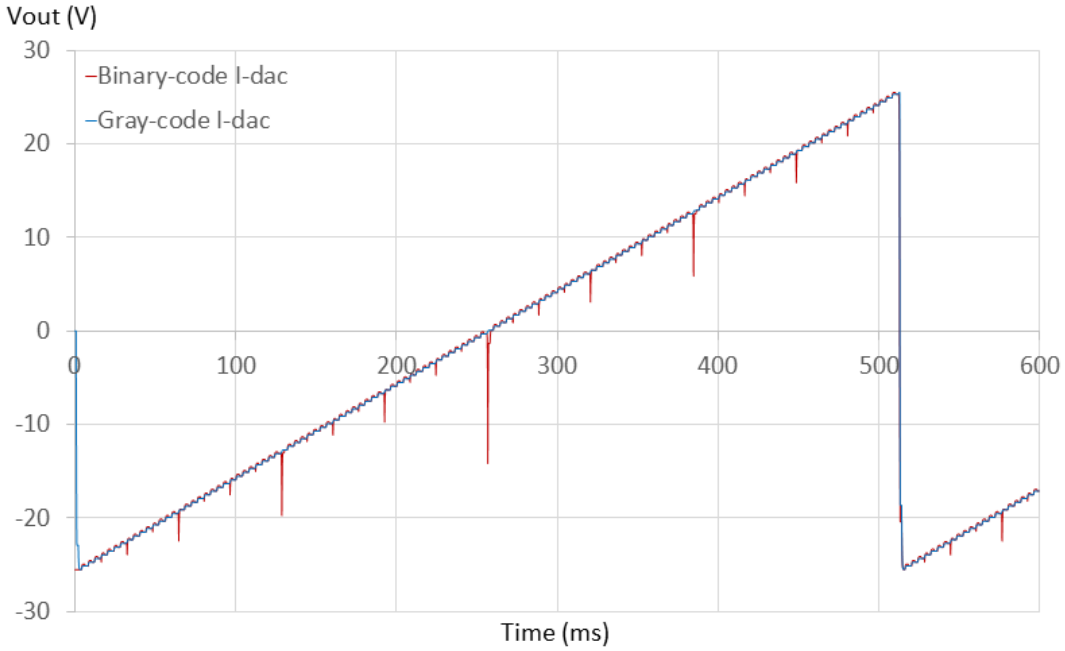
$$I_{out+} = -I + 2I + 4I + 8I = +13I$$

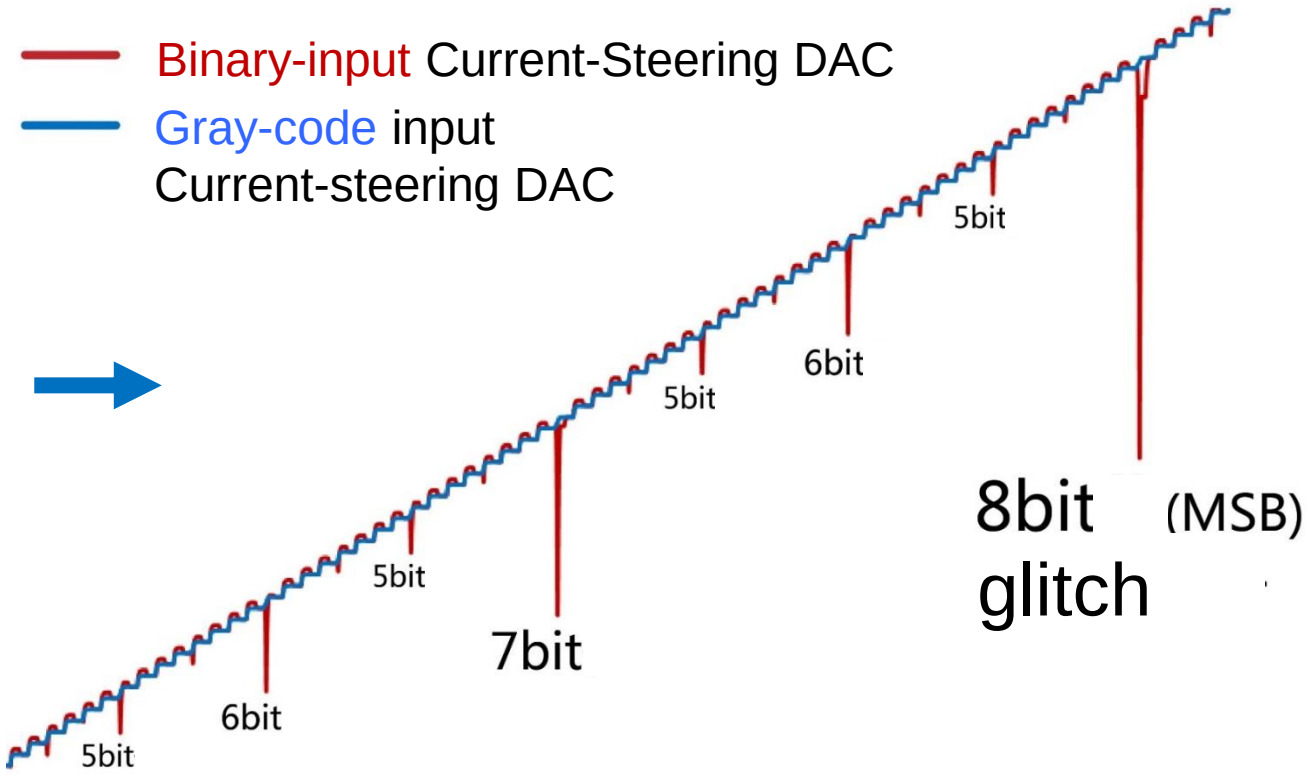
Verification of Glitch Reduction



Current-Steering Gray-code input DAC with switching delay (8bit)

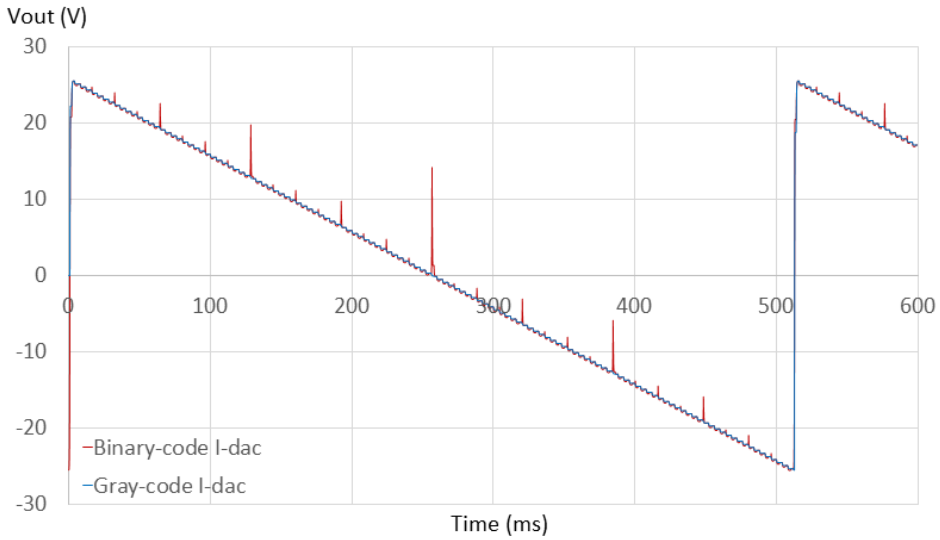
Simulation Result (Up Sweeping)

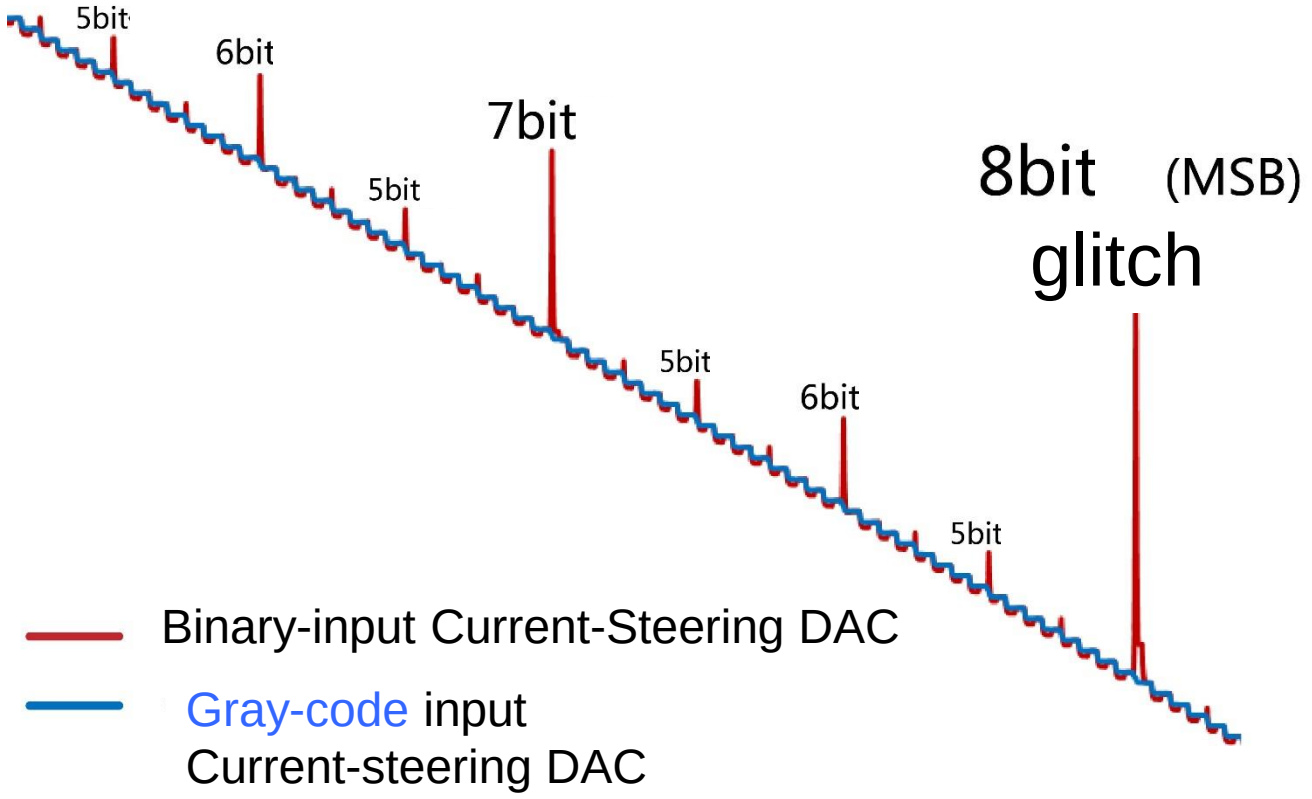




Binary-input Current-Steering DAC vs. Gray-code input current-steering DAC

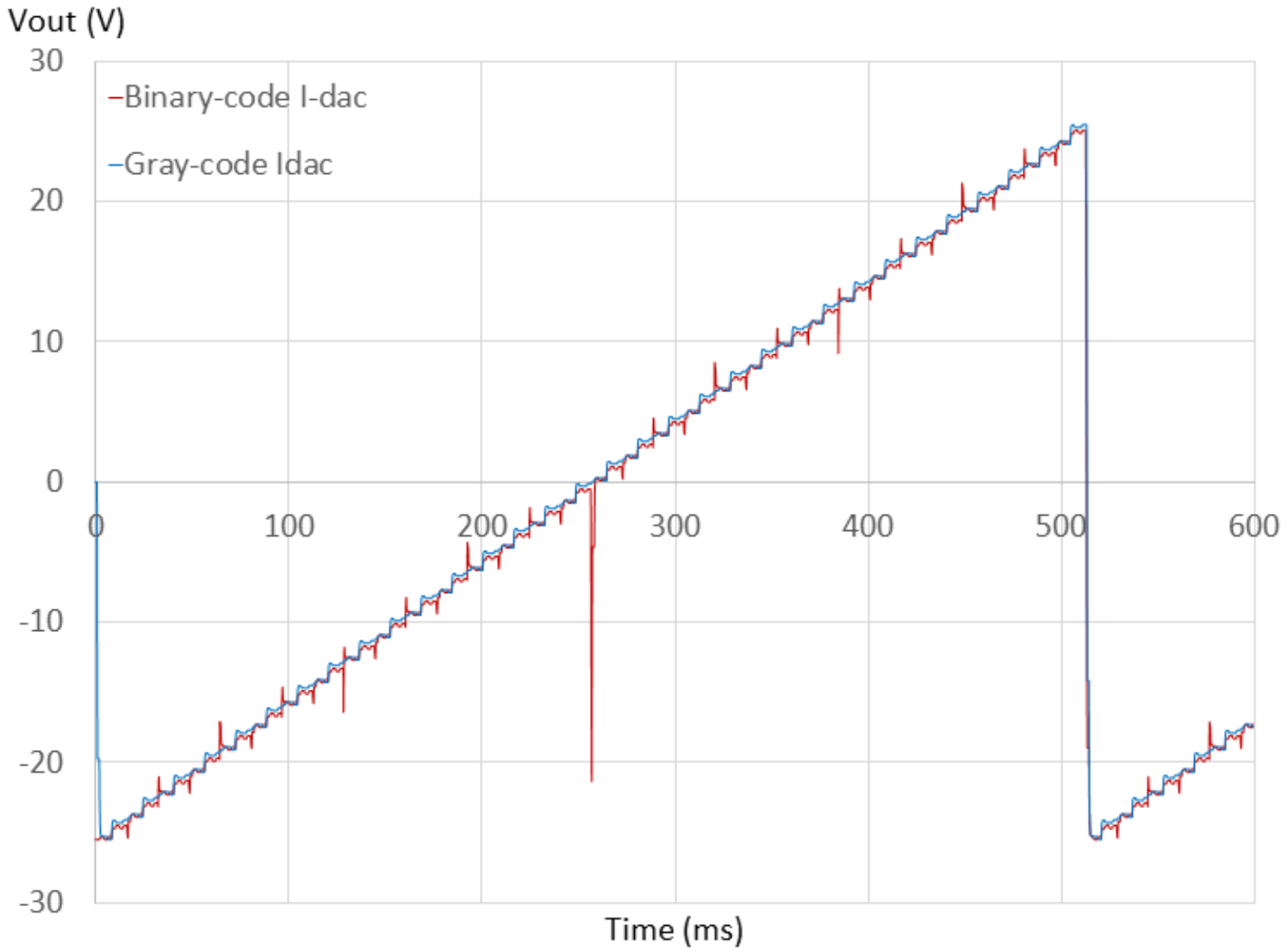
Simulation Result (Down Sweeping)





Binary-input Current-Steering DAC vs. Gray-code input current-steering DAC

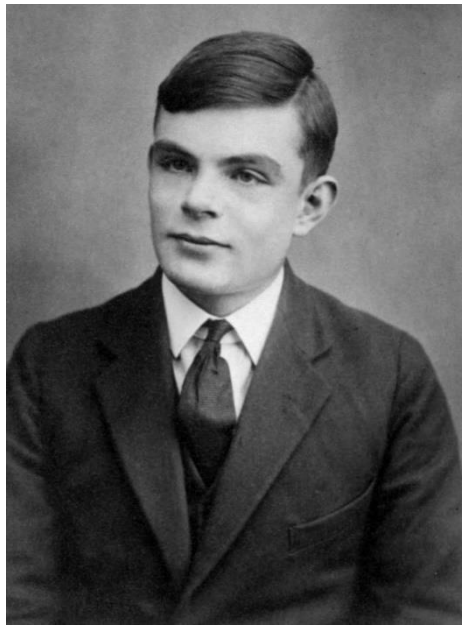
Simulation Result (Random Switching Delay)



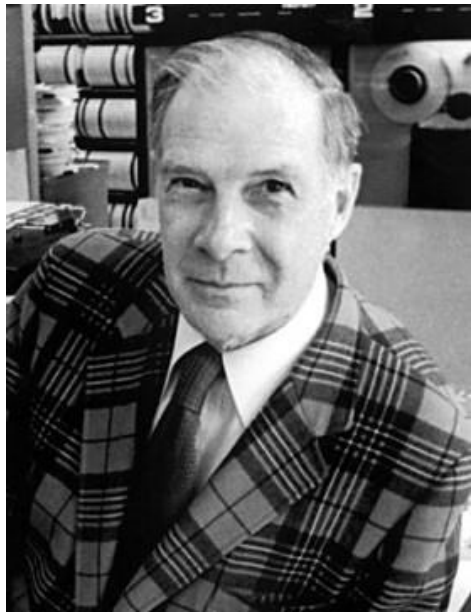
Binary-input Current-Steering DAC vs. Gray-code input current-steering DAC

Lesson from Gray-code Input DAC

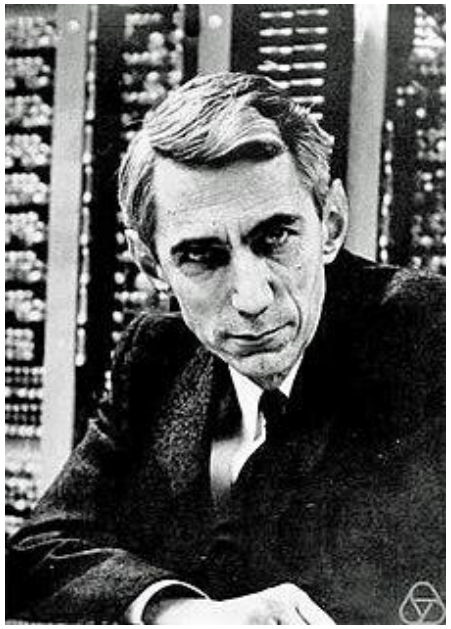
Coding theory leads to robust mixed-signal circuit design.



Alan Mathison Turing
1912 - 1954



Richard Wesley Hamming
1915 - 1998



Claude Elwood Shannon
1916- 2001

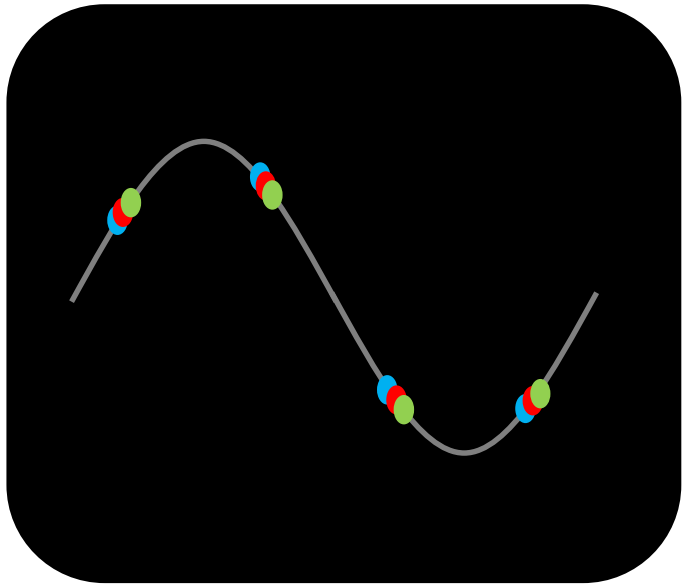
Contents

[11] S. Yamamoto, Y. Sasaki, Y. Zhao, J. Wei, A. Kuwana, K. Sato, T. Ishida, T. Okamoto, T. Ichikawa, T. Nakatani, T. M. Tran, S. Katayama, K. Hatayama, H. Kobayashi, "Metallic Ratio Equivalent-Time Sampling: A Highly Efficient Waveform Acquisition Method", 27th IEEE International Symposium on On-Line Testing and Robust System Design (June 2021).

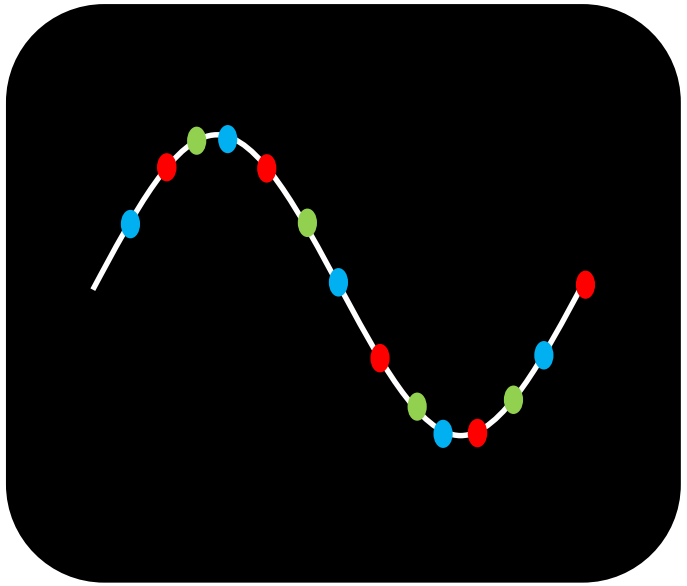
[12] Y. Sasaki, Y. Zhao, A. Kuwana, H. Kobayashi, "Highly Efficient Waveform Acquisition Condition in Equivalent-Time Sampling System", 27th IEEE Asian Test Symposium, Hefei, Anhui, China (Oct. 2018).

Research Objective

For IC testing,
high efficiency waveform acquisition
with equivalent-time sampling.



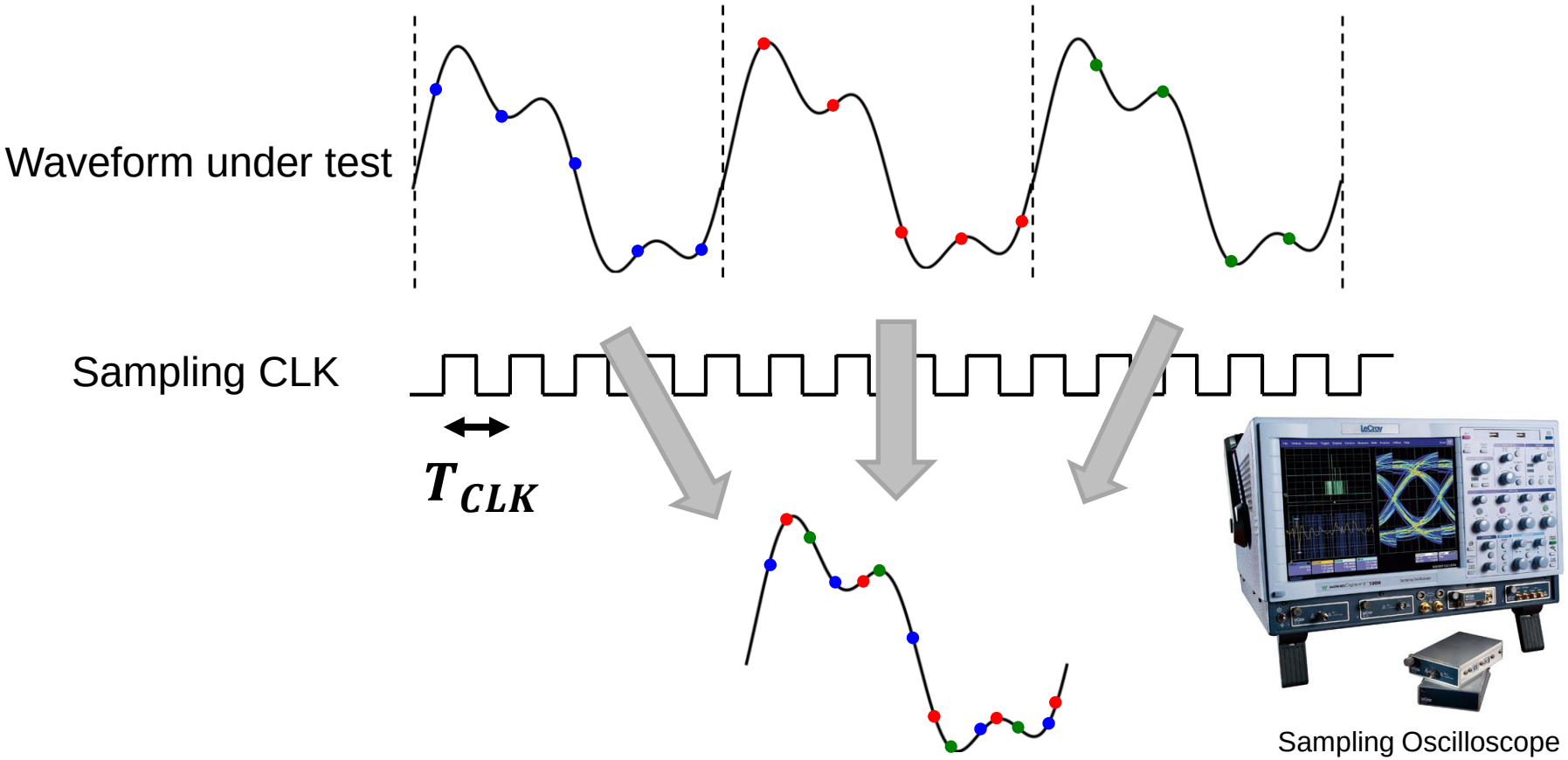
Sampling points: localized



Sampling points: distributed

Equivalent-Time Sampling

- Technique for acquisition of wideband repetitive waveform
- Used in sampling oscilloscope, automatic test equipment (ATE)

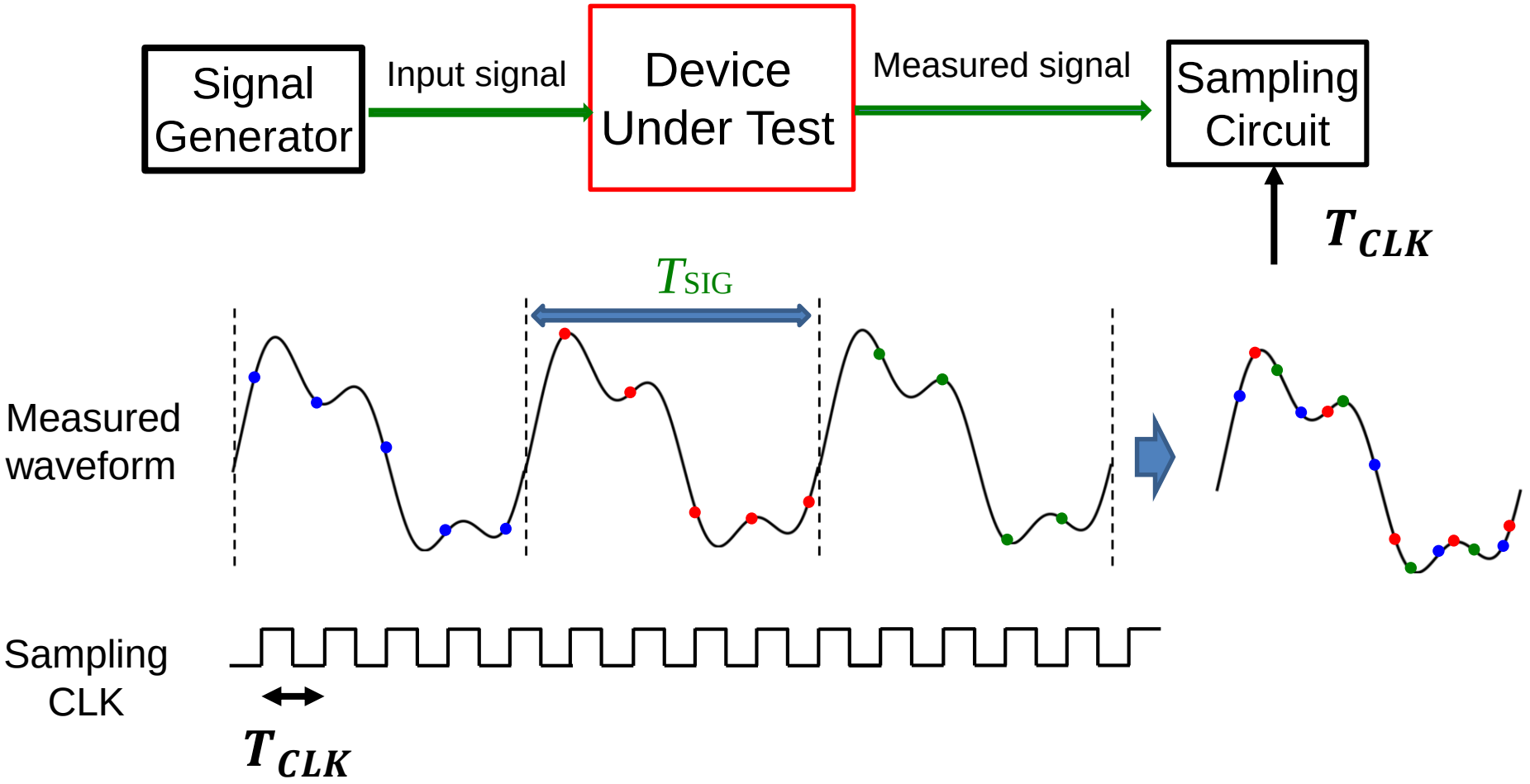


Sampling Oscilloscope

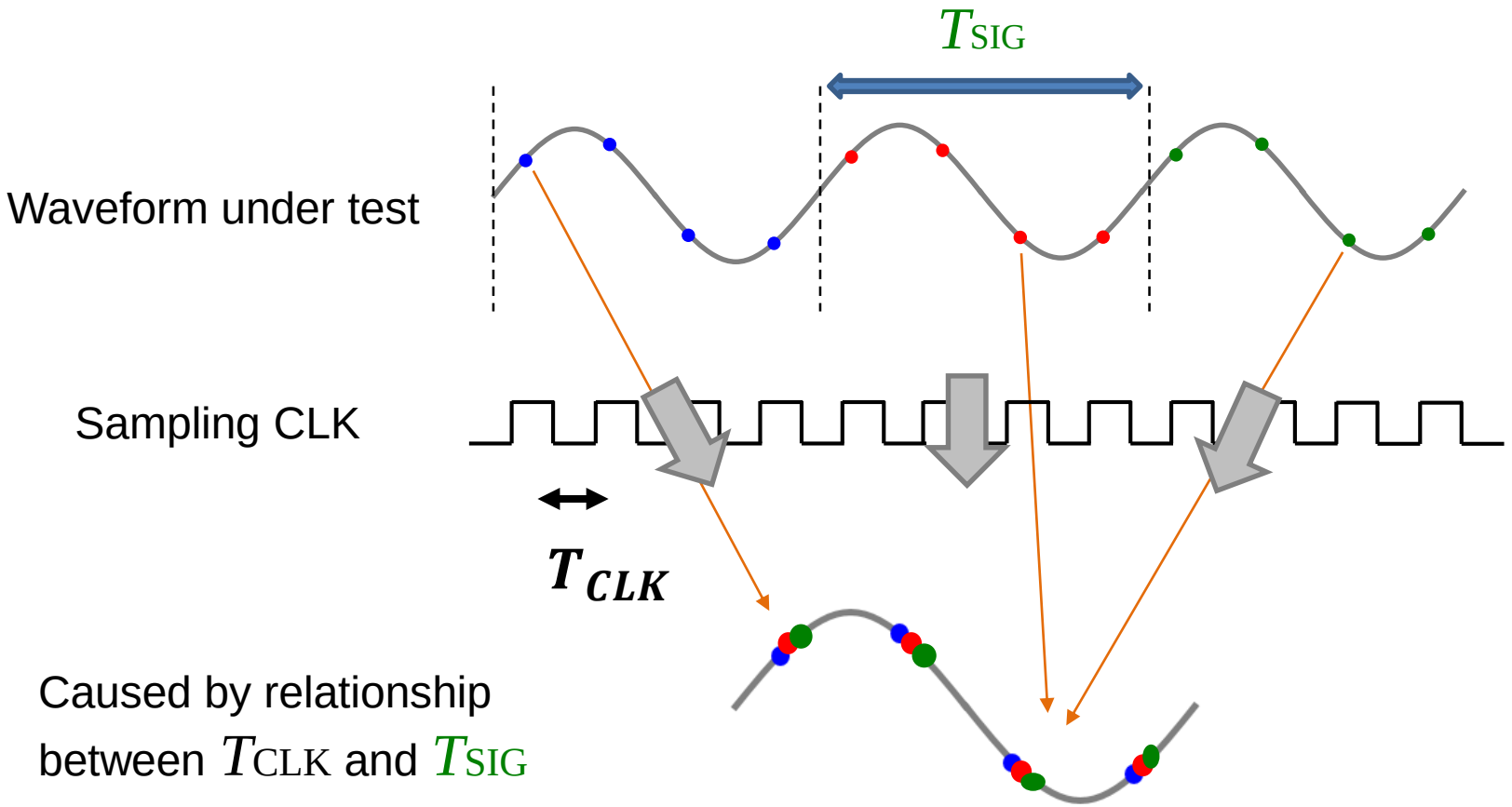
https://teledynelecroy.com/japan/products/scopes/we/default.asp

IC Testing and Equivalent-Time Sampling

- Input signal → Controlled during IC testing
  Input signal period T_{SIG} → Output signal period T_{SIG}



Waveform Missing Phenomena



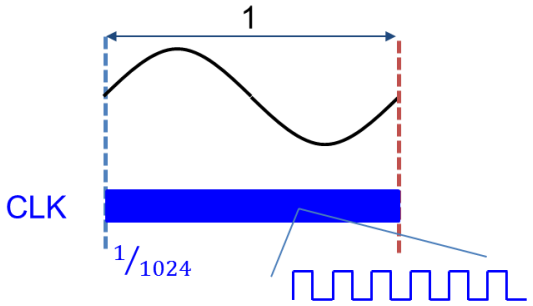
Caused by relationship between T_{CLK} and T_{SIG}

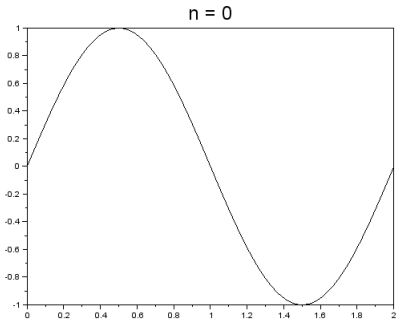
A lot of data → reconstruct one period

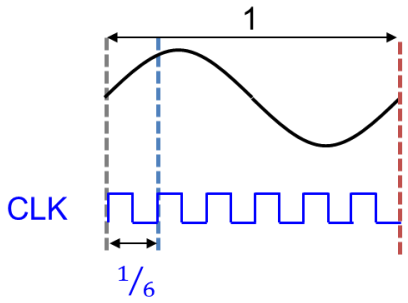
Test time： LONG

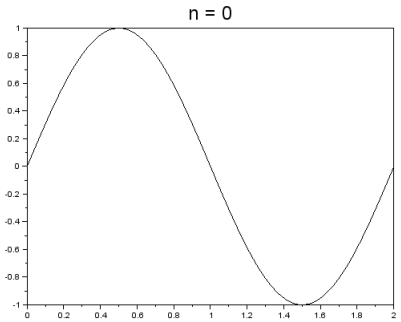
Waveform Missing Condition

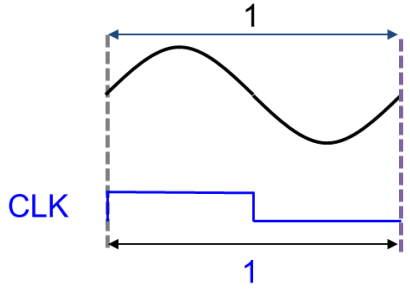
$f_{CLK} \gg f_{sin}$ $\quad f_{CLK} \approx \frac{1}{\alpha} f_{sin} \left(\alpha = 1, \frac{1}{2}, \frac{1}{3}, \frac{2}{3}, \cdots, \frac{1}{6}, \cdots\right)$ $\quad f_{CLK} \approx f_{sin}$

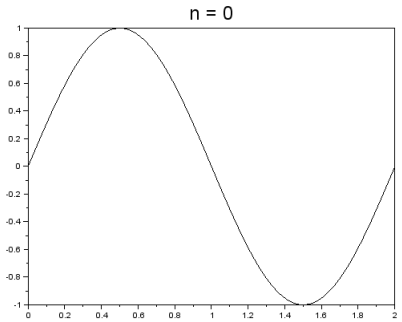










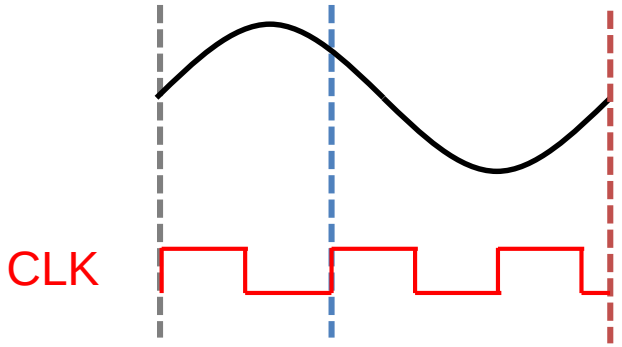


Sampling points: Localized

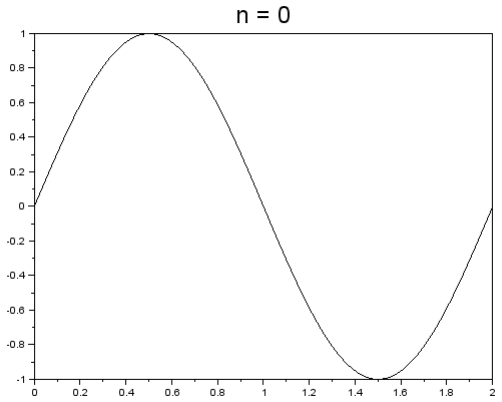
➡ Distance ratio between adjacent sampling points: Large

Efficient Waveform Acquisition Condition

Proper CLK



Sampling points: distributed



High efficiency waveform acquisition

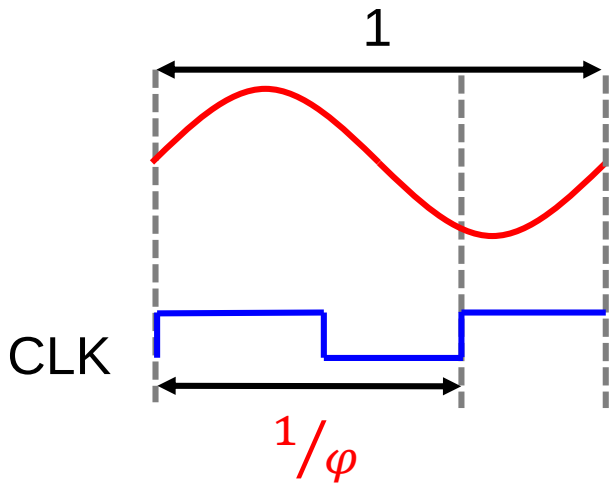
Sampling points: Distributed

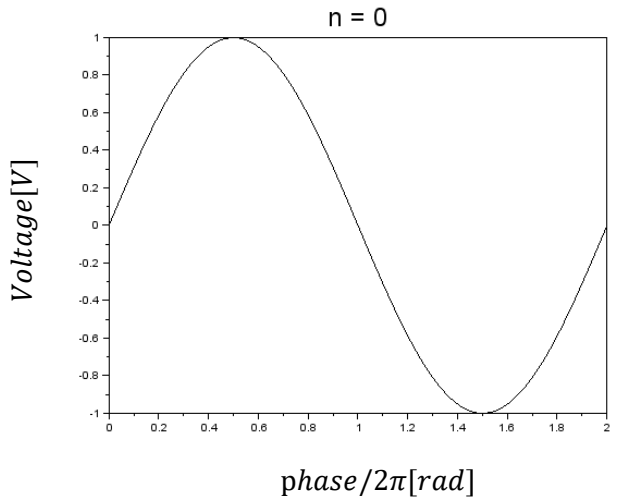
Distance ratio between adjacent sampling points： Small

Golden Ratio Sampling

$$f_{CLK} = \varphi \times f_{sig}$$

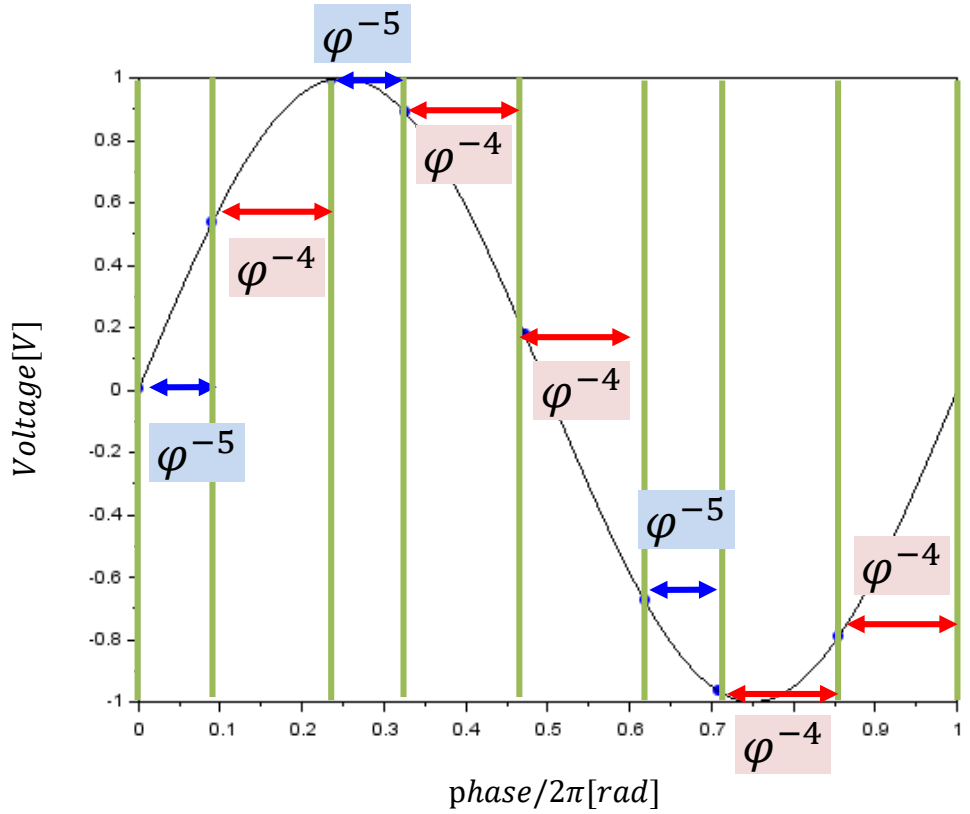
φ : golden ratio (= 1.6180339887…)





Sampling points ➡ Always distributed evenly in phase

Distance of Adjacent Sampling Points



Golden ratio sampling case

$\boldsymbol{\varphi}$: golden ratio (= 1.6180339887…)

Maximum distance／Minimum distance ＝ φ or φ^2

➡ Sampling point distances： Not too close & Not too far

Metallic Ratios

Metallic ratios

$$1 : \frac{n + \sqrt{n^2 + 4}}{2} \qquad (n = 1, 2, 3 \cdots)$$

M：Metallic number

$n=1$： Golden ratio（$M = 1.6180\ldots$）

$n=2$： Silver ratio （$M = 2.4142\ldots$）

$n=3$： Bronze ratio（$M = 3.3027\ldots$）

⋮

$n=m$： $1 : M$

Difference from reciprocal

$$M - \frac{1}{M} = \text{Natural Number}$$

Continued fraction

$$M = n + \cfrac{1}{n + \cfrac{1}{n + M}}$$

Limit of adjacent term ratio

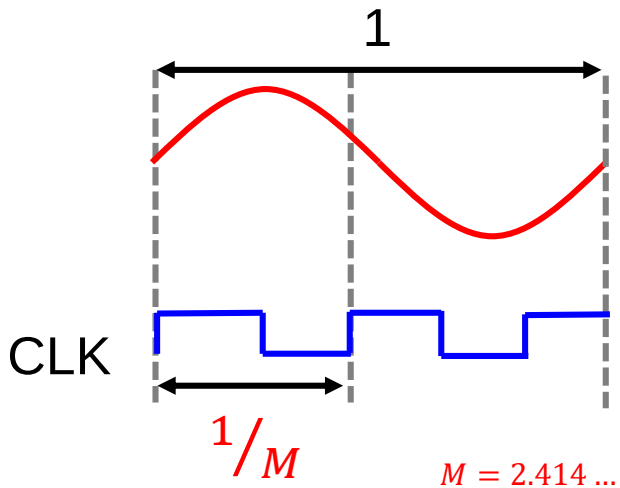
$$F_0 = 0, F_1 = 1, F_{n+2} = nF_{n+1} + F_n$$

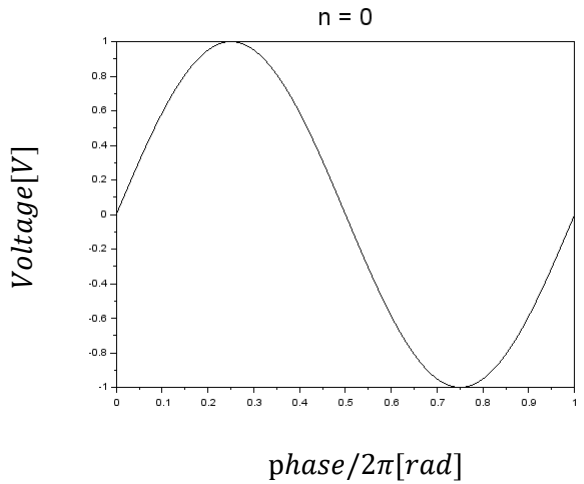
Metallic Ratio Sampling

Fixed f_{CLK} → Test ADC with various f_{sig}

$$f_{CLK} = M \times f_{sig}$$

M : Metallic ratio





In the case of silver ratio

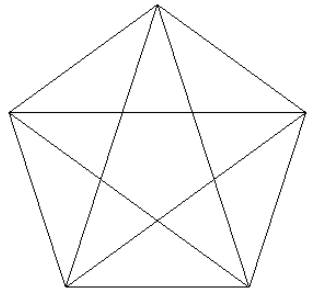
Sampling points ➡ Always distributed evenly in phase

Lesson from Metallic Ratio Sampling

- Discovery of several rules
  of waveform acquisition efficiency
  for metallic ratio sampling

Number is within of all things.

Pythagoras



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[13] Y. Zhao, A. Kuwana, S. Yamamoto, Y. Sasaki, H. Kobayashi, T. M. Tran, T. Nakatani, K. Hatayama, K. Sato, T. Ishida, T. Okamoto, T. Ichikawa, J. Wei, S. Katayama, "Input Signal and Sampling Frequencies Requirements for Efficient ADC Testing with Histogram Method“, 36th International Technical Conference on Circuits/Systems, Computers and Communications, Korea (June 2021).

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Research Objective

SAR ADC linearity test takes a long time

- low-speed sampling
- high-resolution

Test cost is proportional to test time

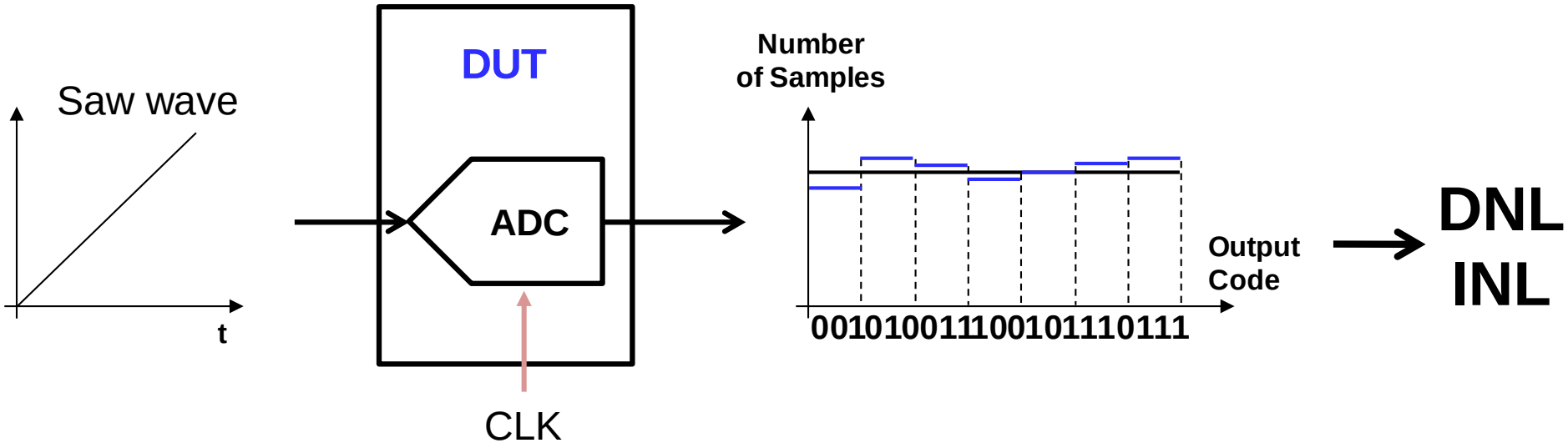
This Work

ADC linearity test with histogram method:

Investigation of "high efficiency relationship"
between input and sampling frequencies

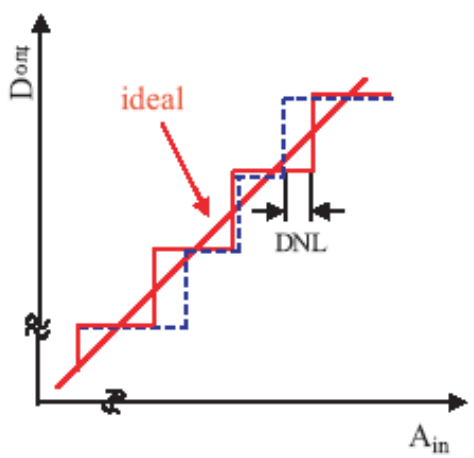
Linearity Testing with Histogram Method

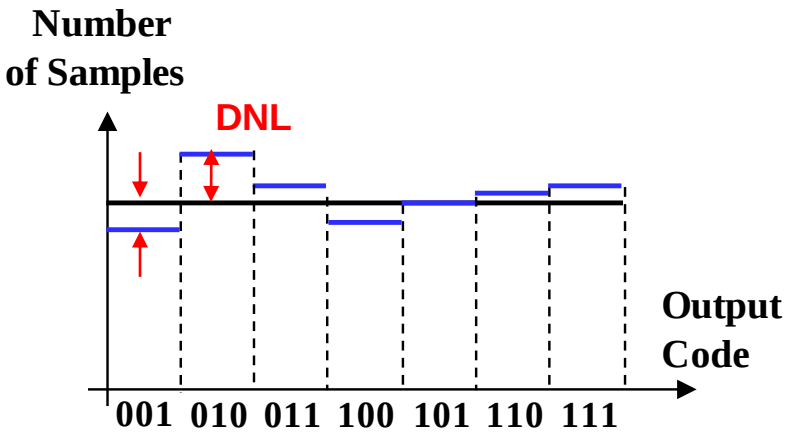
■ Histogram method (Saw wave input)

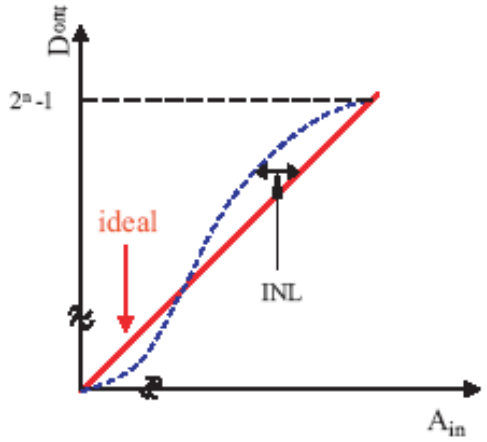


- ADC output histograms for all bins are equal if ADC is perfectly linear

DNL & INL







- Important ADC testing items

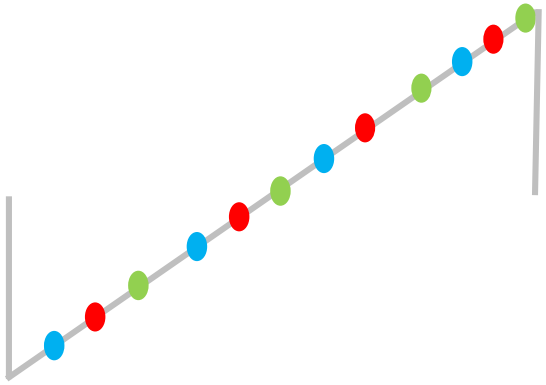
DNL : Difference between
actual step width and ideal value

INL : Deviation from ideal conversion line

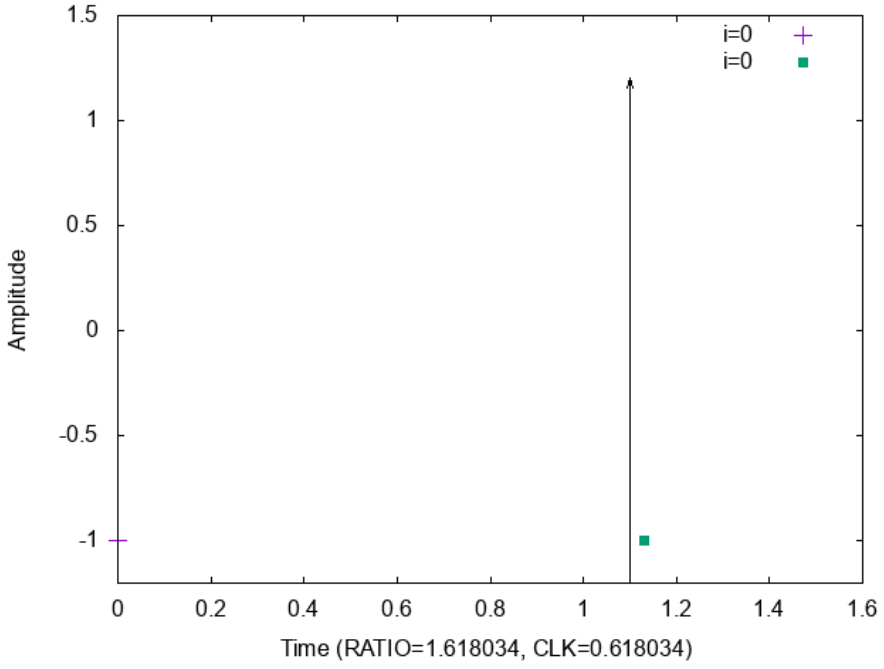
$$INL(k) = \sum_{i=1}^{k} DNL(i)$$

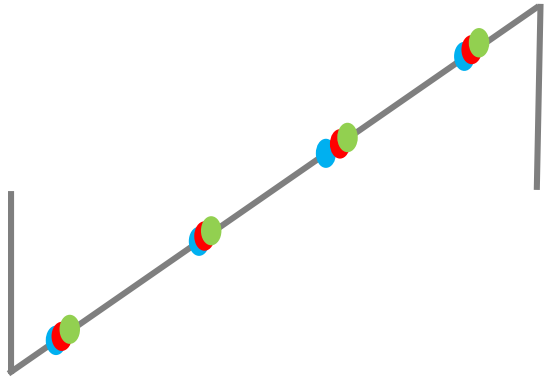
DNL: Differential Non-Linearity
INL: Integral Non-Linearity

Waveform Missing for Saw Signal

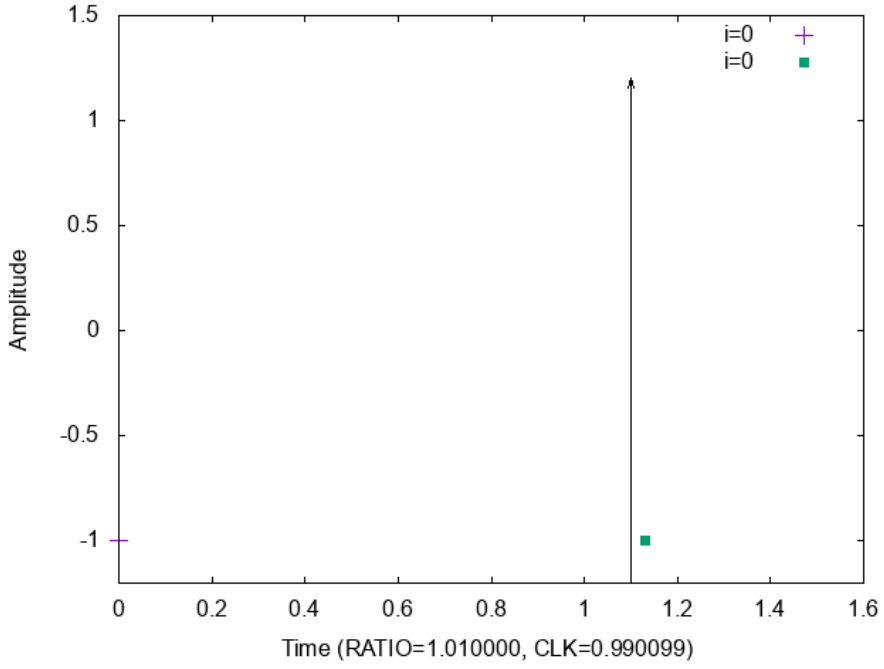


Normal situation





Waveform Missing



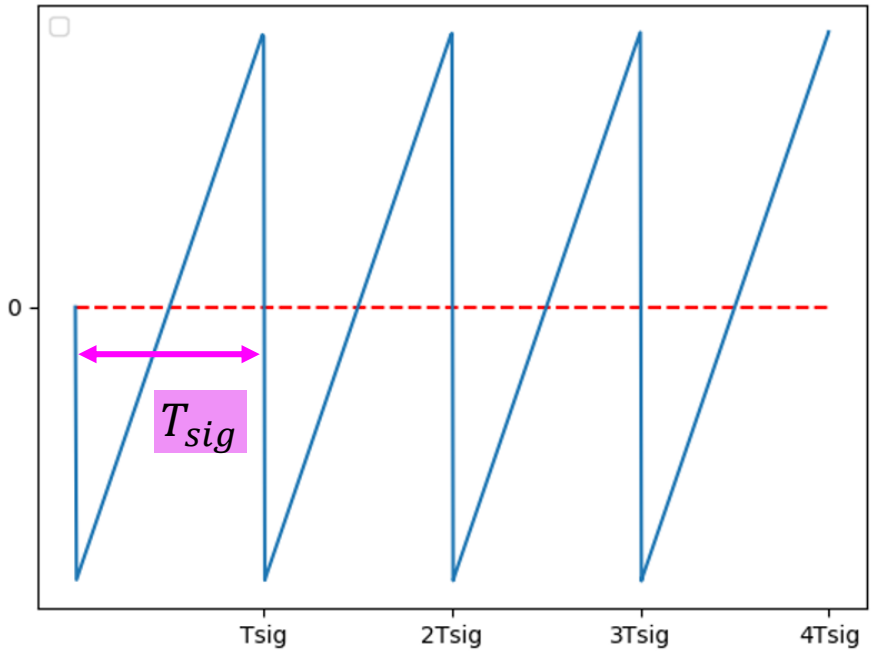
Metallic Ratio

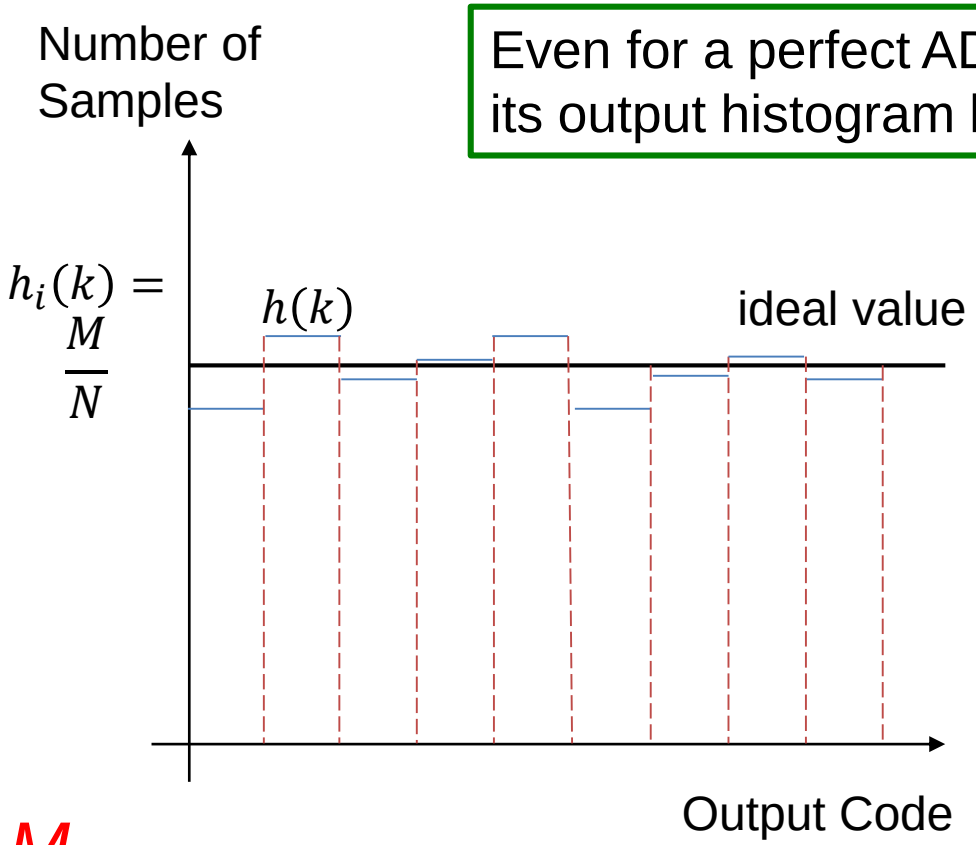
Golden Ratio: $\lim_{n\to\infty} \frac{F_n}{F_{n-1}} = 1.61803398874989.. = \varphi$

n		Decimal	
0	1		
1	$\frac{1+\sqrt{5}}{2}$	1.6180339887…	Golden Ratio
2	$1+\sqrt{2}$	2.4142135623…	Silver Ratio
3	$\frac{3+\sqrt{13}}{2}$	3.3027756377…	Bronze Ratio
4	$2+\sqrt{5}$	4.2360679774…	
…	…		
n	$\frac{n+\sqrt{n^2+4}}{2}$		

Generalization of Golden Ratio

ADC Output Histogram for Saw Signal Input





Even for a perfect ADC,
its output histogram has some errors.

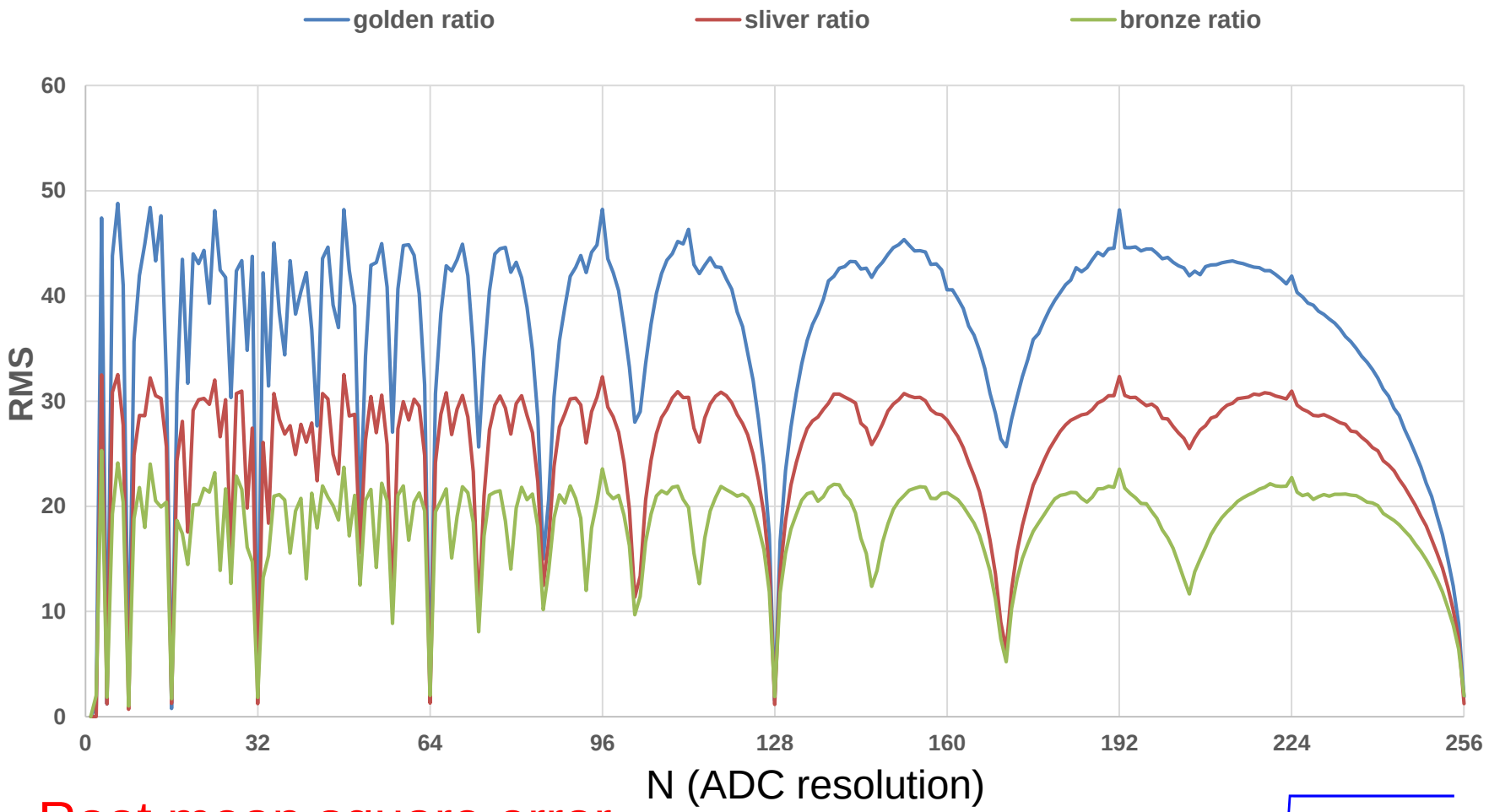
Total number of samples: *M*
ADC resolution :*N*.

ideal value $h_i(k) = \frac{M}{N}, k = 1,2,3,\ldots,N$ error $e(k) = \frac{N \cdot h(k)}{M} - 1$

RMS Error Calculation

$$f_{CLK} = f_{sig} \times RATIO$$

Total number of samples: M=65536



Root mean square error

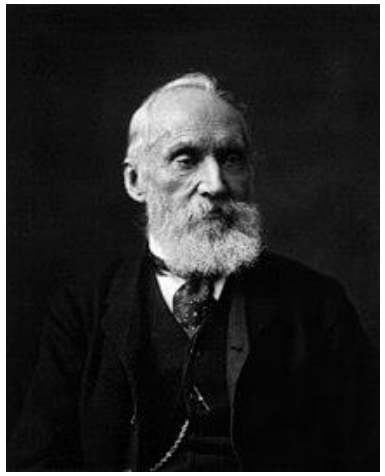
between actual and ideal histograms

$$RMS = \sqrt{\frac{\sum(e(k))^2}{N}}$$

Lesson from ADC Histogram Test

Input frequency vs Sampling frequency

Some metallic ratio sampling is very good.



Lord Kelvin
1824 - 1907

No science
without measurement

No production
without test

Testing is important as well as design

Contents

Conclusion

Analog / mixed-signal IC designers can obtain
new circuit design hints from classical mathematics.

Both circuit design and mathematics are fun !

陳 景潤　Chen Jingrun
Chinese Mathematician
(Integer theory)
1933-1996

厦門大学　Sept. 2013

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