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Analysis of Switching Characteristics of Wide SOA and High Reliability 100 V N-LDMOS Transistor with Dual RESURF and Grounded Field Plate Structure

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Outline

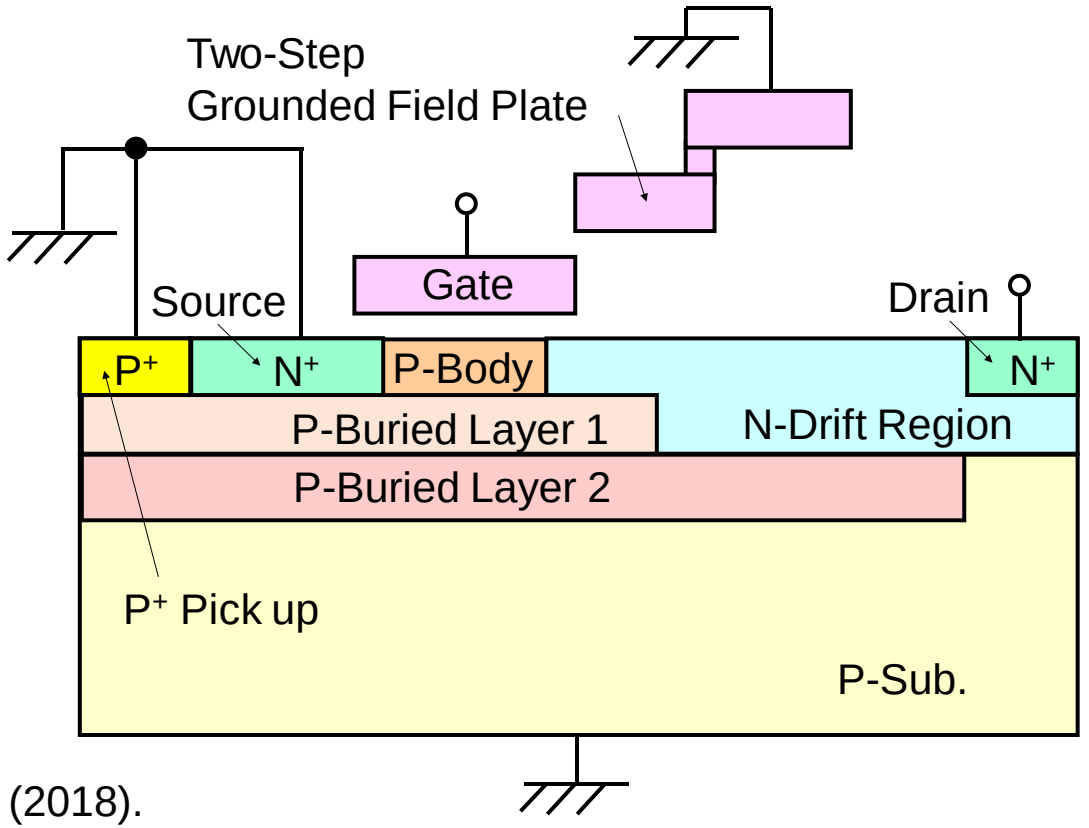
1. Objective and Background
2. Conventional and Proposed LDMOS Transistor Structures
3. Simulation Results
   - Turn-on characteristics (Conventional)
   - Turn-on characteristics (Proposed)
   - Turn-off characteristics (Conventional)
   - Turn-off characteristics (Proposed)
4. Discussion
   - Switching losses by changing R_G&R_L
   - Total energy loss
5. Summary

Simulation:
3D device simulator Advance/DESSERT
developed by AdvanceSoft Corporation

Background

- We proposed a 0.35 μm CMOS compatible dual REduced SURface Field (RESURF) 100 V LDMOS transistor with a two-step grounded field plate*.

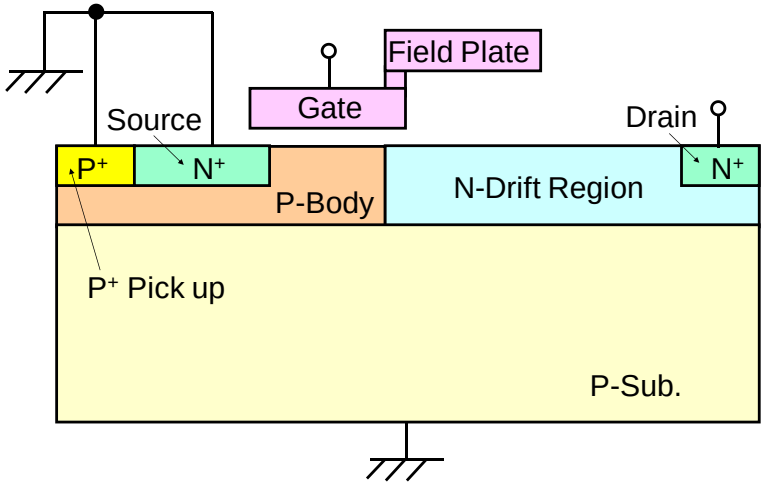
- For automotive applications
  to meet the requirements for...
  - ➢ wide SOA (Safe Operating Area)
  - ➢ high hot carrier endurance
  - ➢ low specific on-resistance
  - ➢ low switching loss



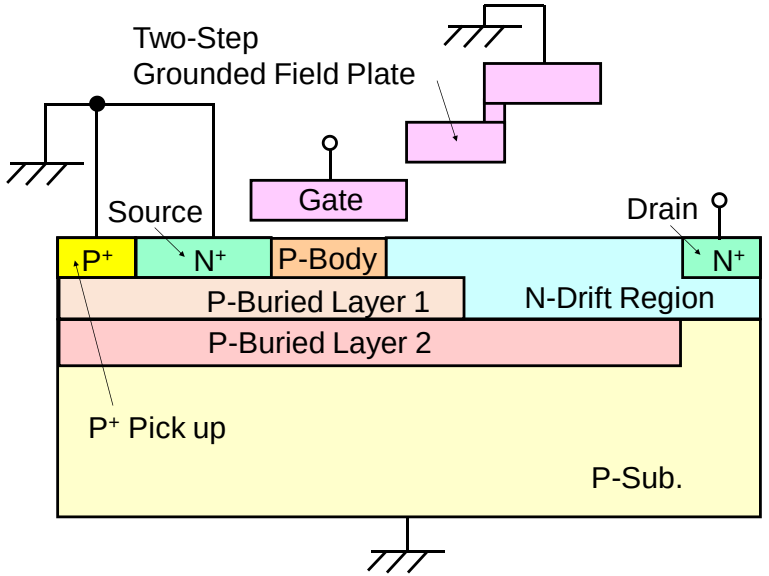
*J. Matsuda, A. Kuwana, J. Kojima, N. Tsukiji, and H. Kobayashi, ICSICT, (2018).

Device Structures and Features

Conventional



Proposed



<u>P-buried layers 1, 2.</u>
<u>Two-step grounded field plate.</u>

↓

Dual RESURF structure.

↓

Reduce the specific on-resistance with keeping the breakdown voltage high. ☺

<u>Grounded field plate.</u>

↓

Much smaller Miller capacitance.

↓

Smaller switching loss. ☺

*J. Matsuda, A. Kuwana, J. Kojima, N. Tsukiji, and H. Kobayashi, ICSICT, (2018).

Objective of This Study

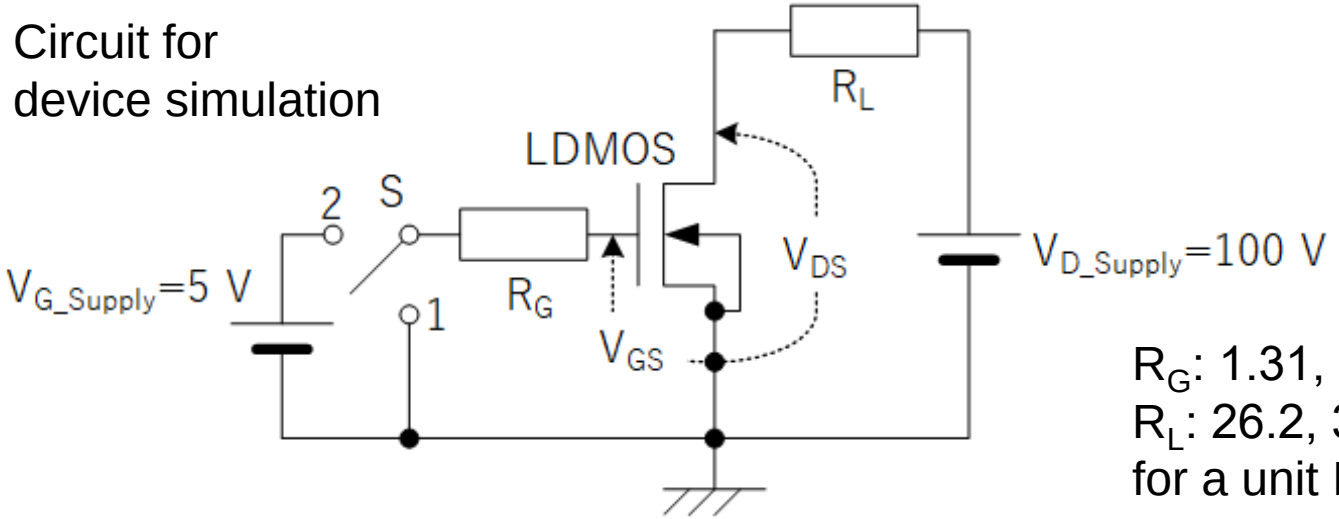
Previous Study

- The parameters were optimized and
  the acceptable range for mass production was clarified.
  - A. Kuwana, J. Matsuda and H. Kobayashi, ASICON, D7-5, Chongqing, China (2019).
  - J. Matsuda, A. Kuwana and H. Kobayashi, IEEJ Trans. EIS, Vol.140, No.11, pp.1220-1229, (2020) (in Japanese)

This Study

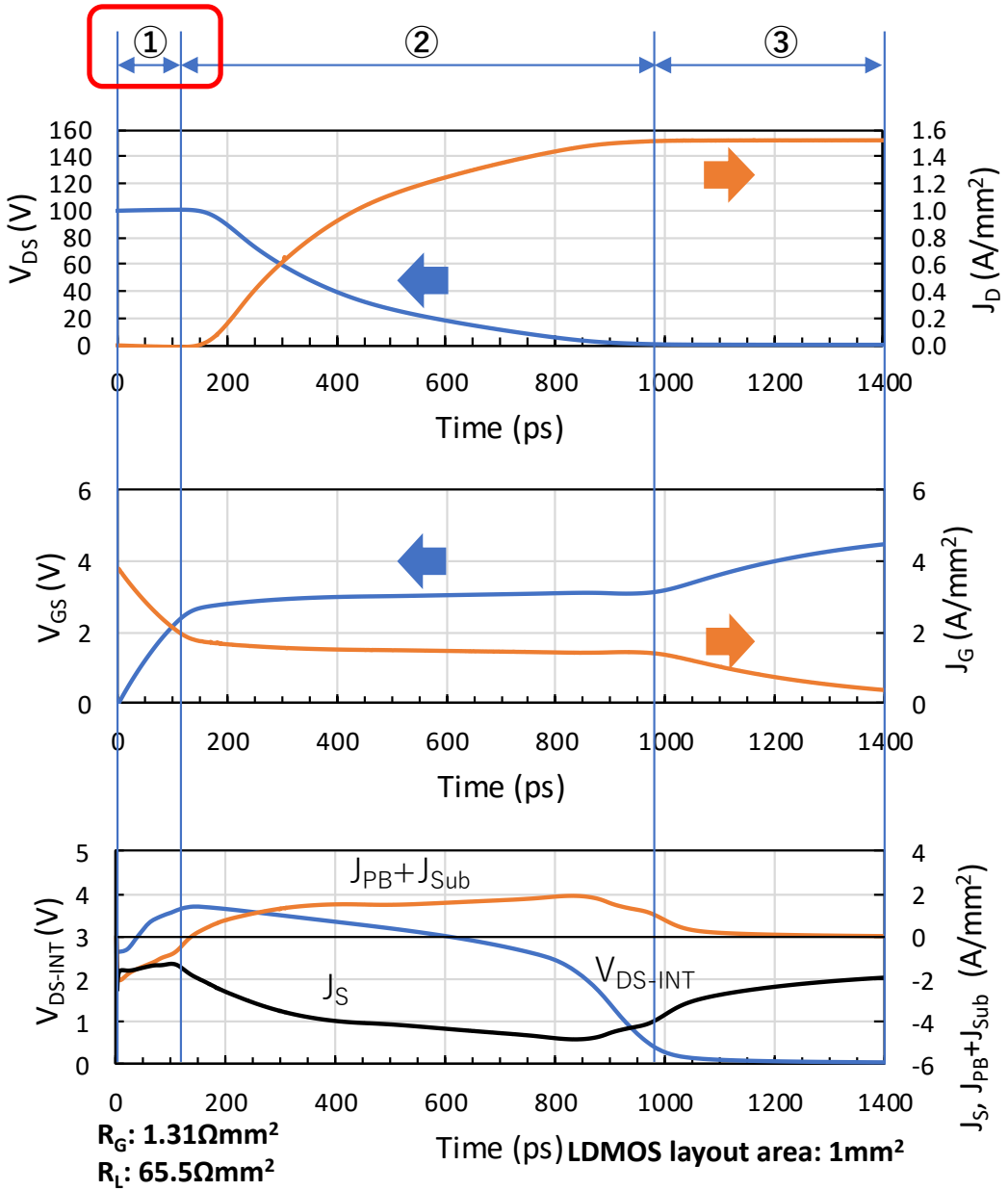
- Switching characteristics are analyzed in detail
  by changing the load resistance R_L and the gate resistance R_G

Circuit for
device simulation



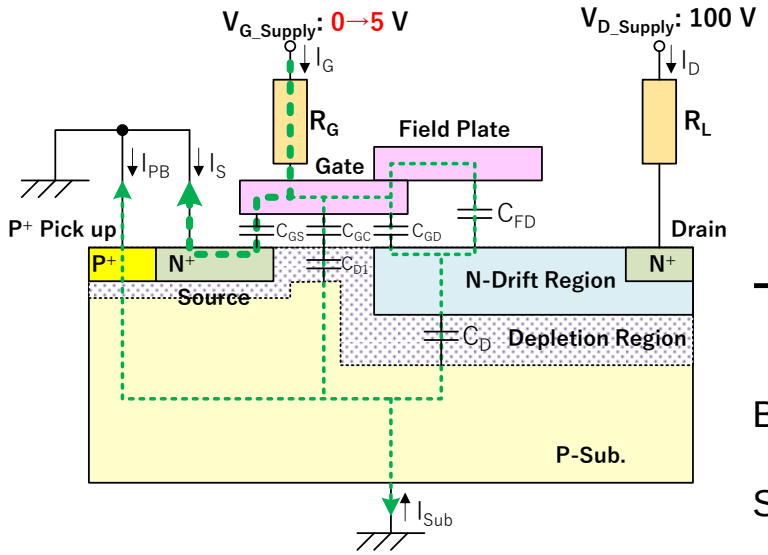
R_G: 1.31, 2.62, 6.55 Ωmm^2
R_L: 26.2, 39.3, 52.4, 65.5 Ωmm^2
for a unit LDMOS layout area of 1 mm^2

Turn-on characteristics (Conventional)



Region ① : OFF state

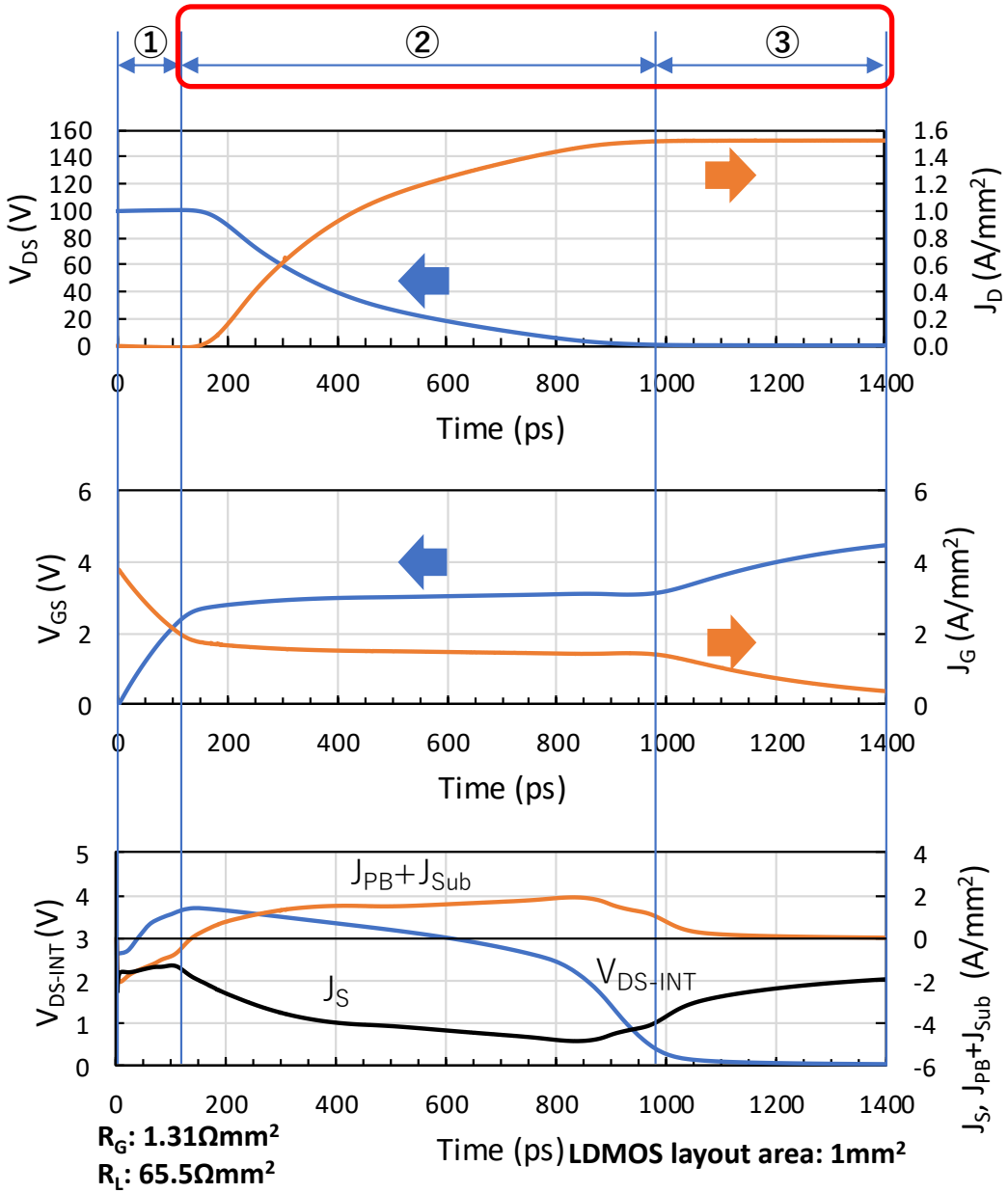
- $V_{GS} < V_T$ (the threshold voltage)
- V_{GS} increases, the gate current J_G flows
- Charge:
  - ✓ Input capacitance (C_{GS}+C_{GC})
  - ✓ Feedback capacitance (Miller capacitance: C_{GD}+C_{FD})
  - ✓ Output capacitance (C_D)



The current path

Broken Line:
Displacement Current
Solid Line:
Conducted Current

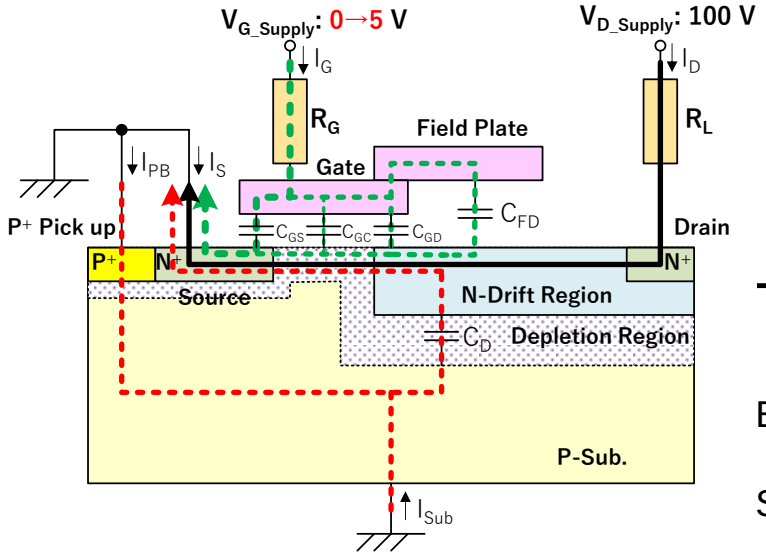
Turn-on characteristics (Conventional)



Region ② : Gate plateau state

- Charge $C_{GD}+C_{FD}$
- Drain voltage V_{DS} decreases
- Drain current J_D increases
- Discharge C_D

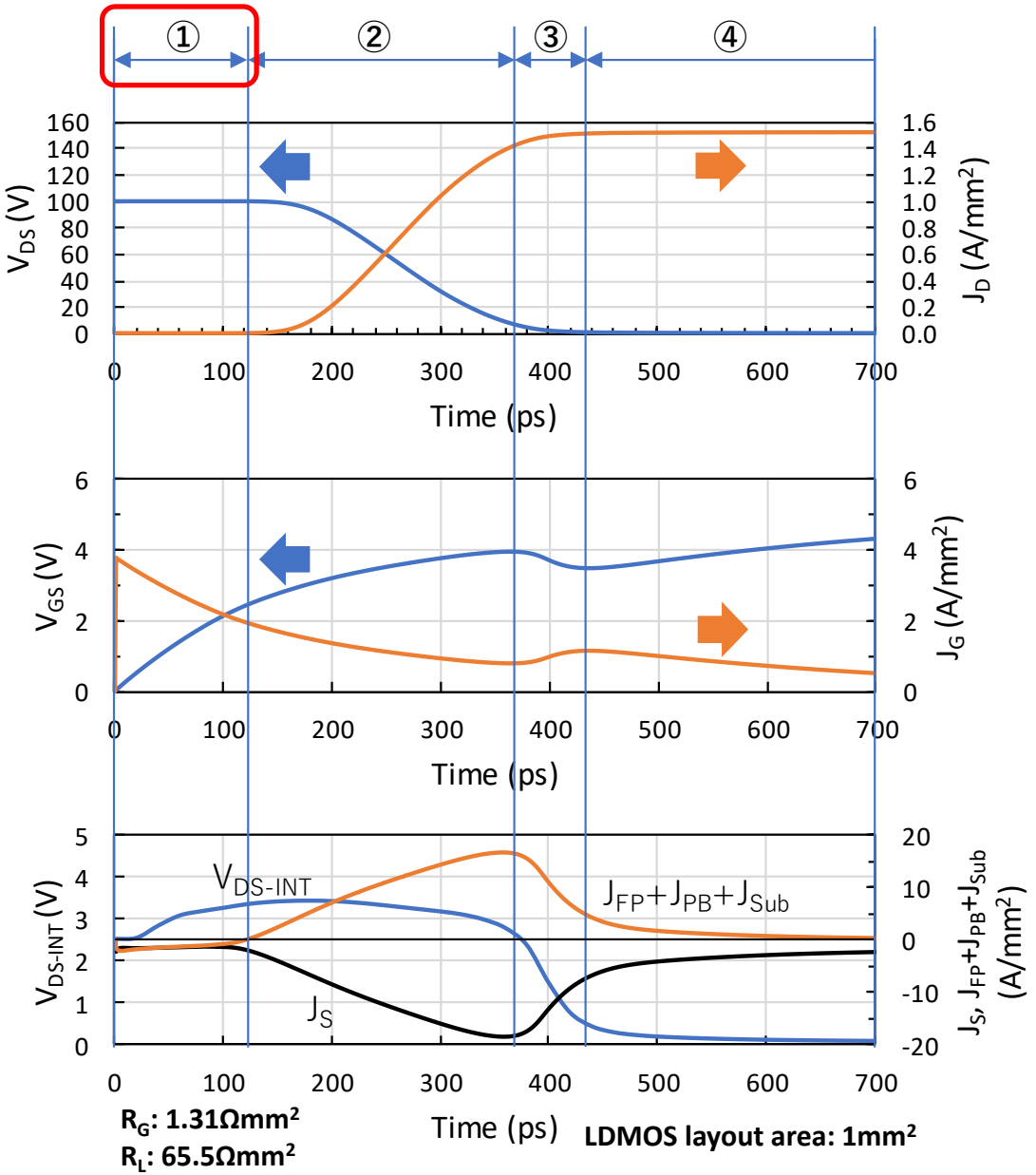
Region ③ : ON state.



The current path

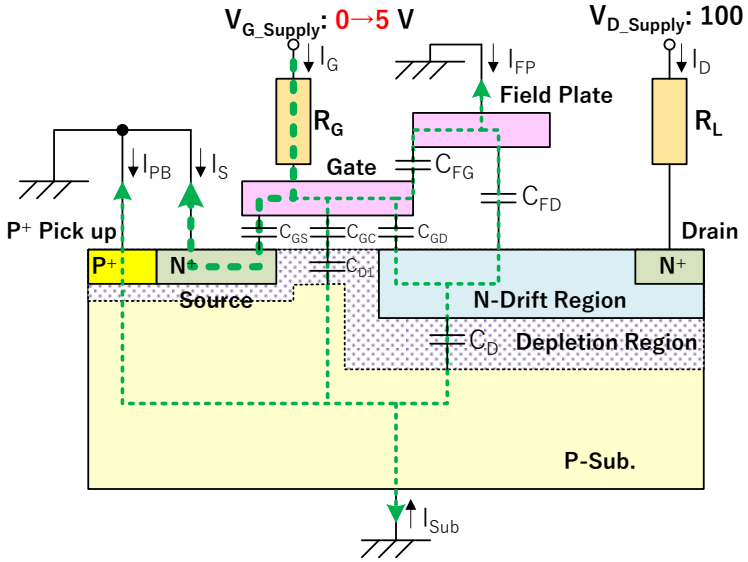
Broken Line:
Displacement Current
Solid Line:
Conducted Current

Turn-on characteristics (Proposed)



Region ① : OFF state

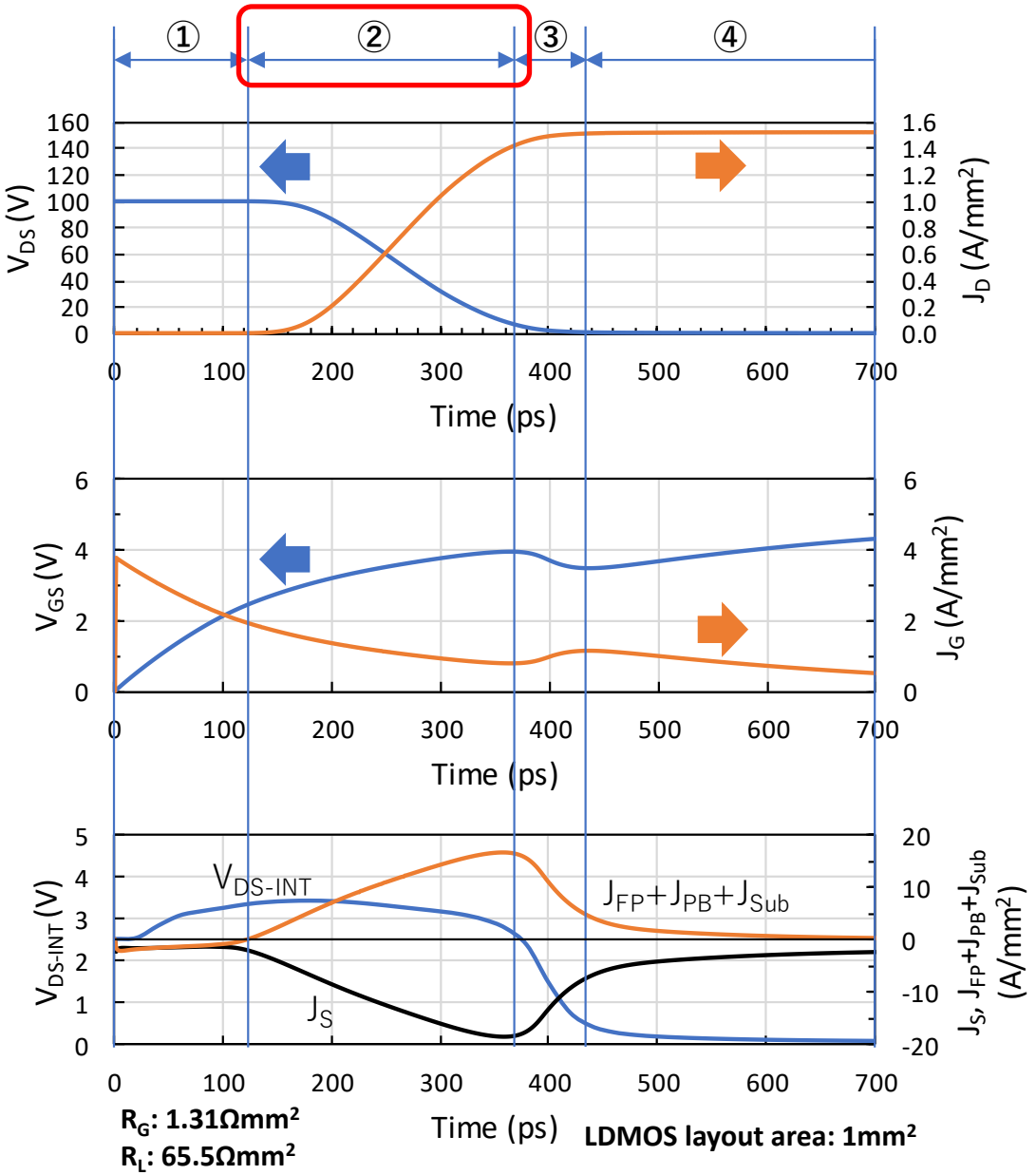
- $V_{GS} < V_T$ (the threshold voltage)
- V_{GS} increases, the gate current J_G flows
- Charge:
  - ✓ Input capacitance ($C_{GS}+C_{GC}+C_{FG}$)
  - ✓ Feedback capacitance (Miller capacitance: C_{GD})
  - ✓ Output capacitance (C_D+C_{FD})



The current path

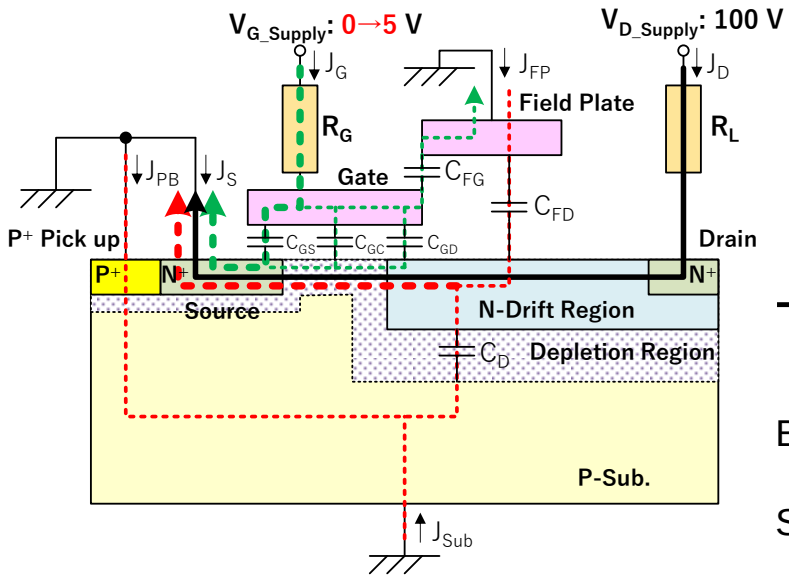
Broken Line:
Displacement Current
Solid Line:
Conducted Current

Turn-on characteristics (Proposed)



Region ② : J_D increase, V_{DS} decrease

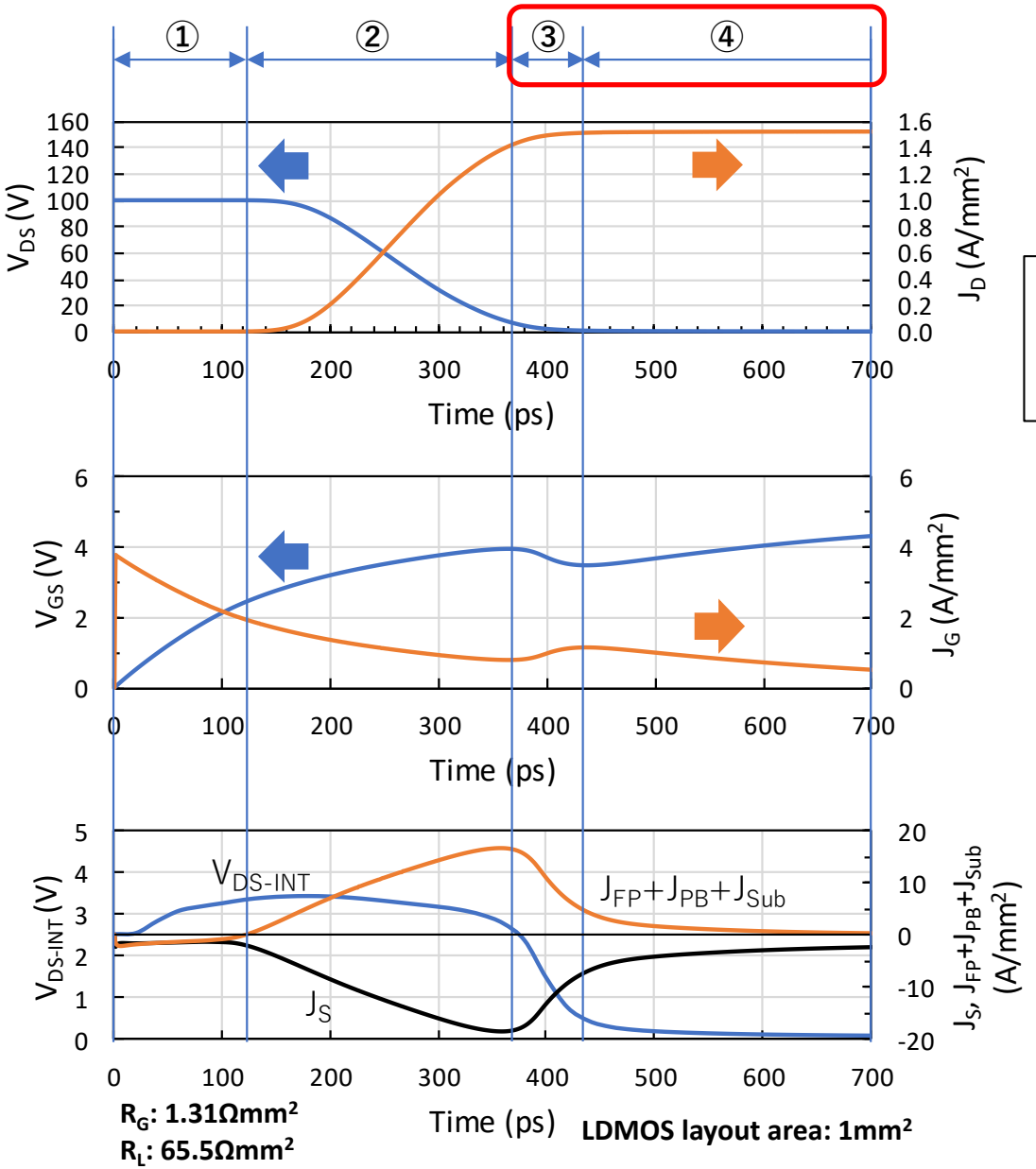
- V_{GS} increases.
- Displacement current ($J_{FP}+J_{PB}+J_{Sub}$) increases.
- Discharging C_D+C_{FD}
  → the drain voltage of the intrinsic MOSFET V_{DS-INT} almost constant.
- C_{GD} is not practically charged.



The current path

Broken Line:
Displacement Current
Solid Line:
Conducted Current

Turn-on characteristics (Proposed)

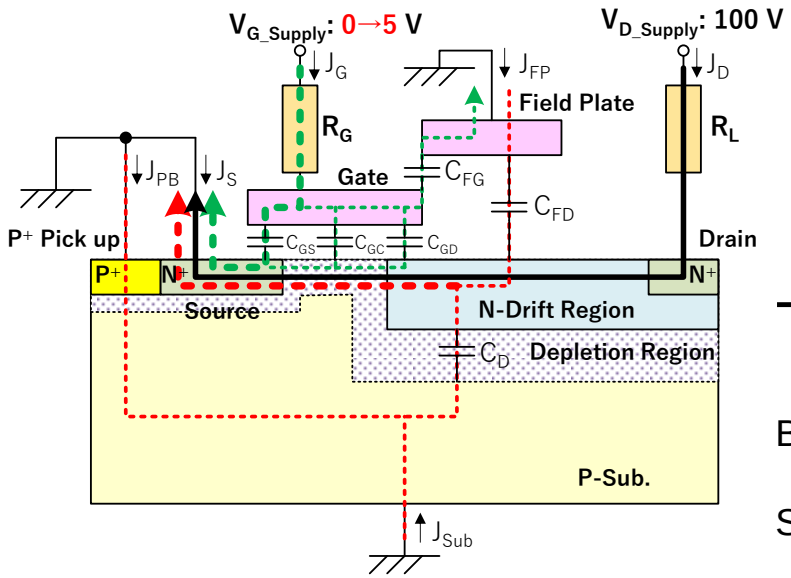


Region ③ : Gate plateau state

- Decrease V_{DS-INT} → C_{GD} charged.
- Miller effect.

Proposed field plate = Output capacitance.
Conventional field plate = Feedback capacitance.

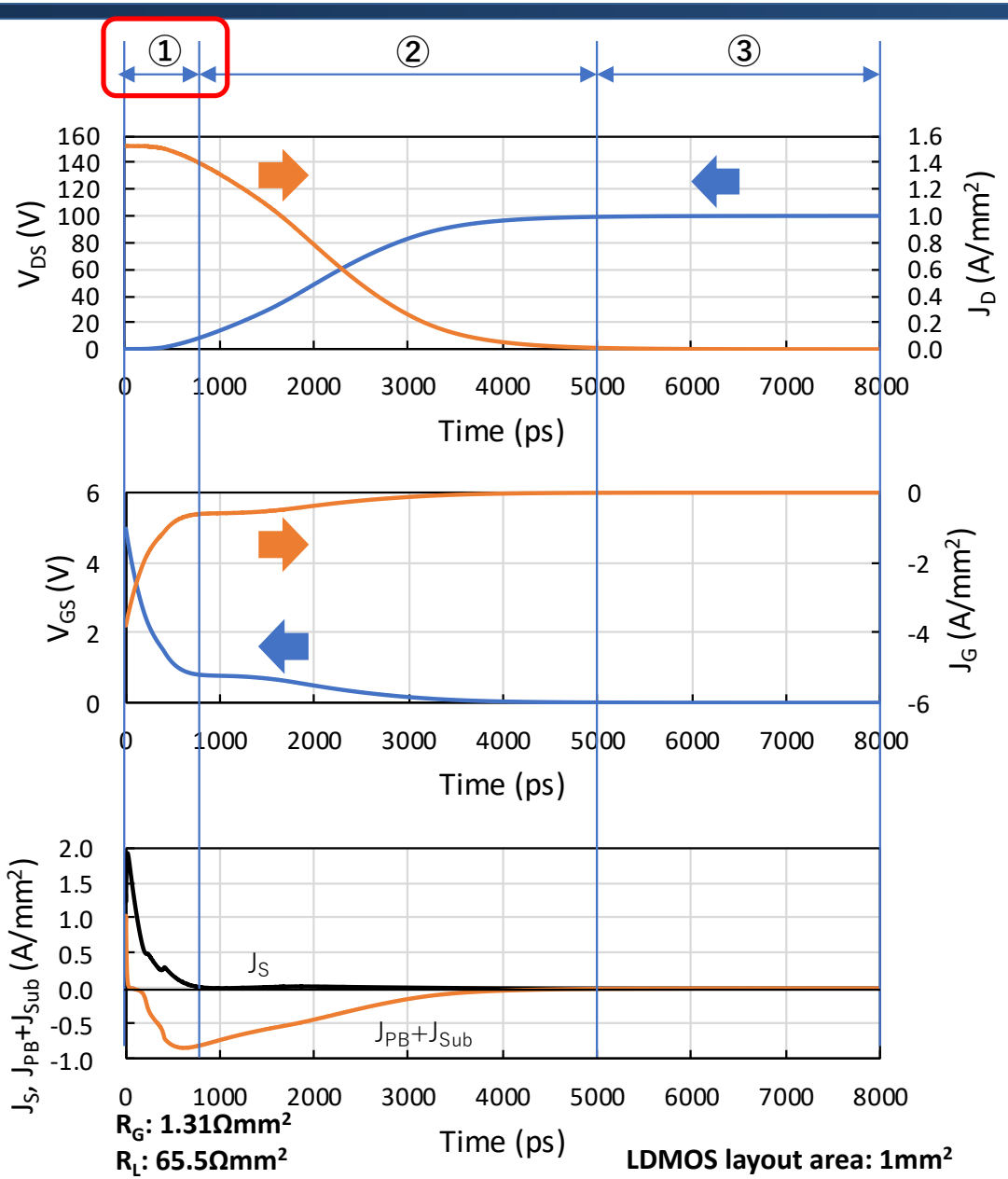
Region ④ is ON state.



The current path

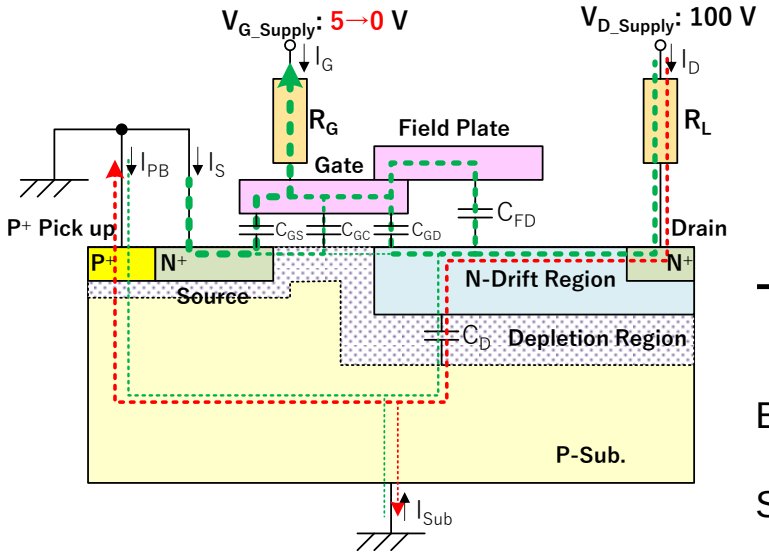
Broken Line:
Displacement Current
Solid Line:
Conducted Current

Turn-off characteristics (Conventional)



Region ① : ON state

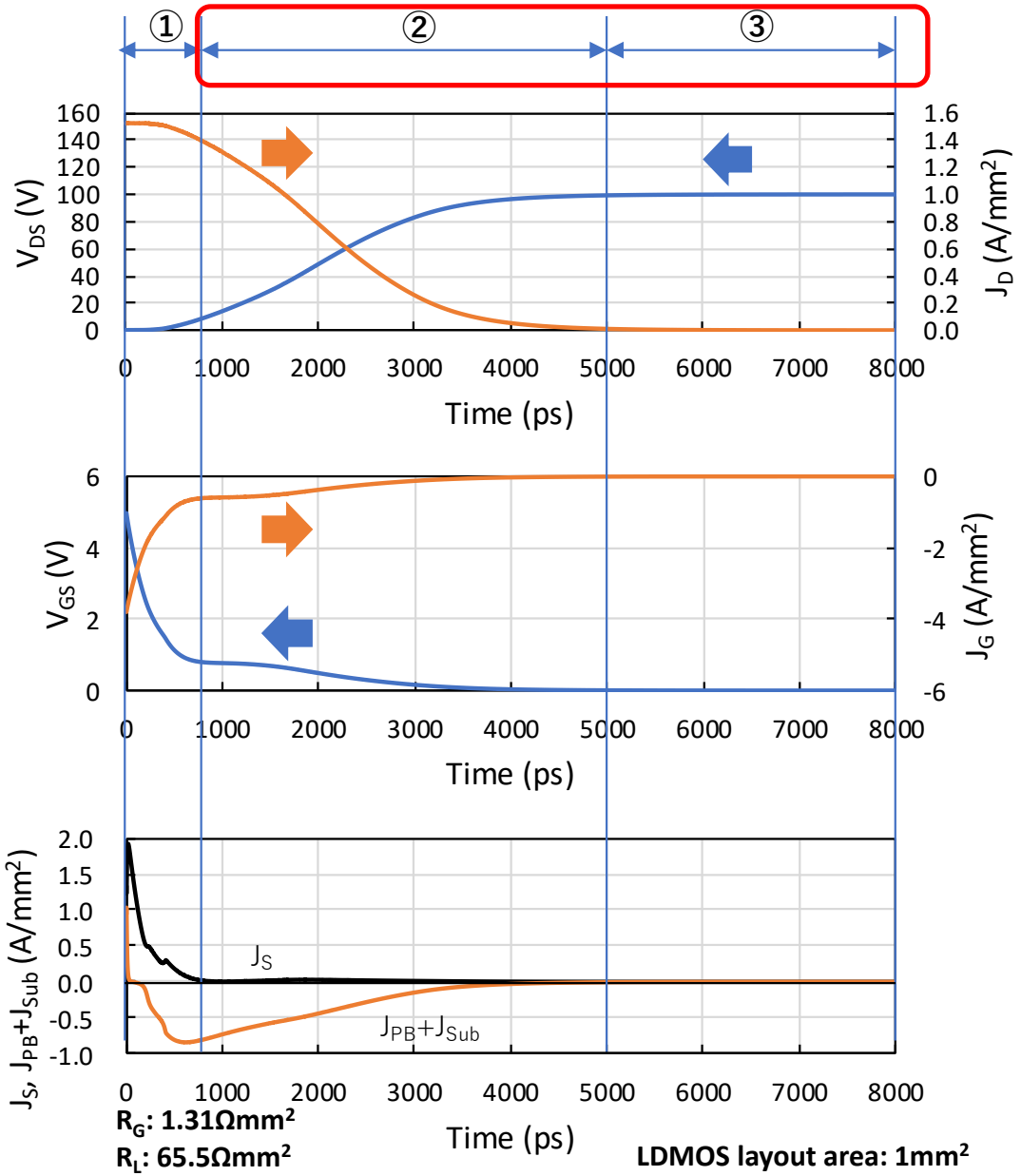
- Gate current J_G discharges
  - ✓ input capacitance (C_{GS}+C_{GC}).
  - ✓ feedback capacitance (C_{GD}+C_{FD}).
  - ✓ output capacitance (C_D).
- Drain current charges C_{GD}+C_{FD} and C_D
- Minus J_{PB}+J_{Sub} and minus J_G.



The current path

Broken Line:
Displacement Current
Solid Line:
Conducted Current

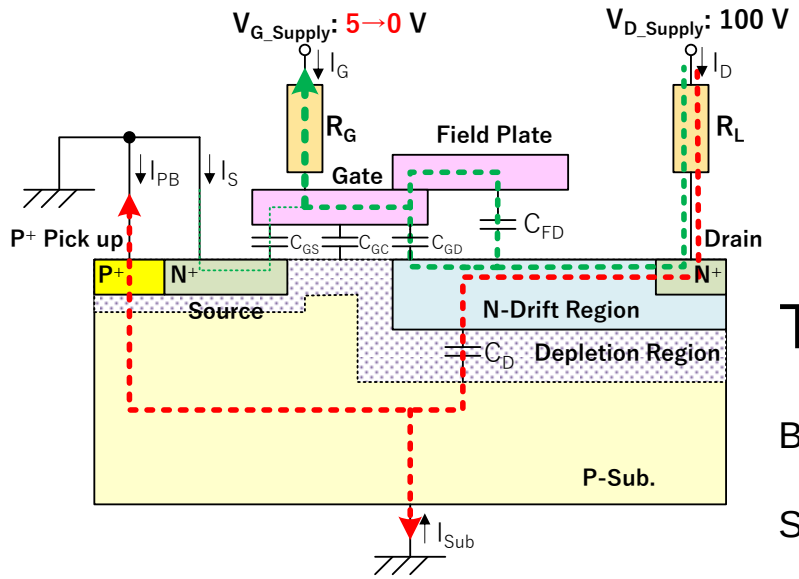
Turn-off characteristics (Conventional)



Region ②: turn-off process

- V_{DS} increases and J_D decreases
- displacement currents charging C_D and $C_{GD}+C_{FD}$
- Charging $C_{GD}+C_{FD}$ →Miller effect.

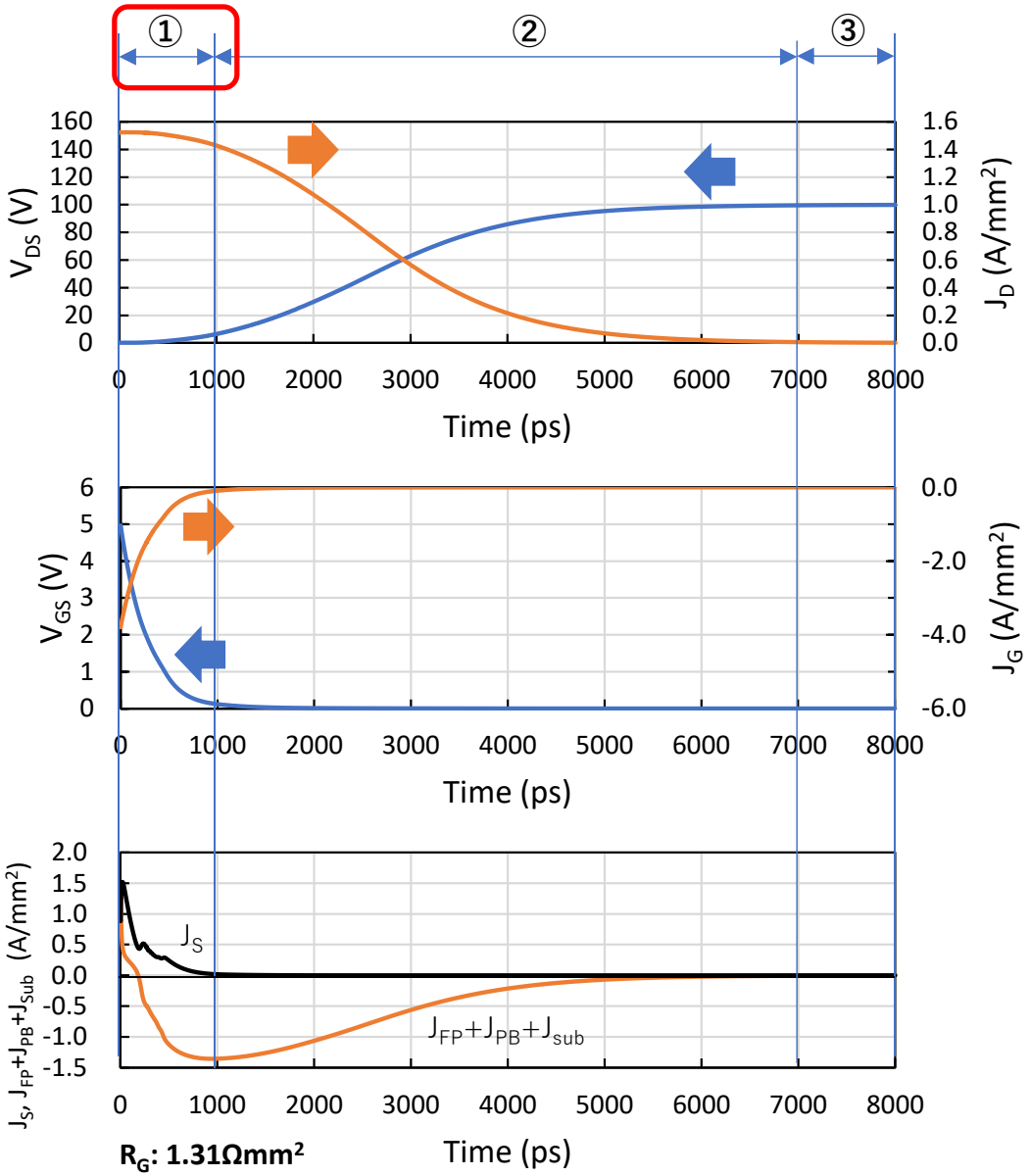
Region ③: OFF state.



The current path

Broken Line:
Displacement Current
Solid Line:
Conducted Current

Turn-off characteristics (Proposed)

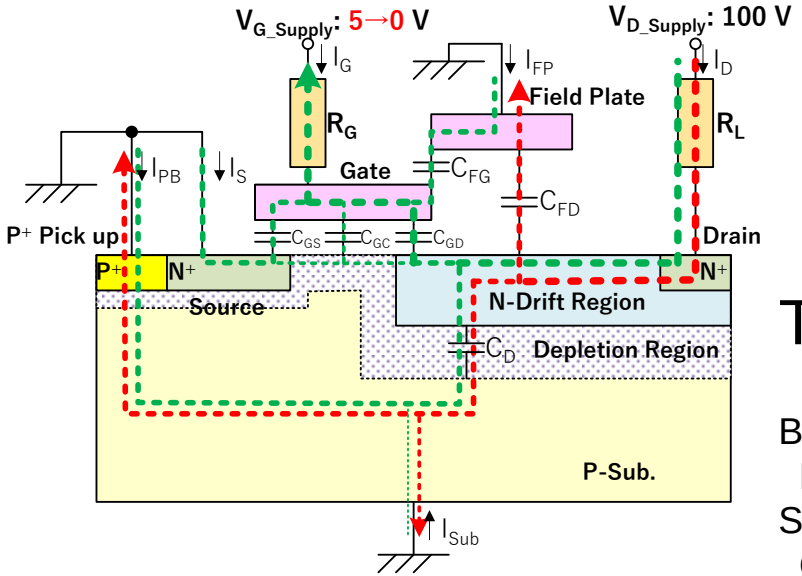


R_G: 1.31Ωmm²
R_L: 65.5Ωmm²

LDMOS layout area: 1mm²

Region ①: ON state

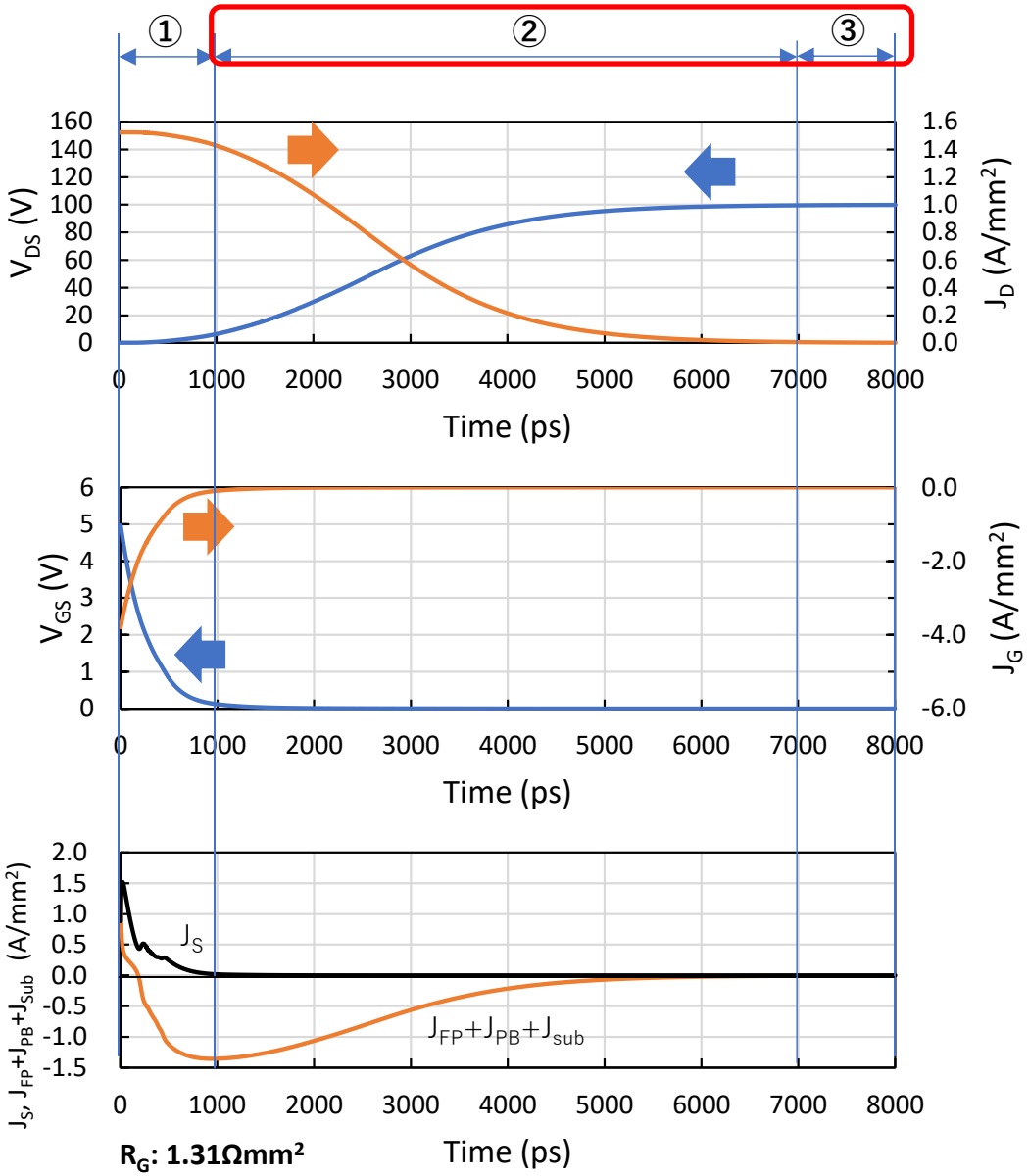
- Parasitic capacitance tied to the gate is smaller
  → Gate switching is faster
  Miller effect is not observed



The current path

Broken Line:
Displacement Current
Solid Line:
Conducted Current

Turn-off characteristics (Proposed)



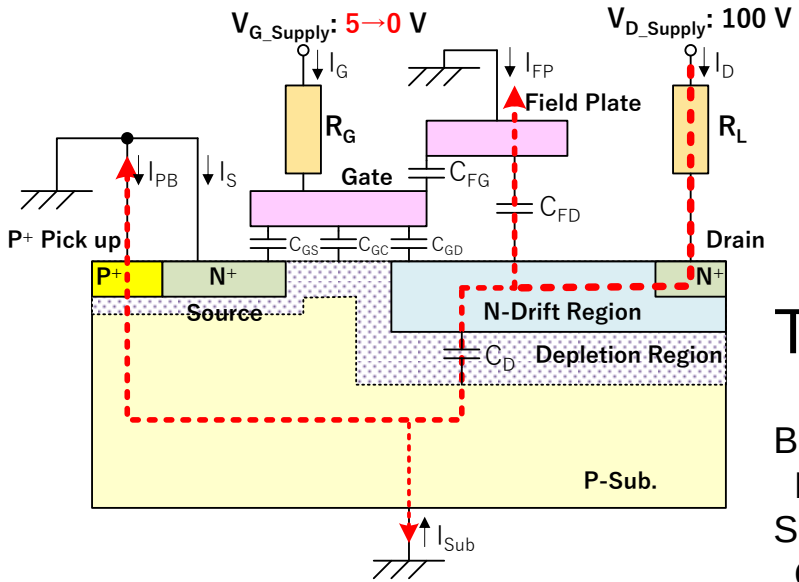
R_G: 1.31Ωmm²
R_L: 65.5Ωmm²

LDMOS layout area: 1mm²

Region ②: turn-off process

- without the Miller effect
- Displacement current ($J_{FP}+J_{PB}+J_{Sub}$) charges output capacitance (C_D+C_{FD}).
- Output capacitance is large.
  →the charging period is longer.

Region ③ is OFF state.



The current path

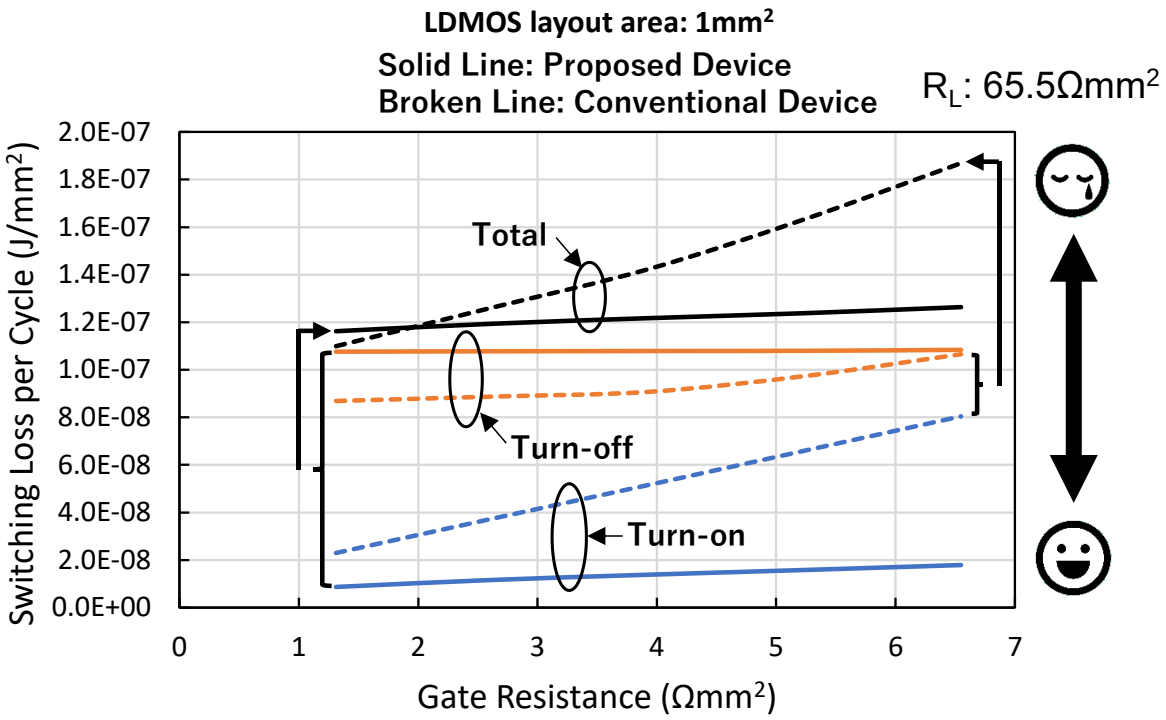
Broken Line:
Displacement Current
Solid Line:
Conducted Current

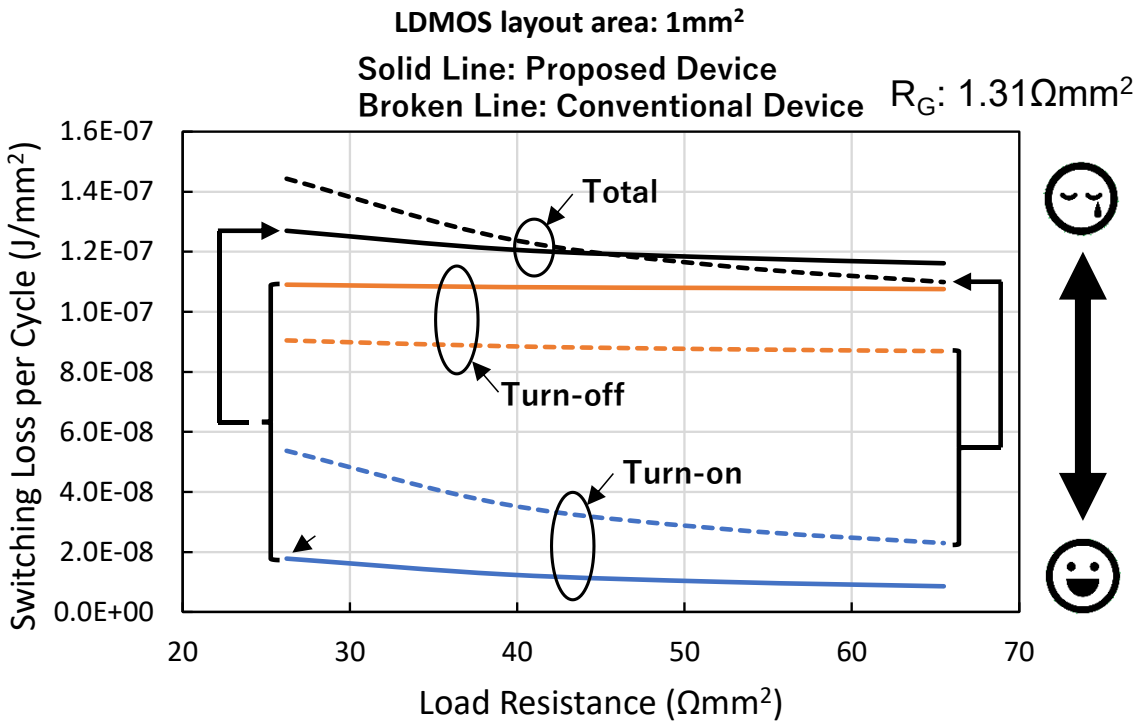
Switching losses by changing R_G&R_L

Total switching loss : Proposed < Conventional (for R_G>2 Ωmm^2 at R_L: 65.5Ωmm^2)
(for R_L<45 Ωmm^2 at R_G: 1.31Ωmm^2)

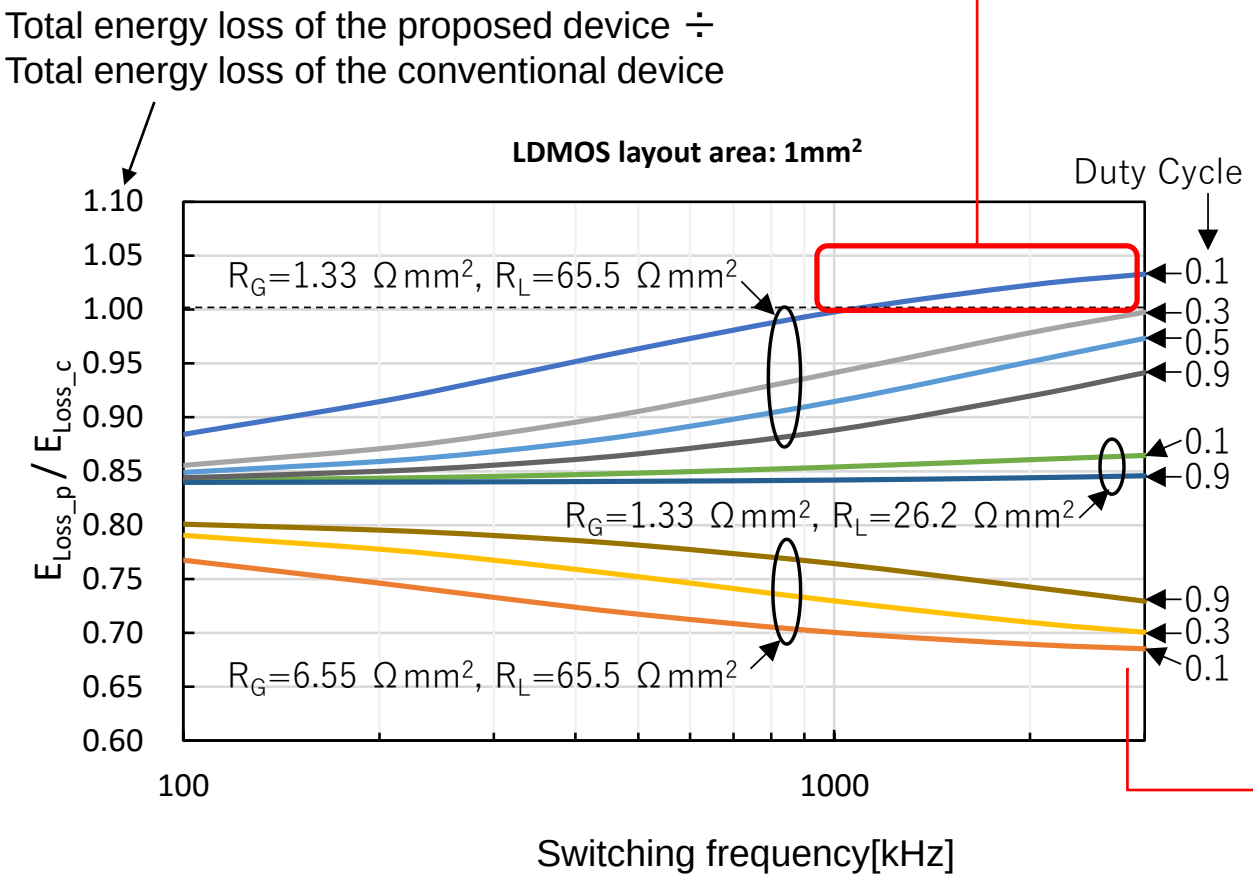
This is caused by...

- Feedback capacitance: Proposed < Conventional.
- Field plate: Proposed →large output capacitance, Conventional →large feedback capacitance.
- Specific on-resistance: Proposed (150 mΩmm^2) < Conventional (178 mΩmm^2).





Total energy loss



Only under some condition

Proposed >Conventional

- Low R_G of 1.31 Ωmm²
- High R_L of 65.5 Ωmm²
- Duty cycle D < 0.1
- Switching frequency f > 1.1 MHz

in Most practical use

Proposed < Conventional

The lowest value is 0.68 at

- R_G = 6.55 Ωmm²
- R_L = 65.5 Ωmm²
- D = 0.1
- f = 3MHz

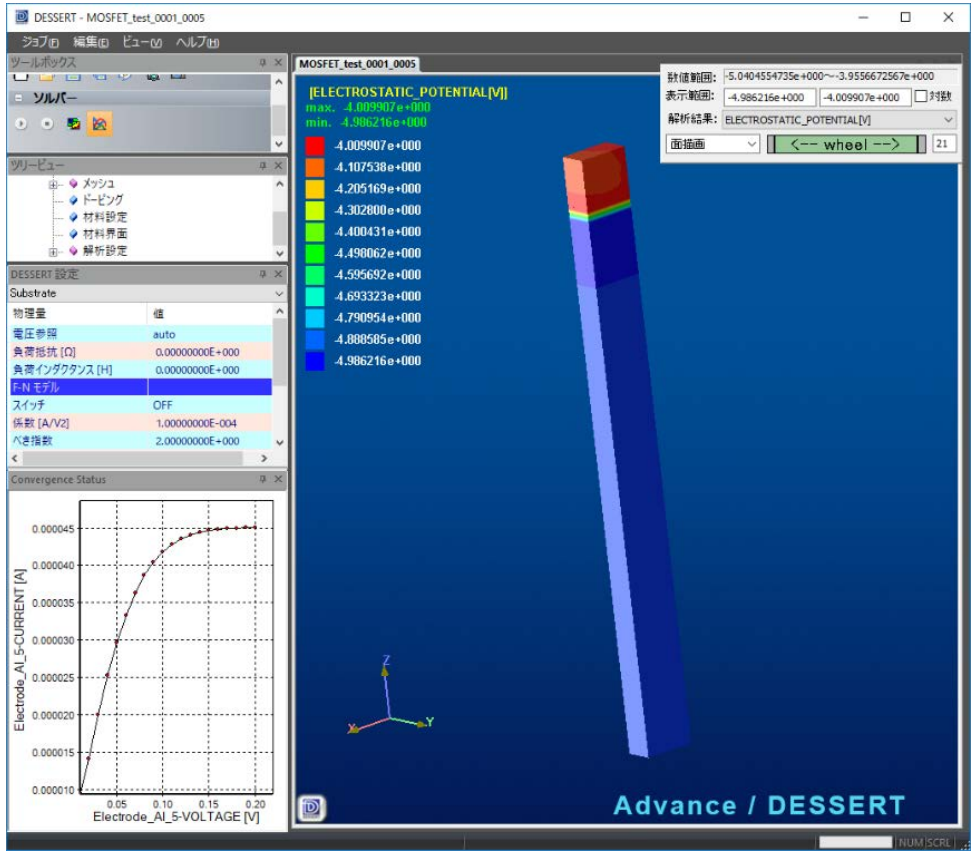
Summary

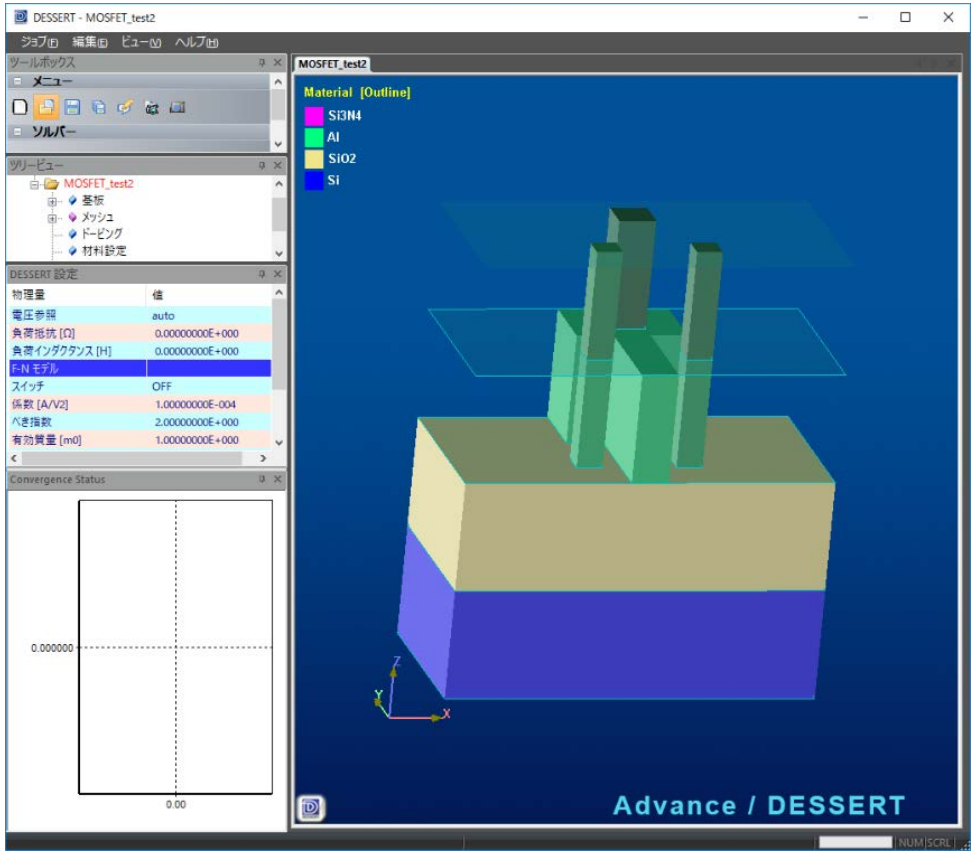
- The switching characteristics were analyzed in detail by changing R_L and R_G.

- The total energy loss (total switching loss + conduction loss)
  - Proposed > Conventional
    Only in the region of low gate resistance, light load (high resistive load), low duty cycle, and high switching frequency.
  - Proposed < Conventional (in most of the actual use range)
- This is caused by...
  - Feedback capacitance: Proposed < Conventional.
  - Field plate: Proposed →large output capacitance
    Conventional →large feedback capacitance.
  - Specific on-resistance: Proposed (150 $m\Omega mm^2$) < Conventional (178 $m\Omega mm^2$).

Acknowledgments

We would like to express sincere thanks to AdvanceSoft Corporation
for providing us some licenses of using a 3D TCAD simulator.
The development of this simulator is assisted by Japan Science and Technology Agency, National Research and Development Agency using A-STEP program.





https://www.advancesoft.jp