Ph. D. Dissertation Title:

ΔΣ ADC Linearity Testing Technology and Floating-Point Arithmetic Algorithms with Taylor-Series Expansion

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Ph. D. Dissertation summary

In this dissertation, two research results related to LSI testing technologies are described. (i) One is fast integral nonlinearity (INL) testing technology of the ΔΣ analog-to-digital converter (ADC) with our proposed FFT method. The ΔΣ ADC is now widely used in sensor interface circuits of IoT systems. It is high-precision but its sampling speed is very slow so that its direct INL testing time takes very long time and then its INL testing is usually omitted at mass production shipping. However, due to the demands for low-cost-yet-highly-reliable IoT systems, its short time testing is now needed, and we have developed its solution. (ii) The second is fast floating-point algorithms for division, inverse square root, logarithm, and exponential calculations, using Tayler-series expansion with the proposed mantissa region division and conversion methods; these algorithms can be used for digital signal processing in ATE systems.

(1) ΔΣAD converter test technology:

We describe a mass production testing methodology for INL of a high precision ΔΣ ADC in short time. We consider its INL testing by separating its analog and digital parts: ΔΣ AD modulator and digital filter. The digital filter can be tested with the scan-path method. For the AD modulator part, its nonlinear curve of the DC input-output characteristics can be obtained using a DC input varying with a fine step, but it takes an enormously long time; it is not practical for mass production testing. So we consider a polynomial model of the ΔΣ AD modulator input-output (I/O) characteristics and estimate its coefficient values from the fundamental and harmonics power by applying a cosine input and obtaining the modulator 1-bit output power spectrum with FFT. Its INL can be estimated from the coefficients accurately when the modulator I/O characteristics is continuous. Our simulation and experimental results show that significant testing time reduction can be achieved with the proposed method; in 7-sps 24-bit ΔΣ ADC case, its test time is reduced from 111 days to 32 seconds.

(2) Floating-point Arithmetic with Taylor-series Expansion:

We have developed floating-point digital arithmetic algorithms to deal with division, inverse square root, logarithm and exponential calculation, using Taylor-series expansion. Three methods are proposed for fast calculation with high efficiency: (i) mantissa region uniform division, (ii) mantissa region non-uniform division and (iii) mantissa region conversion. We have clarified the Taylor-series expansion calculation algorithm trade-offs among accuracy, numbers of multiplications/additions/ subtractions and LUT sizes; the designer can choose the optimal algorithm for ATE systems.

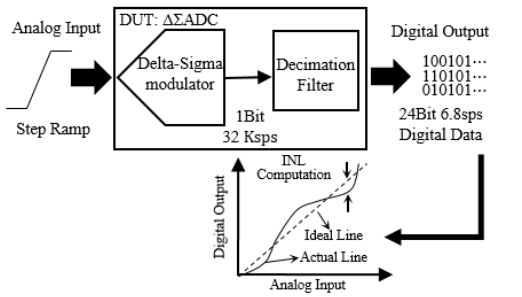

Fig. 1 Conventional ΔΣADC INL testing with all codes.

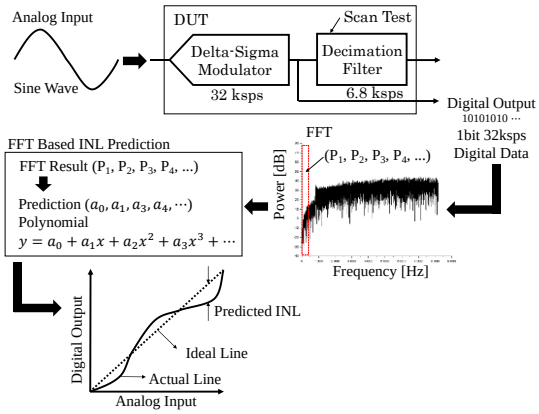

Fig. 2 Proposed FFT-based ΔΣADC INL prediction method.

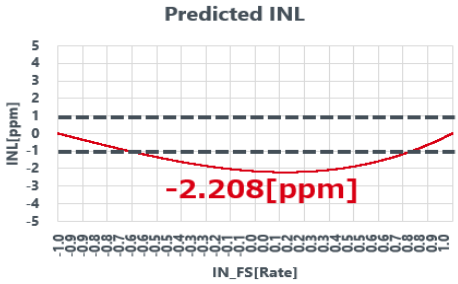

Fig. 3 Obtained INL prediction with the proposed method for an actual 7-sps 24bit ΔΣADC chip.

Publications – ADC test technology

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[7] K. Sato, T. Ishida, T. Okamoto, T. Ichikawa, Jiang-Lin Wei, T. Nakatani, Y. Zhao, S. Katayama, S. Yamamoto, A. Kuwana, K. Hatayama, H. Kobayashi, "Revisit to Accurate ADC Testing with Incoherent Sampling Using Proper Sinusoidal Signal and Sampling Frequencies", 51st IEEE International Test Conference, Oct. 2021 (accepted)

[8] K. Sato, T. Ishida, T. Okamoto, T. Ichikawa, Jiang-Lin Wei, N. Kushita, H. Arai, A. Kuwana, T. Nakatani, K. Hatayama, H. Kobayashi, "An FFT-based INL Prediction Methodology for Low Sampling Rate and High Resolution Analog-to-Digital Converter", IP Session 9C: Innovative Test Practices in Japan, IEEE VLSI Test Symposium, April 2019.

Publications – Floating-Point Calculation Algorithm

[1] Jiang-Lin Wei, A. Kuwana, H. Kobayashi, K. Kubo, Y. Tanaka, "Floating-Point Inverse Square Root Algorithm Based on Taylor-Series Expansion", IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 68, Issue 7, pp. 2640-2644, July. 2021.

[2] Jiang-Lin Wei, A. Kuwana, H. Kobayashi, K. Kubo,"Divide and Conquer: Floating-Point Exponential Calculation Based on Taylor-Series Expansion", IEEE 14th International Conference on ASIC, Oct. 2021. (accepted)

[3] Jiang-Lin Wei, A. Kuwana, H. Kobayashi,K. Kubo, Y. Tanaka, "Floating-Point Square Root Calculation Algorithm Based on Taylor-Series Expansion and Region Division", IEEE 64th International Midwest Symposium on Circuits and Systems, Aug. 2021.

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[5] Jiang-Lin Wei, A. Kuwana, H. Kobayashi, K. Kubo, "Revisit to Floating-Point Division Algorithm Based on Taylor-Series Expansion", 16th IEEE Asia Pacific Conference on Circuits and Systems, Dec. 2020.