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Design Considerations for MOS Peaking Current Sources Insensitive to Supply Voltage and Temperature

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Outline

- Research Objective
- Peaking Current Source
- Drain Current Temperature Characteristics
- Single-Peak Current Sources
- Multiple-peak current Sources
- Conclusion

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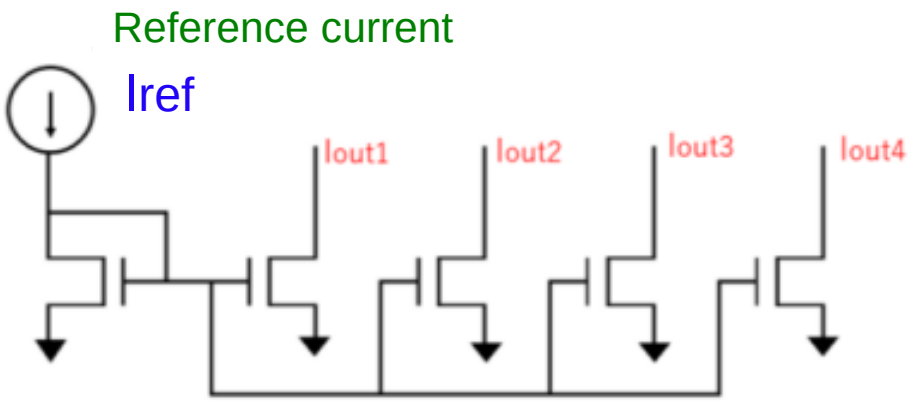
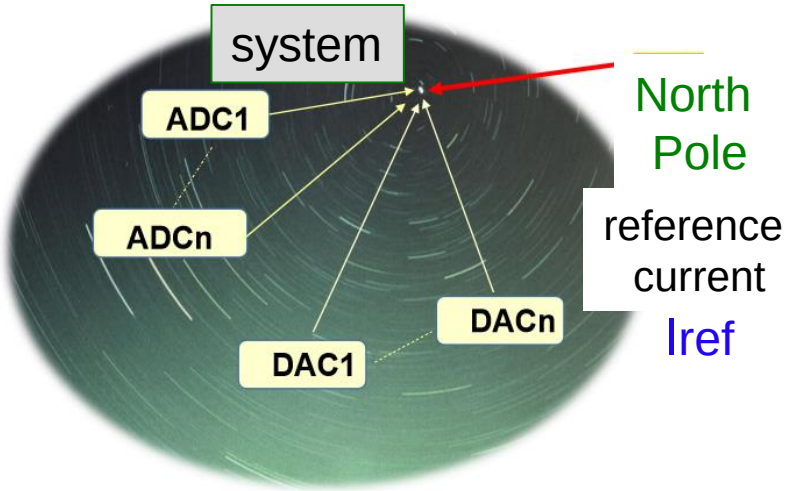
Research Objective

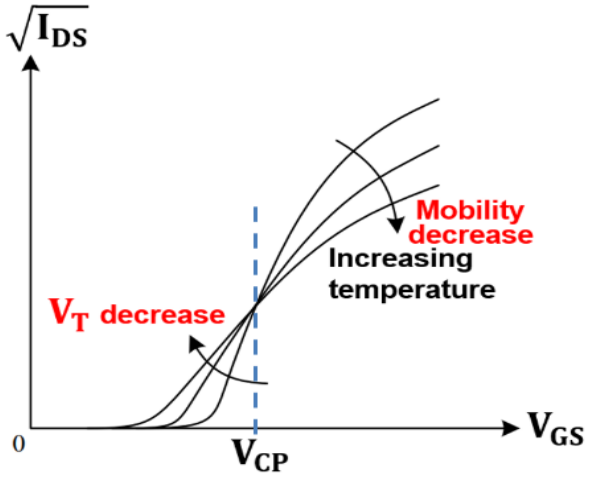
Development of reference current source insensitive to temperature and supply voltage with simple CMOS circuit.



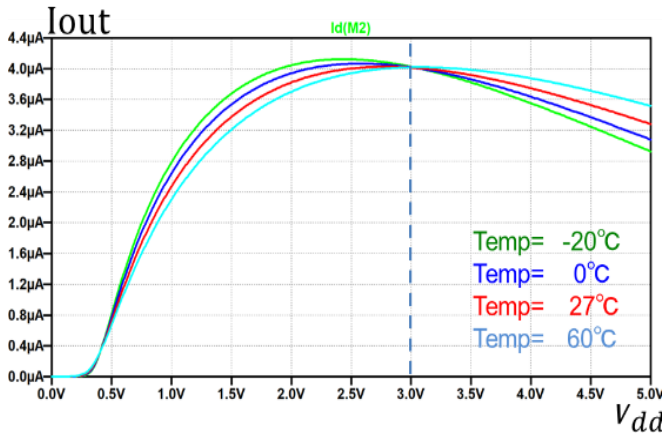


Our Approach

- Realization of MOS peaking current sources insensitive to temperature and supply voltage.
- Clarification of drain current temperature characteristics cross-point gate voltage (V_{CP})
- Obtain design guideline.



NMOS drain current



Current source insensitive to temperature and supply voltage

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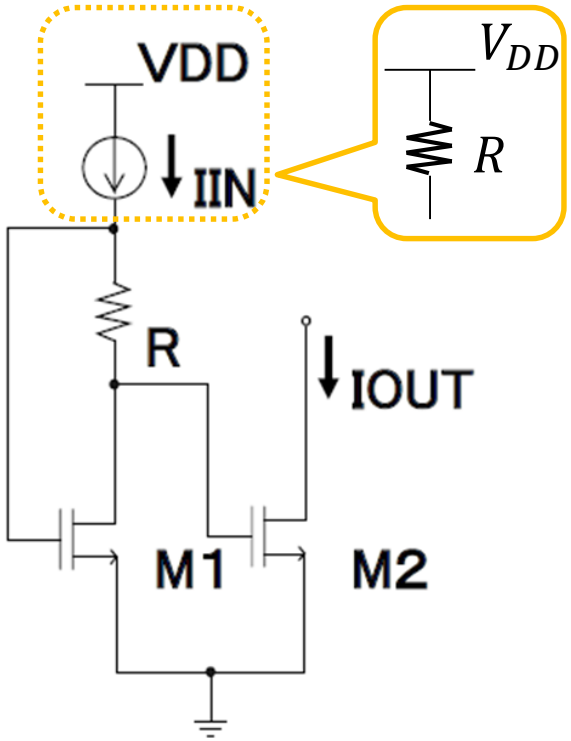
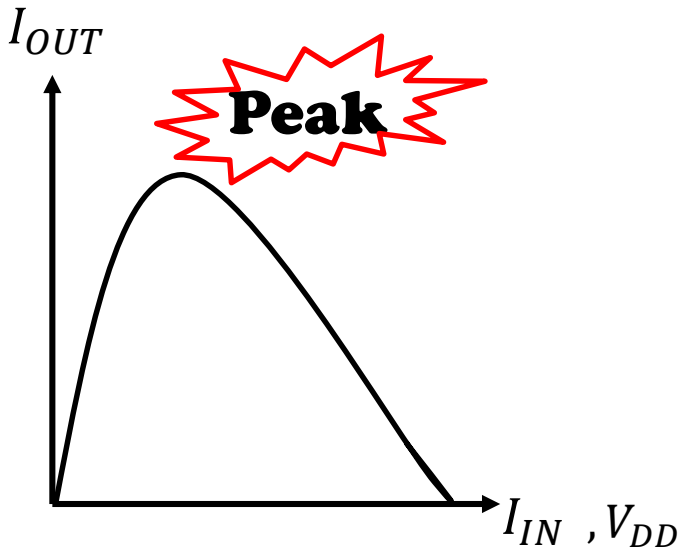
Original Nagata Current Mirror



MOS Nagata
Current Mirror Circuit



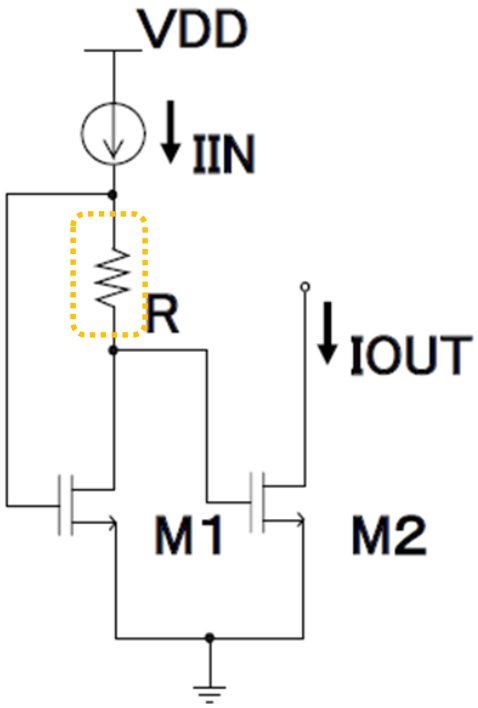
Peaking current characteristics

At peak vicinity

Small output current change
against input current change

Simple ⇨ Widely used. Ex: in DC-DC converter ICs

Circuit Configuration and Operation(1)

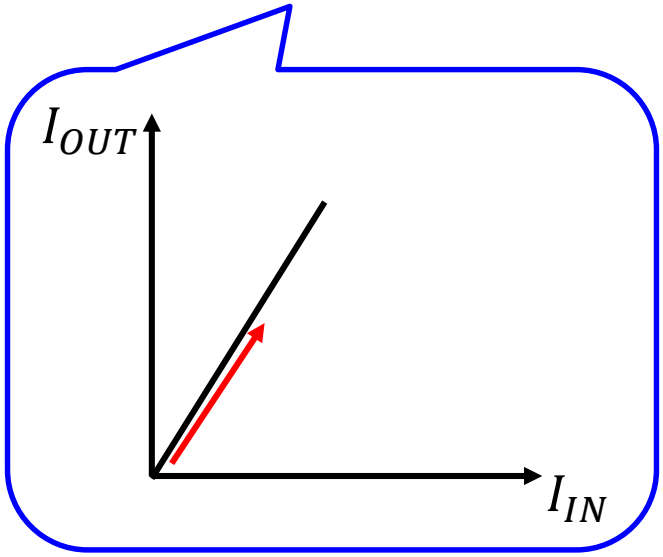


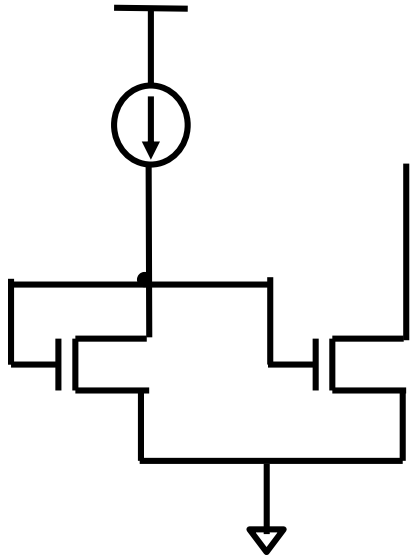
MOS Nagata
Current Mirror

I_{IN}: small

RI_{IN}: small

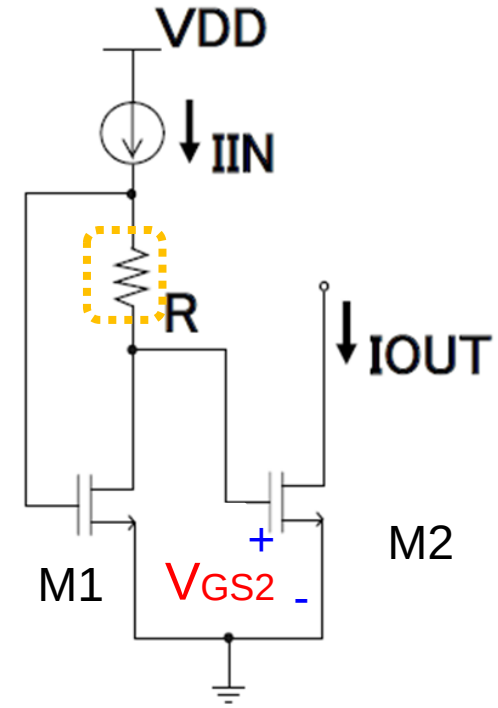
$I_{IN} = I_{OUT}$





Current Mirror

Circuit Configuration and Operation(2)

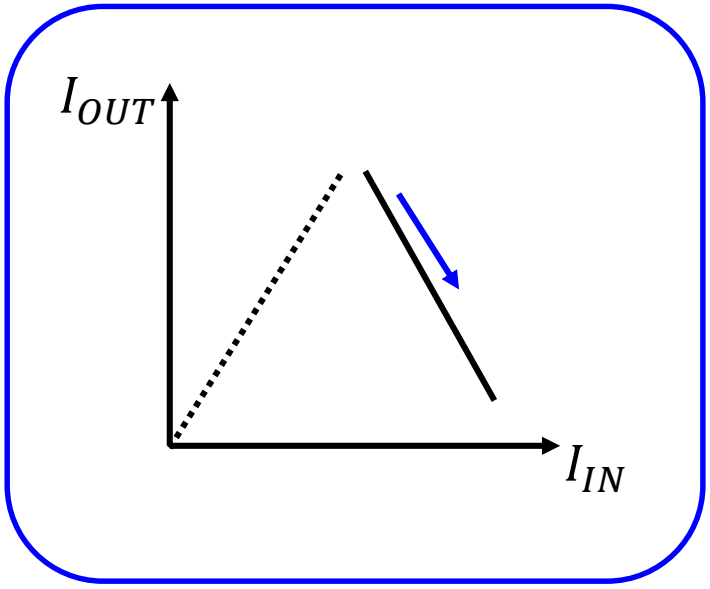


MOS Nagata
Current Mirror Circuit

➡ I_{IN}: $large$

➡ RI_{IN}: $large$

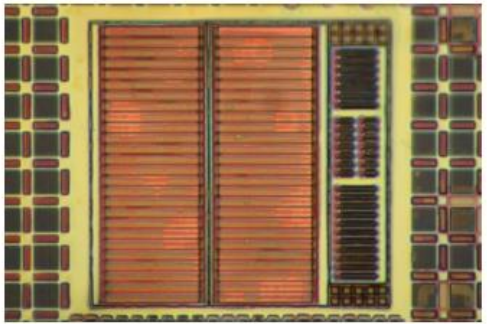
➡ V_{GS2} $becomes$ $smaller$



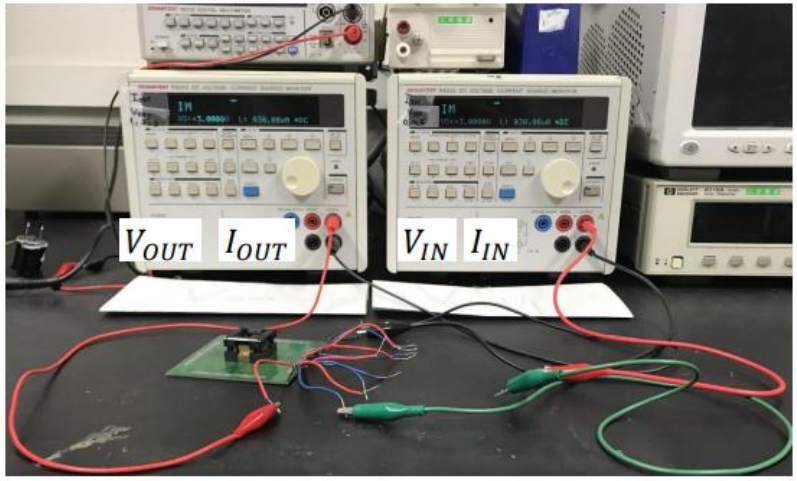
Temperature characteristics should be also considered.

Need for Temperature Care

Layout by
ASO Corp.

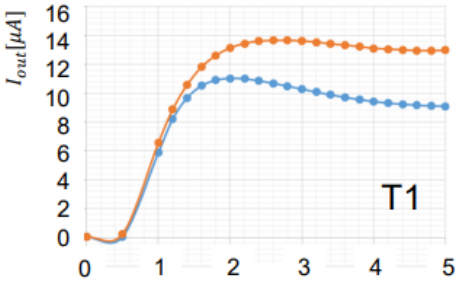


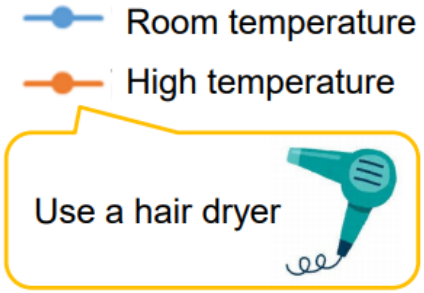
Our first prototype chip

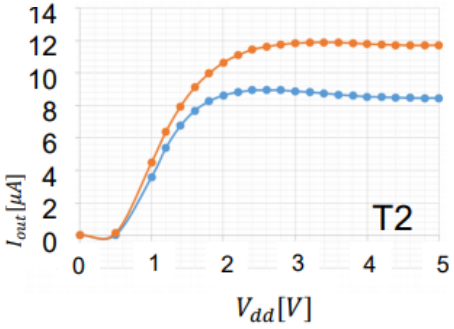


Measurement environment

- Insensitive to supply voltage
- Sensitive to temperature







[1] M. Hirano, et. al., “Silicon Verification of Improved Nagata Current Mirrors”, IEEE ICSICT(Nov. 2018)

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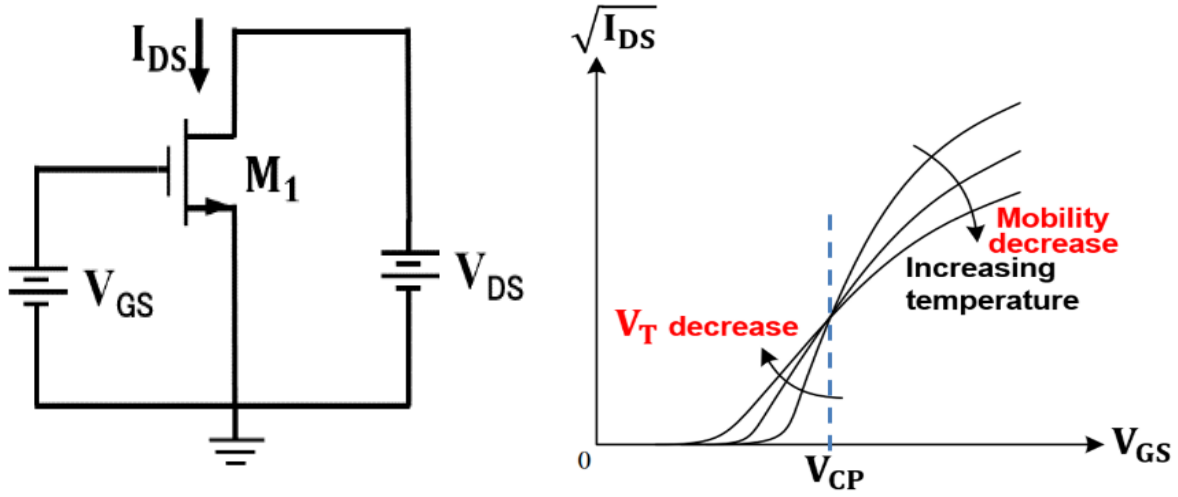
Drain Current Temperature Characteristics



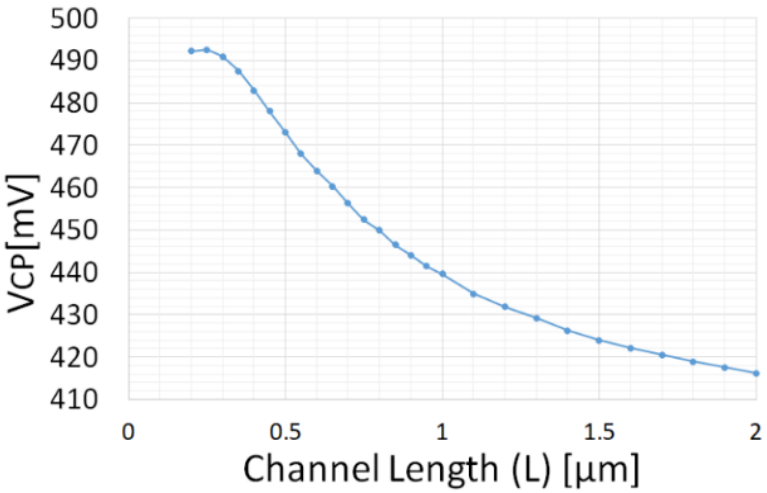
NMOS drain current temperature characteristics

- For $V_{GS} = V_{CP}$, I_{DS} is insensitive to temperature.
  - At high temperature,

    For $V_{GS} < V_{CP}$, I_{DS} becomes larger

    For $V_{GS} > V_{CP}$, I_{DS} becomes smaller.

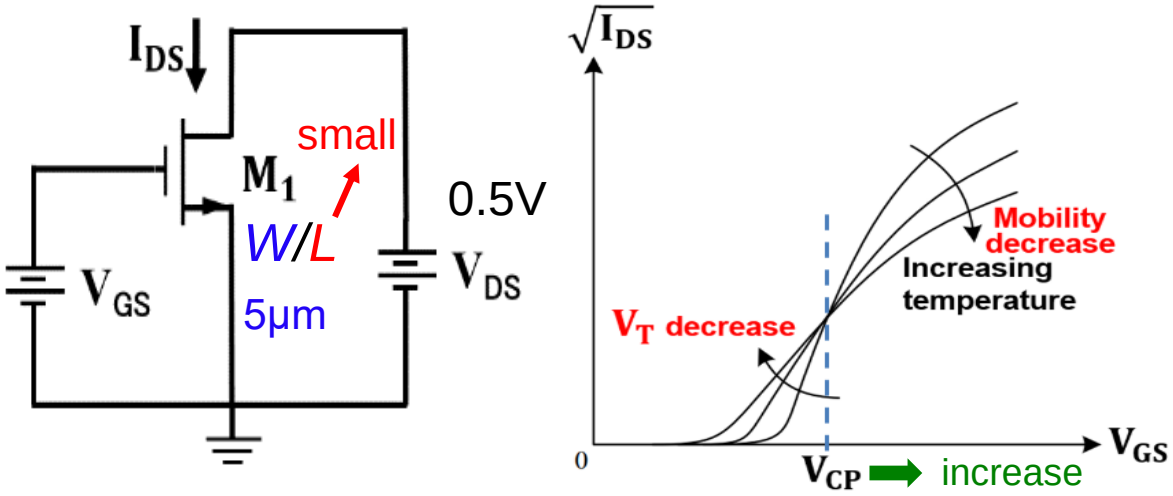
V_{CP} and Small Channel Length L



SPICE simulation result
with BSIM3v3 model parameters

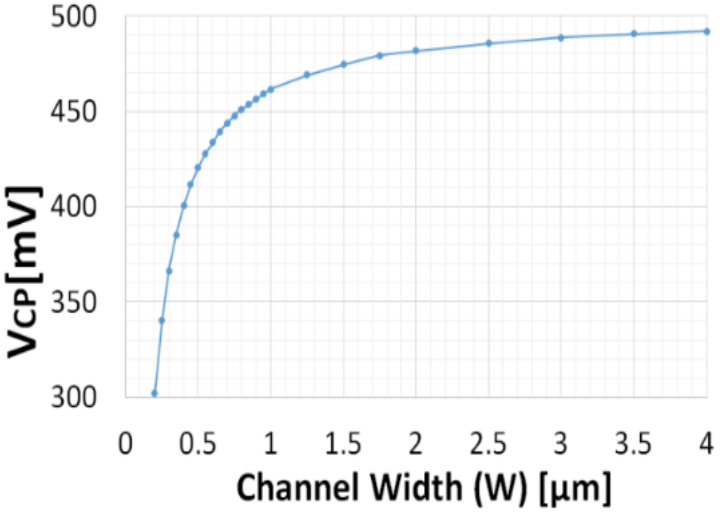
L → small ➡ V_{CP} → increase

Explained by **short channel effect**



NMOS drain current temperature characteristics

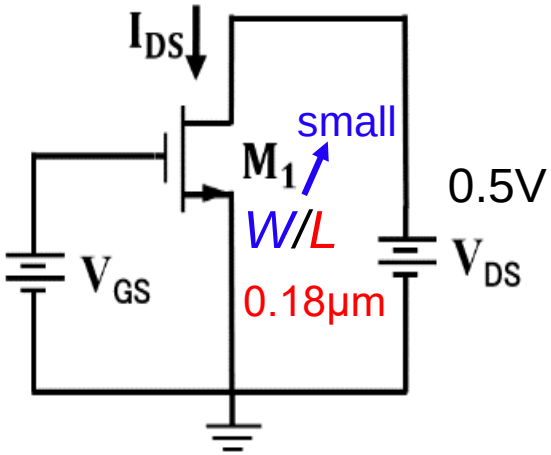
VCP and Small Channel Width *W*

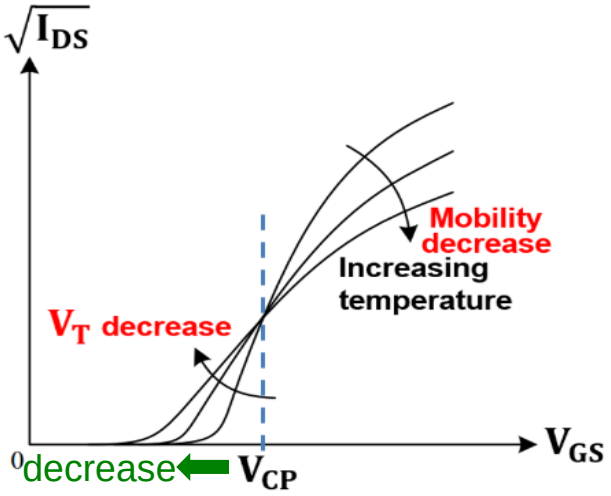


SPICE simulation result
with BSIM3v3 model parameters

W → small ➡ VCP → decrease

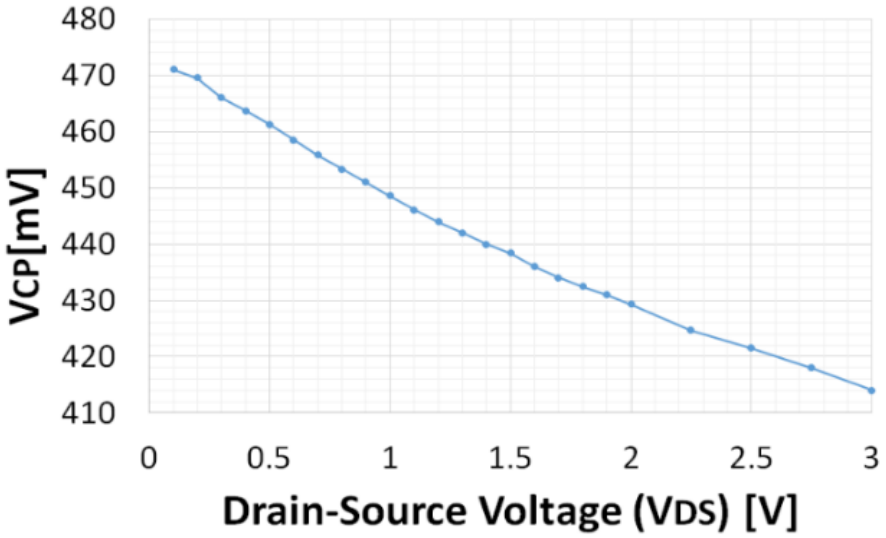
Explained by narrow channel effect





NMOS drain current temperature characteristics

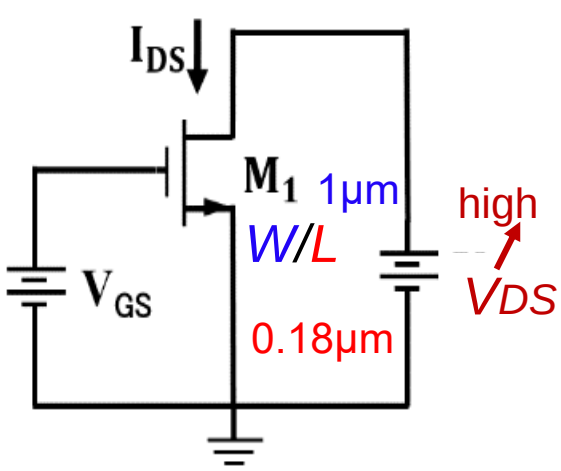
V_{CP} and Drain-Source Voltage V_{DS}

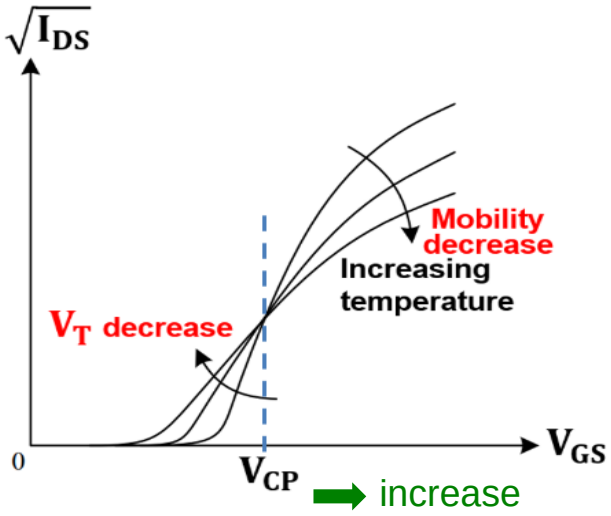


SPICE simulation result
with BSIM3v3 model parameters

V_{DS} → small ⇒ V_{CP} → increase

Explained by
drain induced barrier lowering *(DIBL)*





NMOS drain current temperature characteristics

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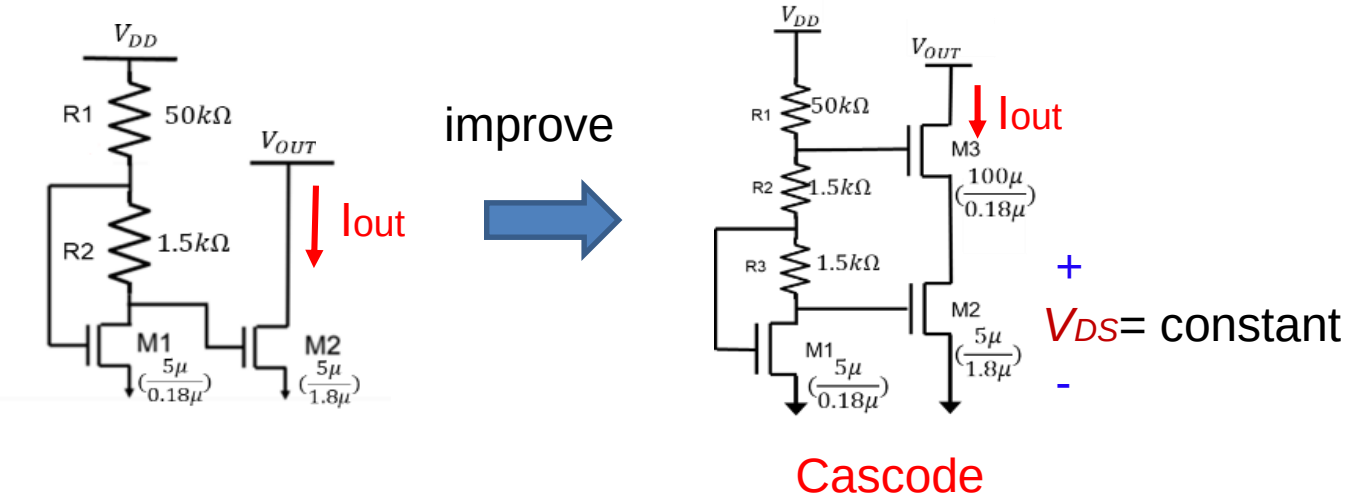
Temperature Insensitive Current Source

Design guideline

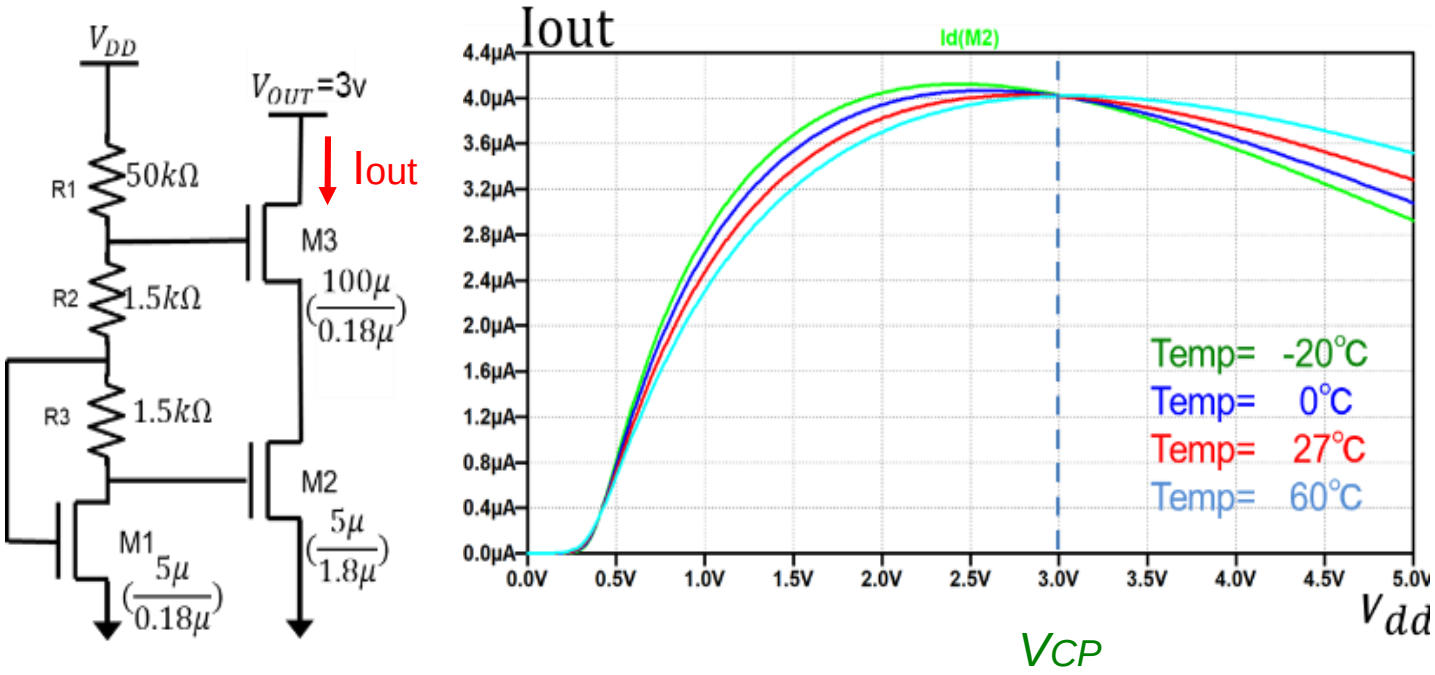
- Channel length *L* should be long enough.
  If short, process variation for *L*+*ΔL*, *VCP* varies a lot.

- Channel width *W* should be wide enough.
  If narrow, process variation for *W*+*ΔW*, *VCP* varies a lot.

- Drain-source voltage *VDS* should be constant.
  such as using cascode circuit.



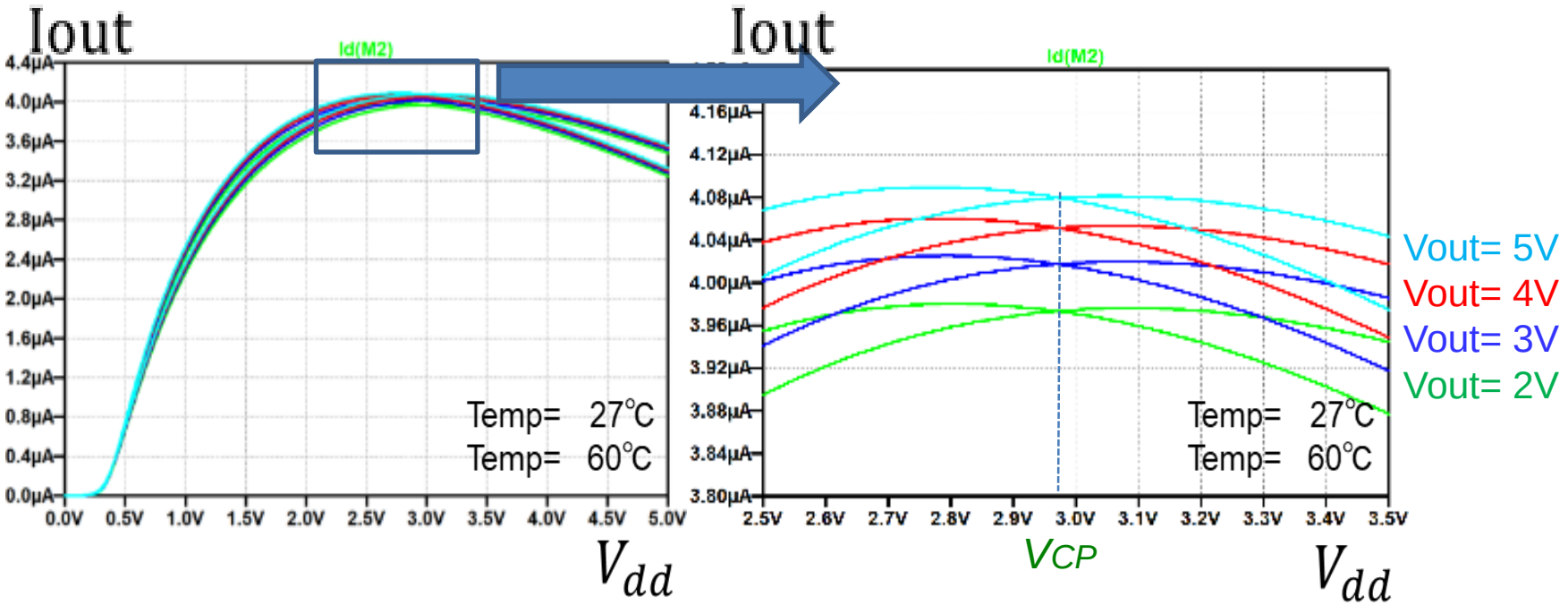
NMOS Single-Peak Cascode Circuit



NMOS cascode single-peak current source

- Temperature insensitivity point (V_{CP}) exists
- Output current Iout is insensitive also to the supply voltage (V_{DD}).

NMOS Single-Peak Cascode Result

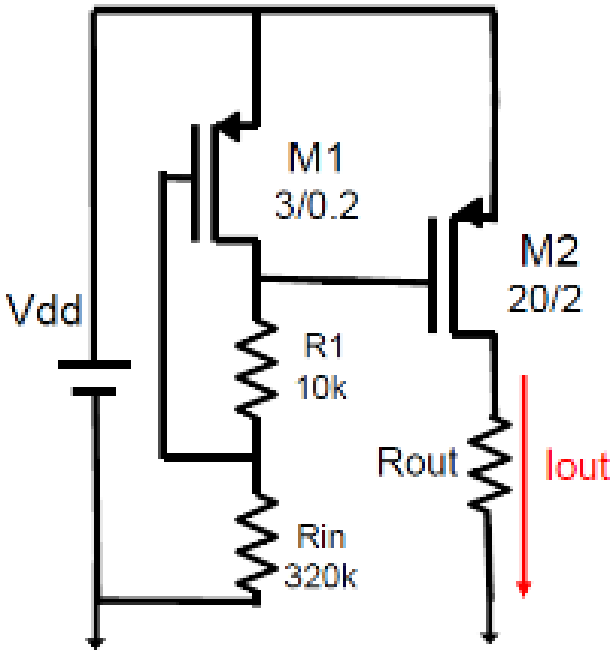


NMOS cascade circuit simulation results
for several output voltages (VOUT) at 27℃, 60℃.

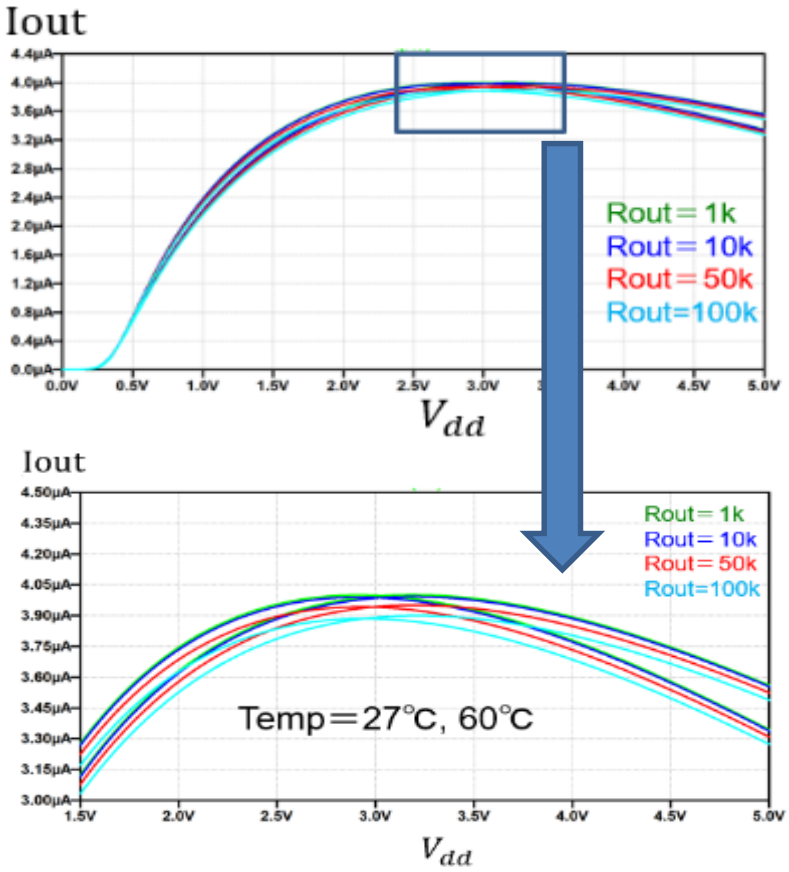
Even when *VOUT* changes

- Temperature insensitivity point (*VCP*) does NOT change.
- M2 drain voltage keeps constant.

PMOS Single-Peak Current Source



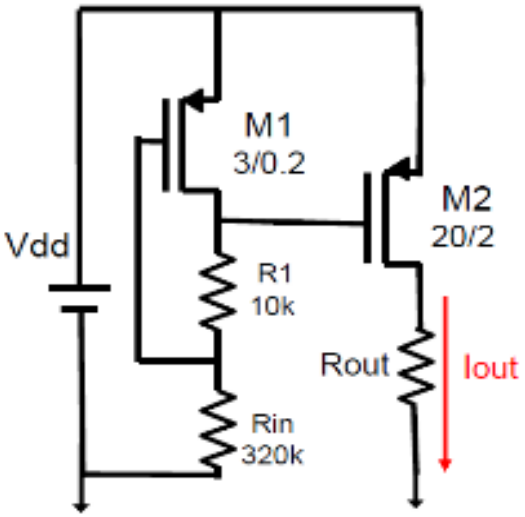
PMOS Nagata Current Source



when the load resistor (Rout) is changed,
drain voltage of M2 changes and Iout changes

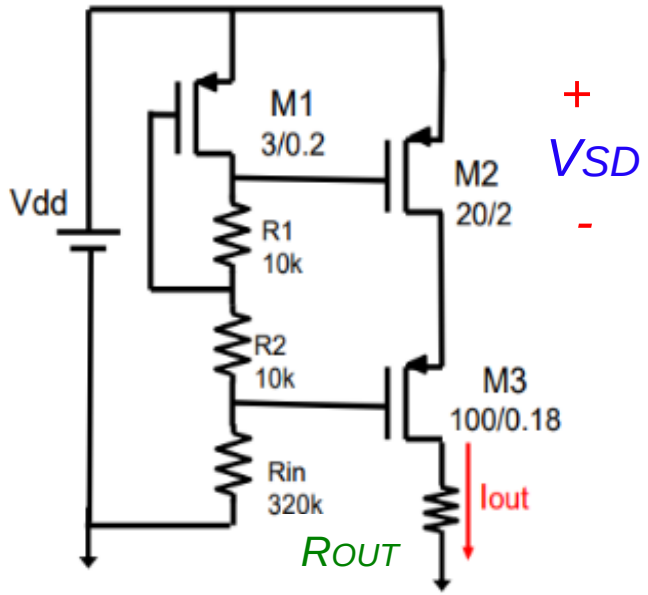
using cascode circuit

PMOS Circuit Improvement



PMOS Nagata current source

improve

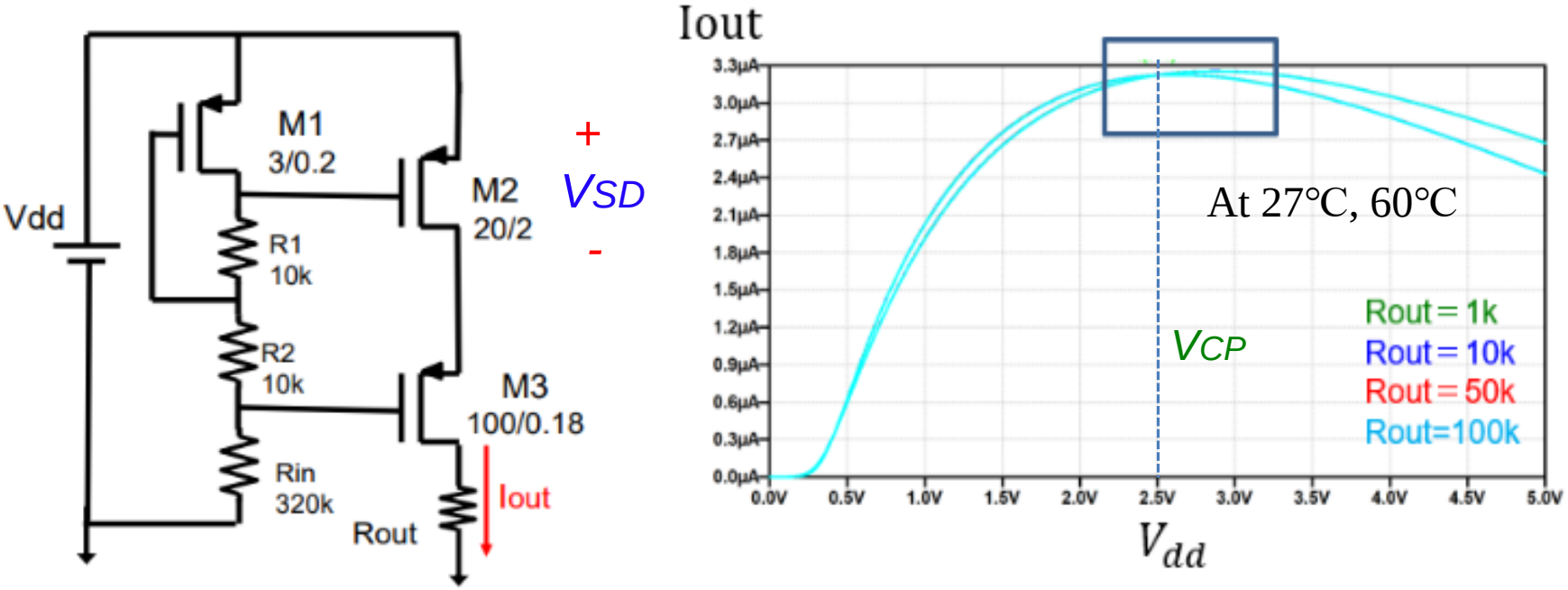


PMOS single-peak cascode circuit

Even when R_{OUT} changes,

M2 drain voltage (V_{SD}) keeps constant, thanks to cascade.

PMOS Single-Peak Cascode Circuit



PMOS cascode single-peak current source

Even when *ROUT* changes

- Temperature insensitivity point (*VCP*) does NOT change.

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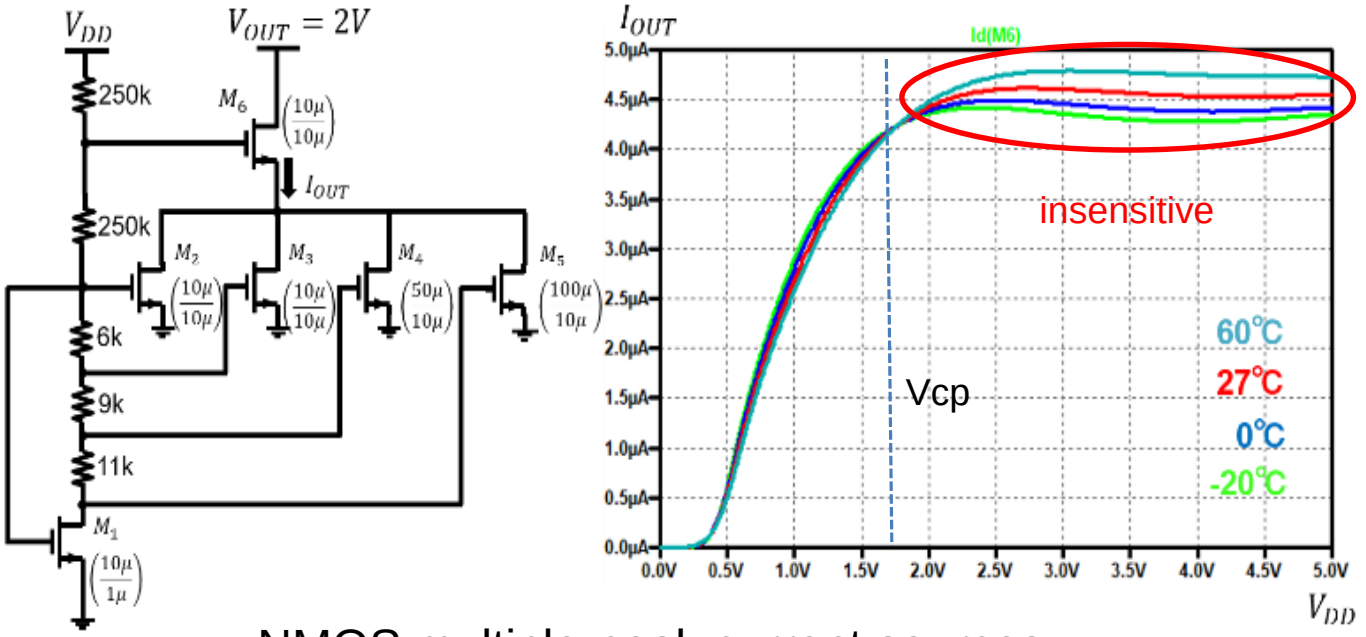
NMOS Multiple-Peak Current Sources



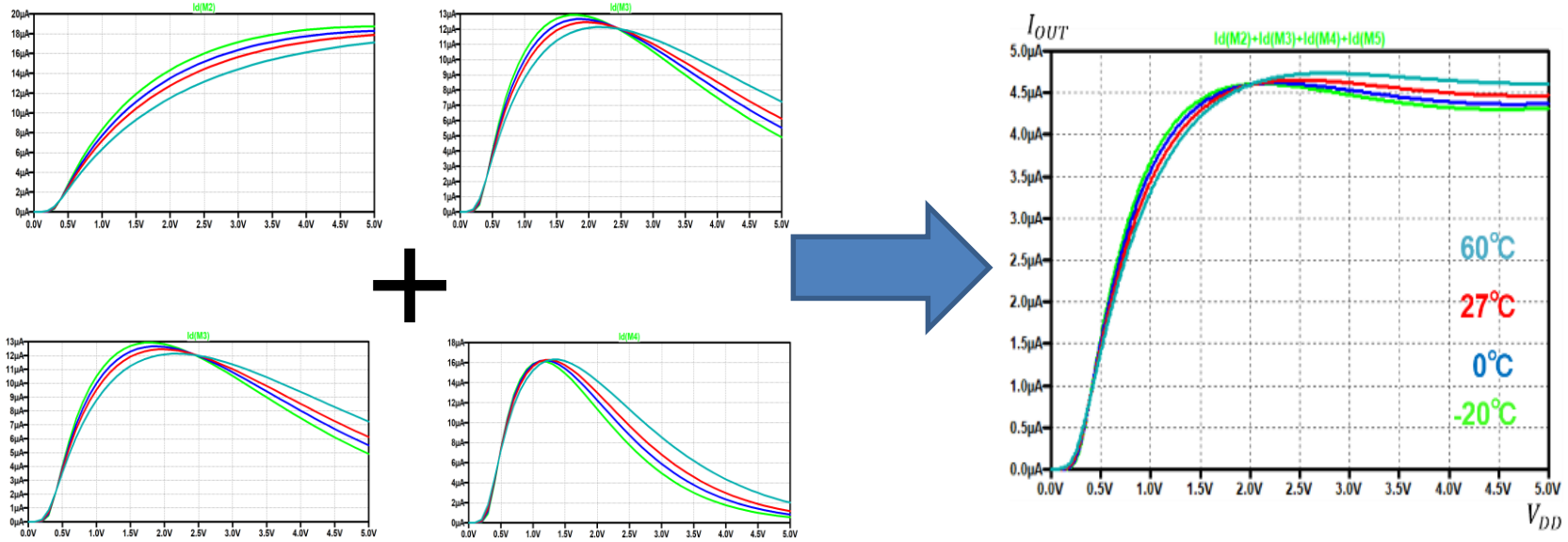
NMOS multiple-peak current sources

- Output current is insensitive to supply voltage.
- Temperature variations with supply voltage more than 2.0V.

Multiple-Peak Circuit Design

Use of multiple peaking current sources

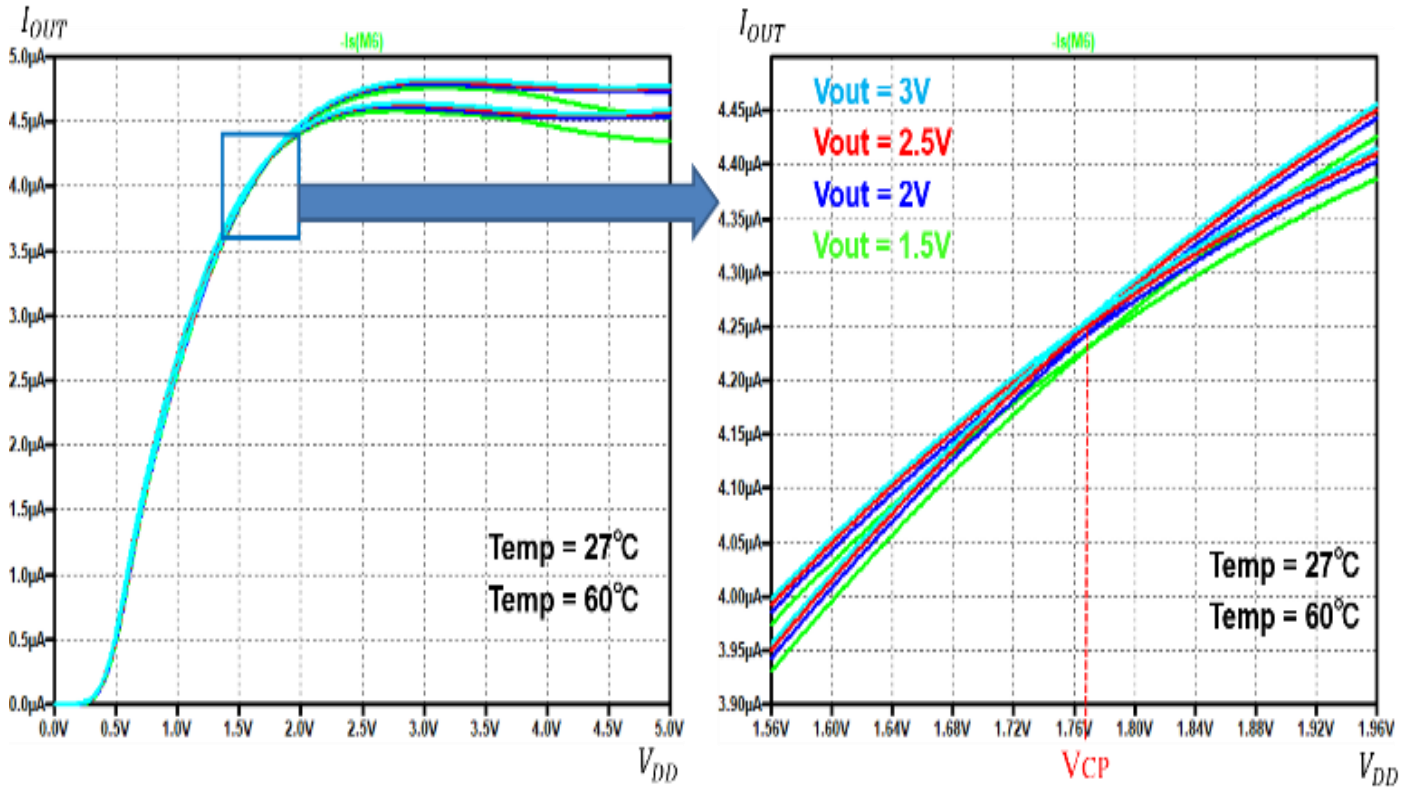
Current source design is relatively easy.



Multiple peaks ⇒

Total current is insensitive to supply voltage and temperature.

NMOS Multiple-Peak Current Source Result



Even when *VOUT* changes

- Temperature insensitivity point (*VCP*) does NOT change.
- M2 drain voltage keeps constant.

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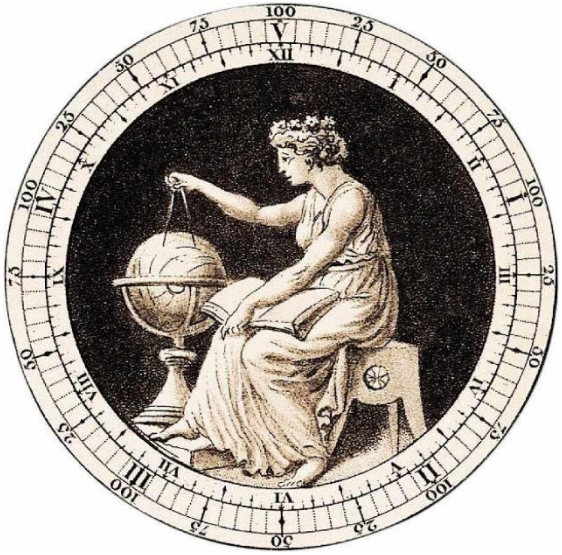
Conclusion

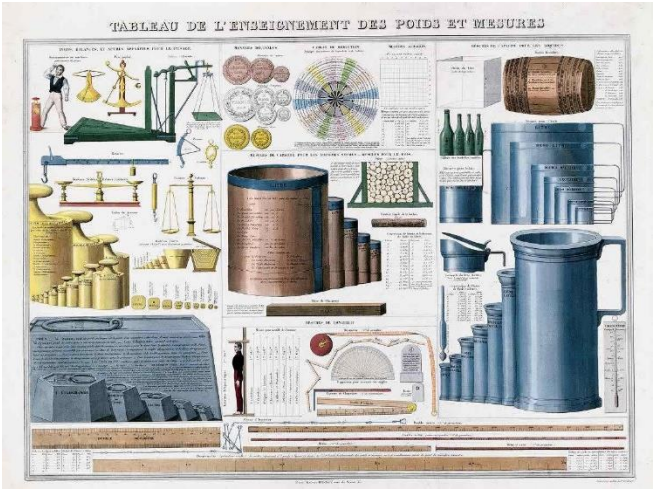
- MOS peaking current sources
  insensitive to supply voltage and temperature
- Both NMOS and PMOS types
- Resistor temperature coefficients can be positive, zero or negative
  if they are known a priori.
- Design guideline :

  Use enough L, W and keep V_{DS} constant.
- Knowledge of CMOS device physics and modeling as well as circuit
  is useful.

Q&A

Reference and standard are important !





Metric System at French Revolution

Thank you very much

群馬大学
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