Two-Step Incremental ADC Architecture With Self-Calibration of Two Reference Voltages Ratio

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OUTLINE

- Research Background and Objective
- 2-step Incremental ADC:
  - Configuration and Operation
  - Effect of Clock Periods for 1st, 2nd Steps
  - 2nd Reference Voltage V_{r2}
- Proposed Self-Calibration:
  - Configuration and Operation
  - Simulation Verification
- Conclusion

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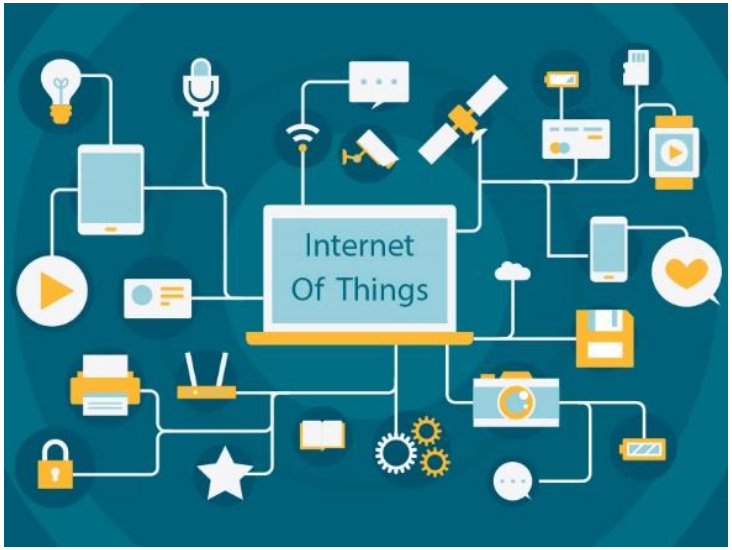
Research Background

IoT systems are everywhere



Integrated sensors

ADCs are key elements
in sensor interface circuit

Incremental ADCs receive a lot of attention
because of circuit simplicity, low power and high accuracy

Research Objective

- 1-step incremental ADC
  - 🙂 - Circuit simplicity
  - 😥 - Long conversion time

↓

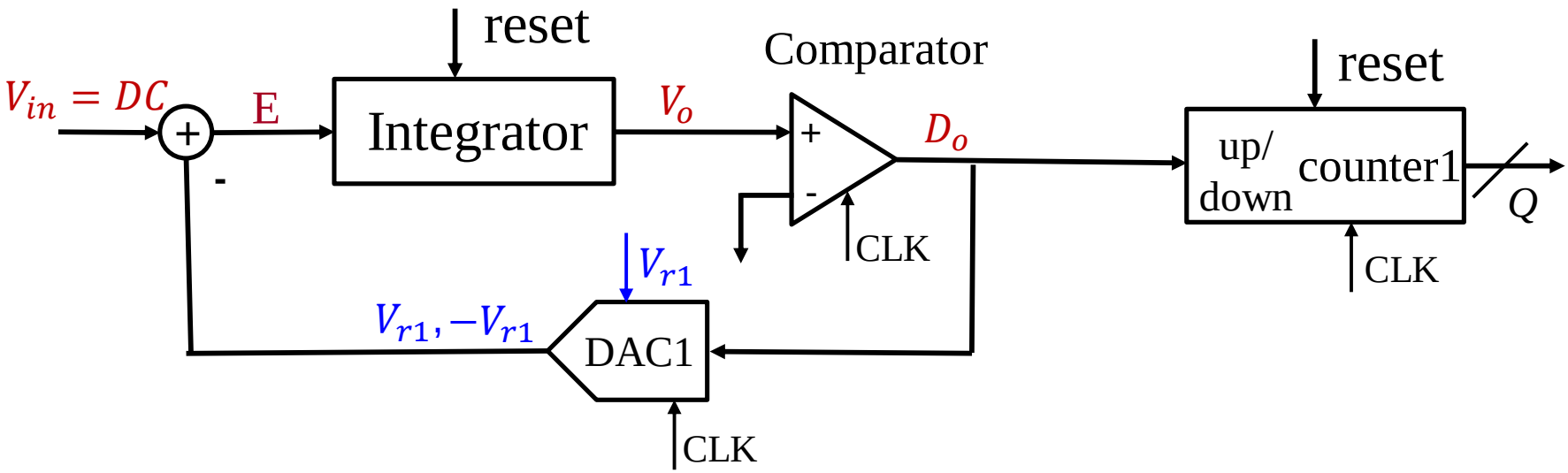
- 2-step incremental ADC
  - 🙂 - Short conversion time
  - 😥 - Nonlinearity due to 1st and 2nd steps mismatch.

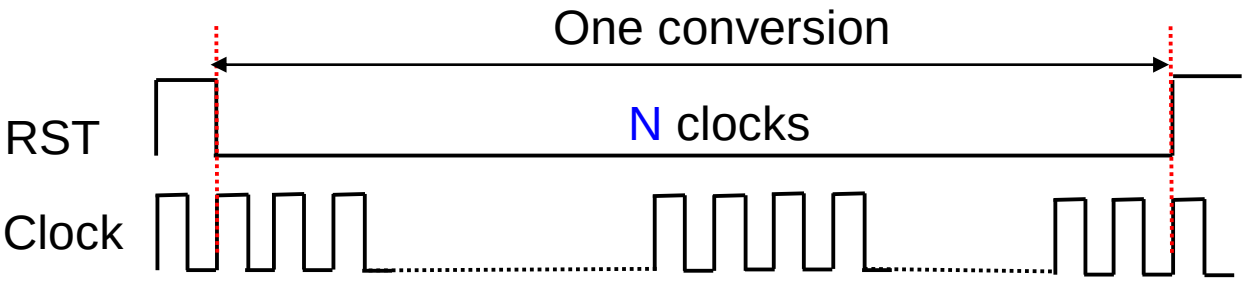
↓

Objective:
- 2-step incremental ADC with its behavioral simulation
- Proposal of self-calibration method for mismatch compensation.

What is Incremental ADC ?

- ΔΣ AD modulator + Reset
- Nyquist-Rate ADC, NOT Oversampling ADC





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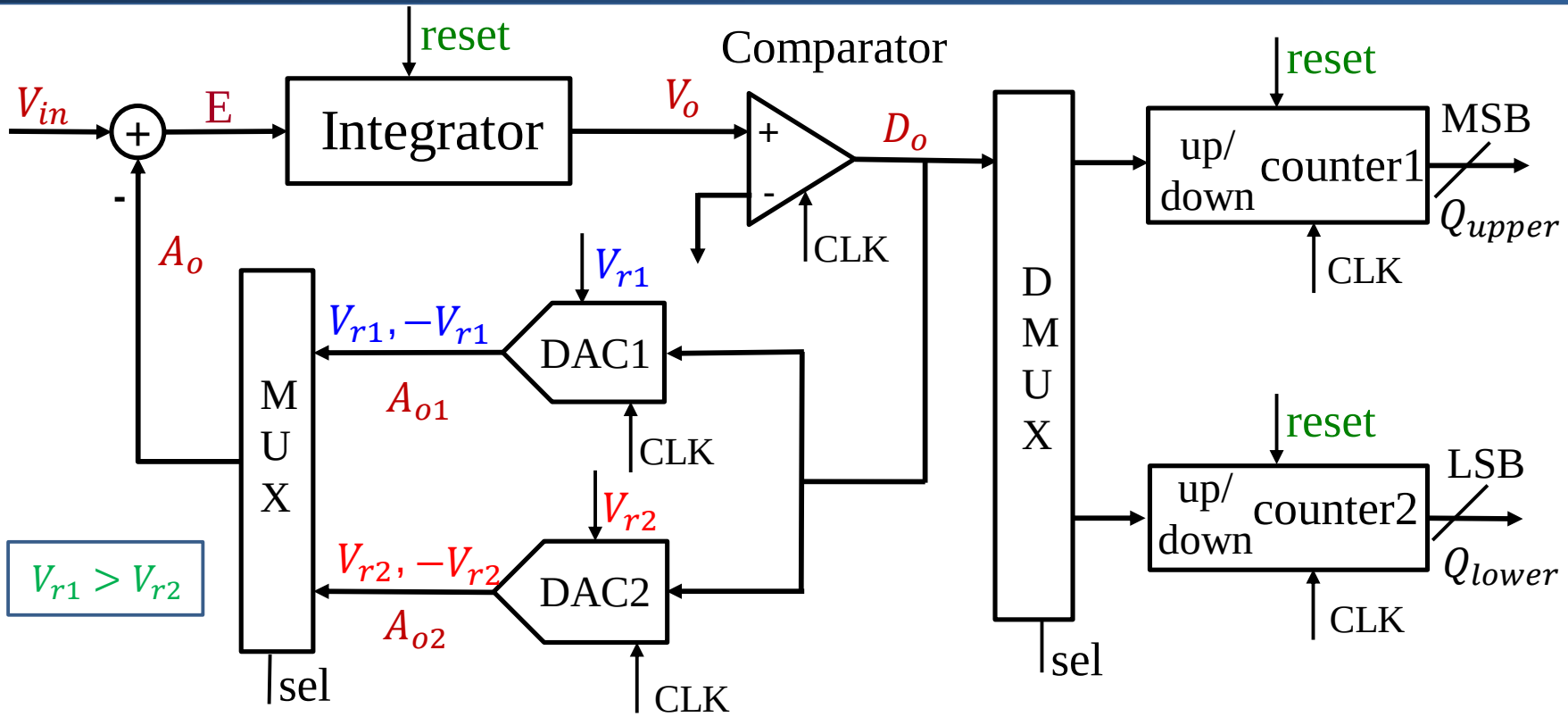
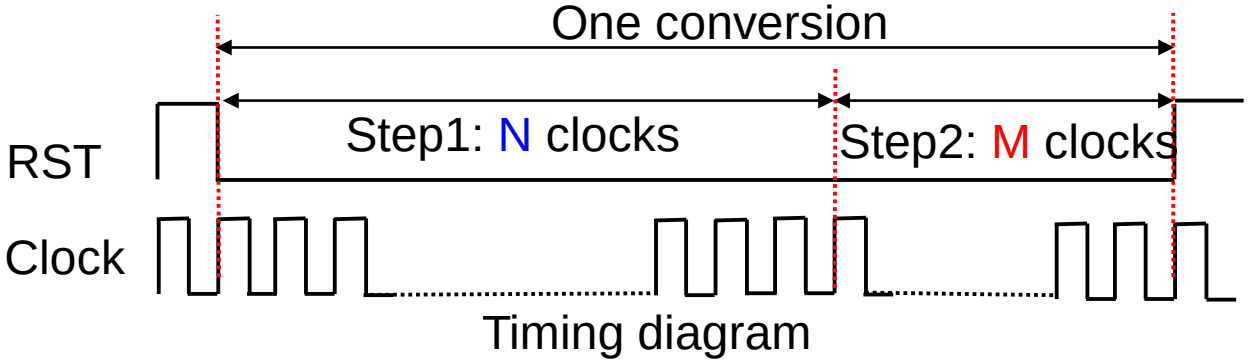
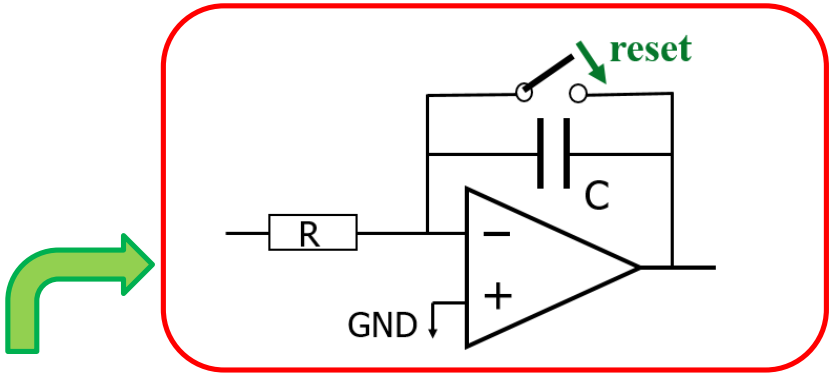
2-Step Incremental ADC





Reset Operation



reset

$V_{in} = DC$

E

Integrator

V_o

Comparator

D_o

CLK

reset

MSB

up/ down

counter1

Q_{upper}

CLK

-

A_o

V_{r1}

$V_{r1}, -V_{r1}$

DAC1

A_{o1}

CLK

M U X

D M U X

V_{r2}

$V_{r2}, -V_{r2}$

DAC2

A_{o2}

CLK

sel

sel

$V_{r1} > V_{r2}$

reset

LSB

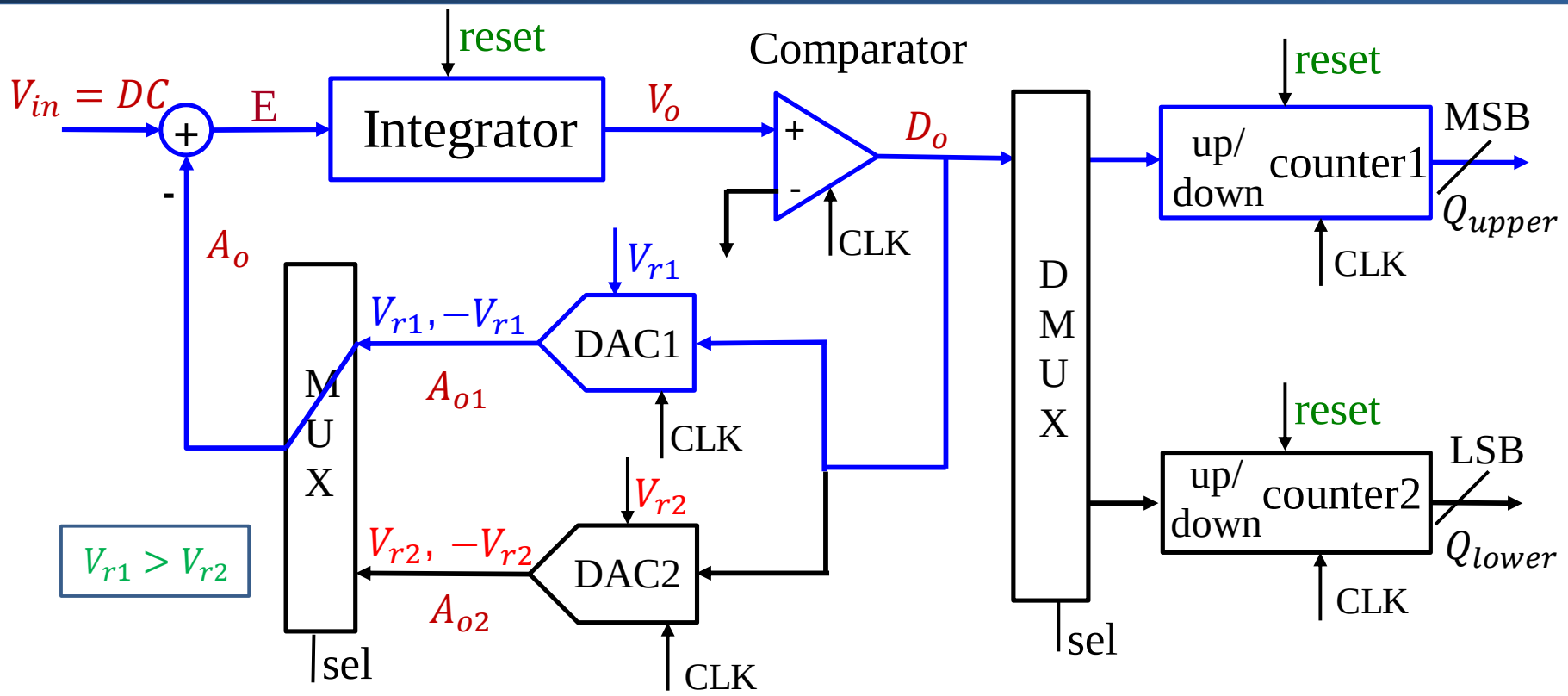
up/ down

counter2

Q_{lower}

CLK

Operation of Step 1



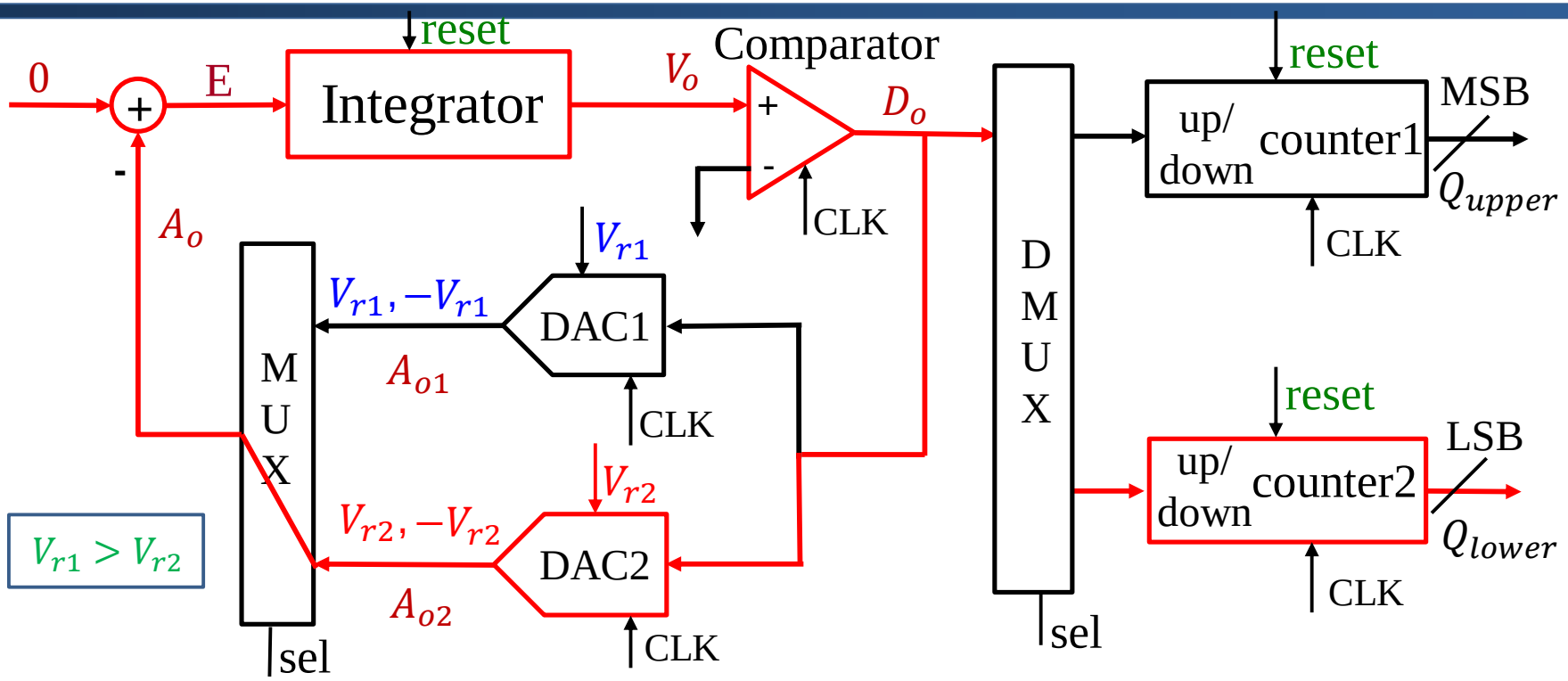
After N clocks, integrator output V_o:

$$V_o(N+1) = N \cdot V_{in} - (N_p - N_m)V_{r1}$$

N_p: Number of comparator outputs $D_o = 1$

N_m: Number of comparator outputs $D_o = 0$

Operation of Step 2



After N+M clocks, integrator output V_o

$$V_o(N+M+1) = N \cdot V_{in} - (N_p - N_m)V_{r1} - (M_p - M_m)V_{r2} \fallingdotseq 0$$

$$V_{in} = V_{r1}\left\{\left[2 \cdot \frac{N_p}{N} - 1\right] + K \cdot \left[2 \cdot \frac{M_p}{M-1} - 1\right]\frac{M-1}{N}\right\}, K = V_{r2}/V_{r1}$$

This should be known

M_p: Number of comparator outputs $D_o = 1$

M_m: Number of comparator outputs $D_o = 0$

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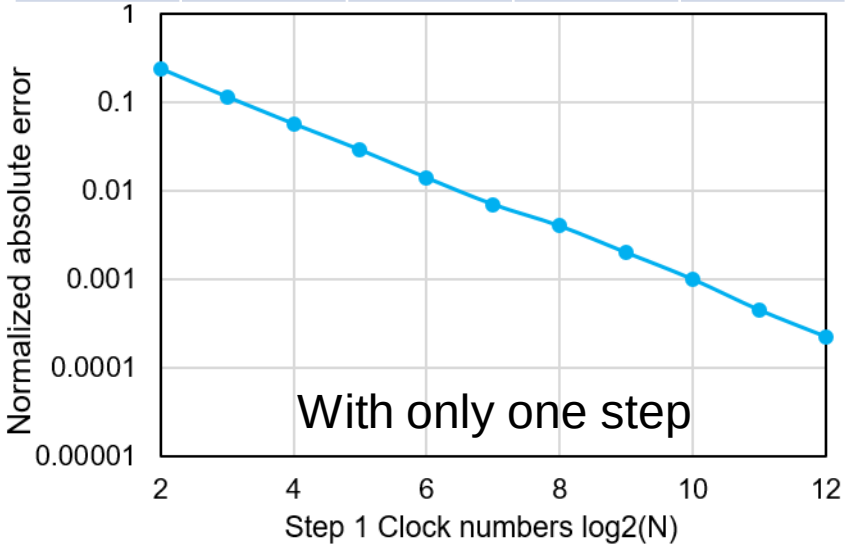
Clock Periods N in Step 1

1st-step parameters

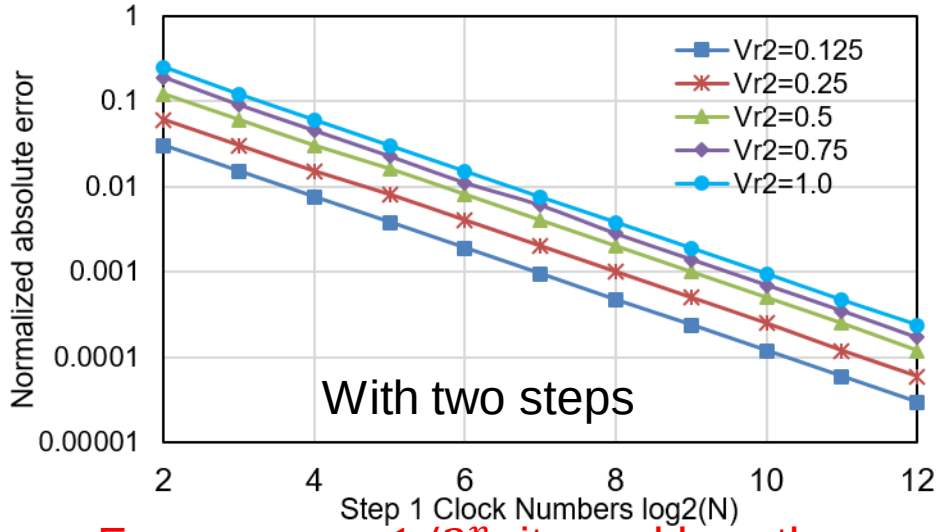
V_{in}	V_{r1}	V_{r2}	N	M
0.1~1	1.0	N/A	$2\sim2^{12}$	8



For accuracy $1/2^n$, 2^n clocks needed

2nd-step parameters

V_{in}	V_{r1}	V_{r2}	N	M
0.1~1	1.0	0.125, 0.25, 0.5 0.75, 1.0	$2\sim2^{12}$	8



For accuracy $1/2^n$, it need less than 2^n clocks with reference voltage V_{r2}

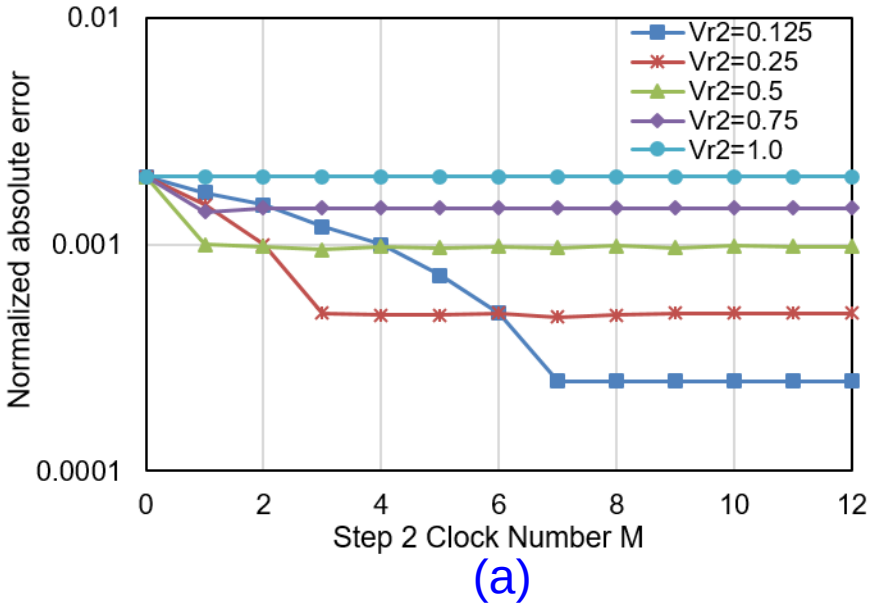
Normalized absolute error $= max_{V_{in}} |V_{in}\text{simulation} - V_{in}\text{calculation}|$

- V_{in} simulation: *exact input* V_{in}
- V_{in} calculation: *input* V_{in} *evaluated by derived equation*

Clock Periods M in Step 2

Simulation parameters

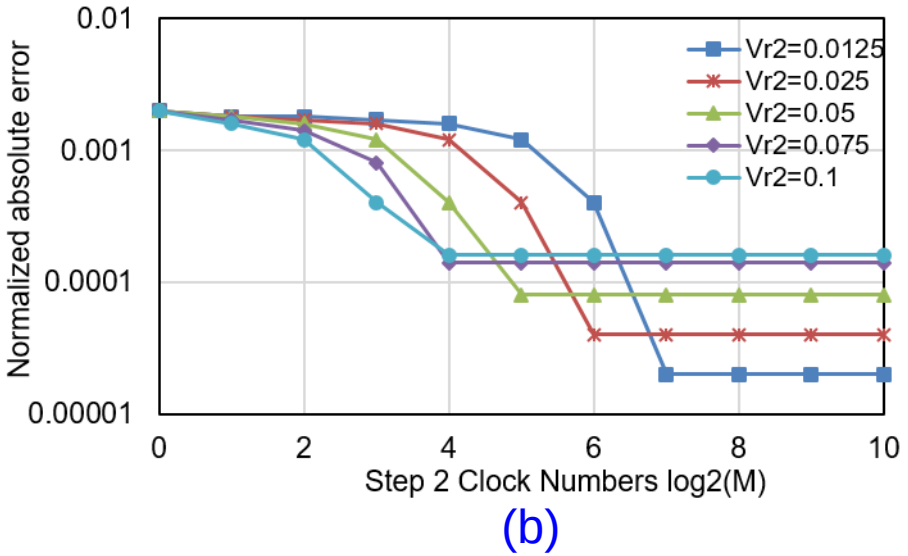
	V_{in}	V_{r1}	V_{r2}	N	M
(a)	0.1~1	1	0.125, 0.25, 0.5 0.75, 1.0	512	0~12
(b)	0.1~1	1	0.0125, 0.025, 0.05 0.075, 0.1	512	$0\sim2^{10}$



(a)

Small V_{r2}

- Significant error reduction
- Large number of M clocks



(b)

Ex, for $1/2^{16}$ accuracy,

$N = 1024, M = 128,$

$V_{r1} = 1, V_{r2} = 0.0125$

Shorten conversion time

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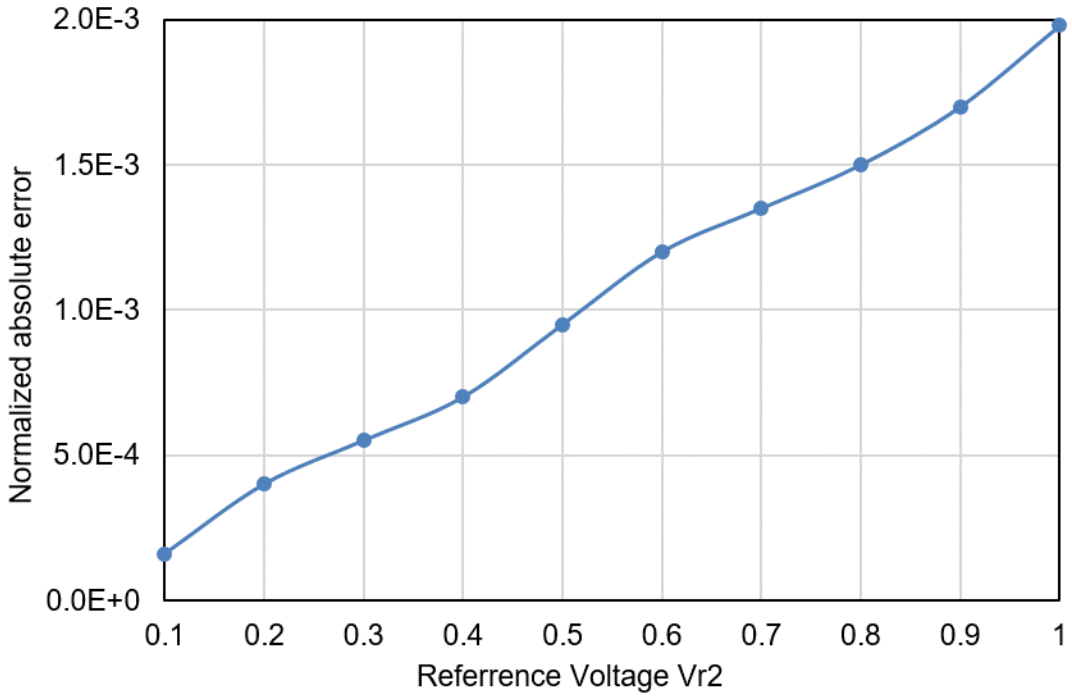
Effect of Reference Voltage V_{r2}

Simulation parameters

V_{in}	V_{r1}	V_{r2}	N	M
0.1~1	1.0	0.1~1.0	512	16



- ADC error is proportional to reference voltage Vr2
- Small value of V_{r2} reduces ADC error

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Basic Idea

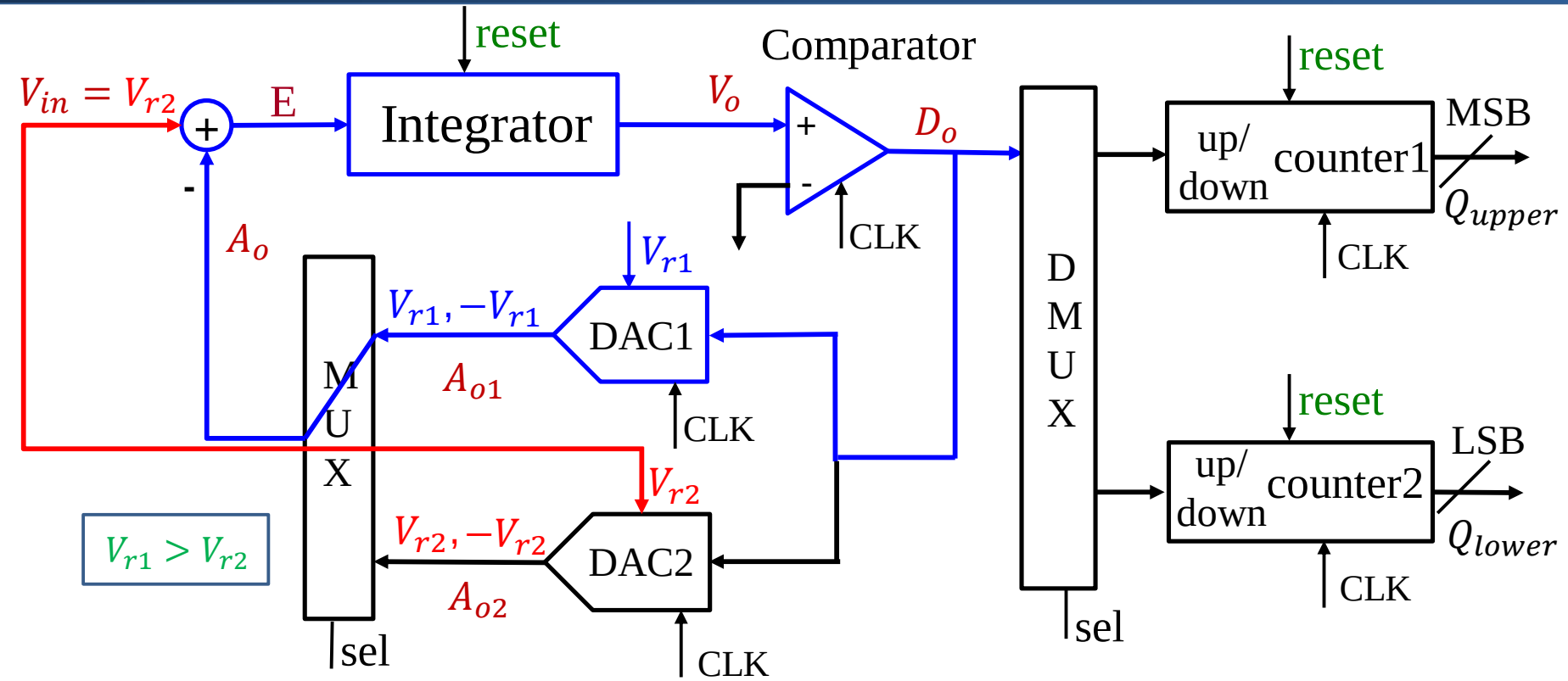
2nd reference voltage V_{r2} :

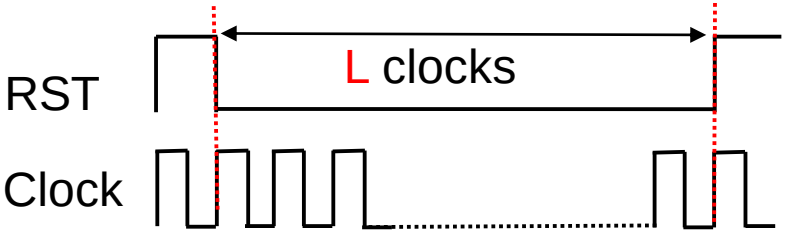
Measurement with the incremental ADC itself with 1st reference voltage V_{r1}

Two reference voltages ratio can be measured

- Accurately
- With only small extra circuits (only additional switches)

Self-Calibration Operation





After L clock cycles, integrator output V_o:

$$V_o(L+1) = L \cdot V_{r2} - (L_p - L_m)V_{r1} \fallingdotseq 0$$

$$K = V_{r2}/V_{r1} \fallingdotseq (L_p - L_m)/L$$

L_p: Number of comparator outputs $D_o = 1$

L_m: Number of comparator outputs $D_o = 0$

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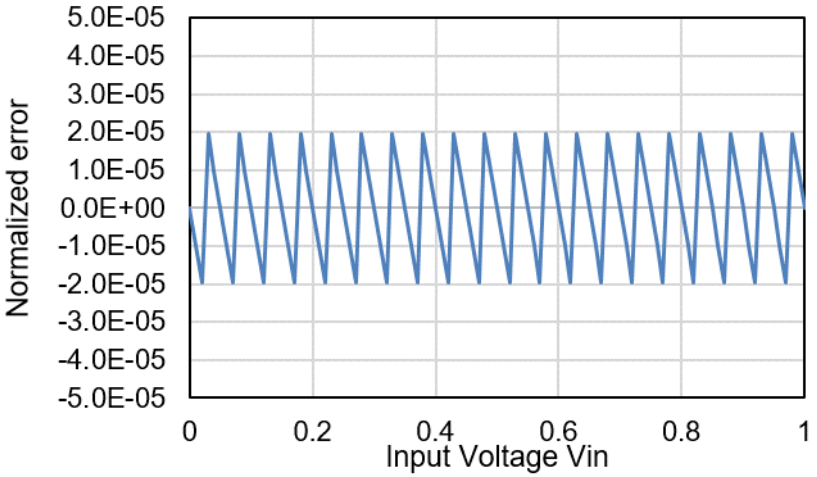
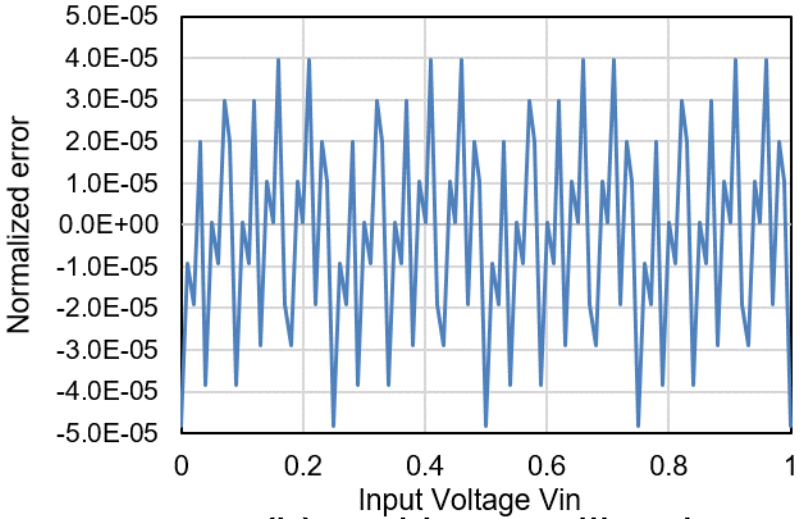
Simulation Results 1

Simulation parameters

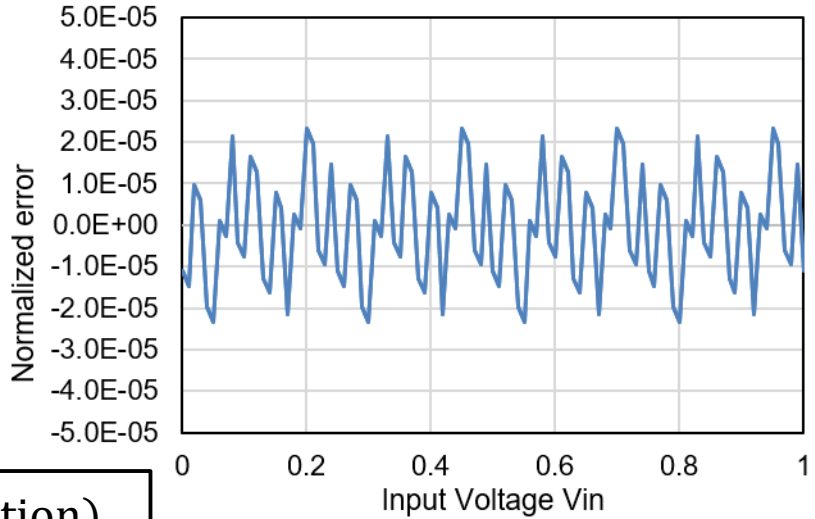
	V_{in}	V_{r1}	V_{r2}	K	N	M
(a)	0.1~1	1	0.0125	0.0125	512	128
(b)		1	0.01275	0.0125		
(c)		1	0.0125	0.01248		



(a) Ideal



(b) Without calibration



(c) With calibration

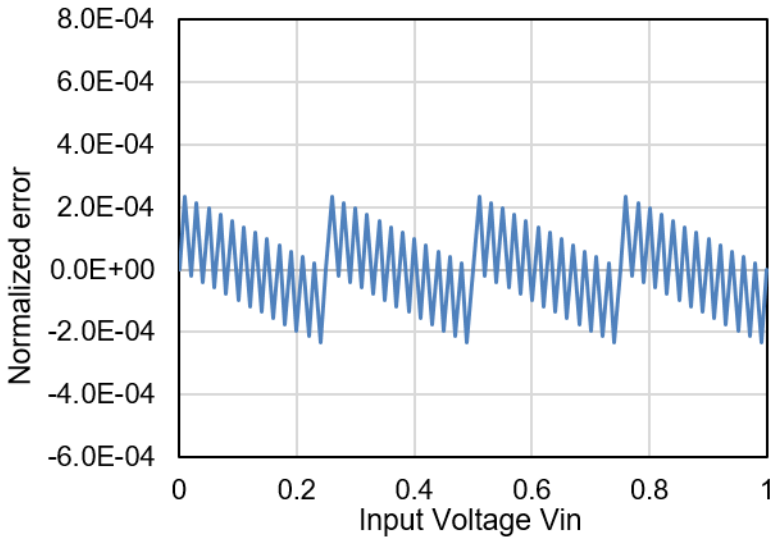
$$\text{Normalized error} = (V_{in}\ \text{simulation} - V_{in}\ \text{calculation})$$

Normalized error in (c) is smaller than (b).

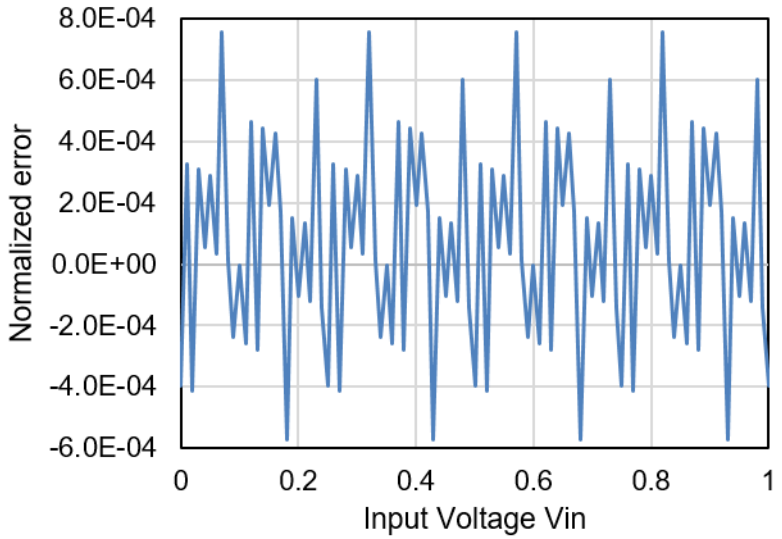
Simulation Results 2

Simulation parameters

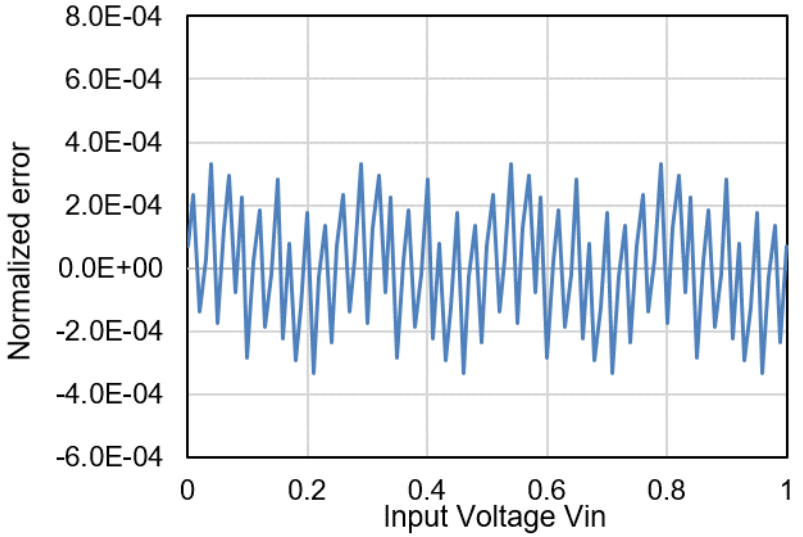
	V_{in}	V_{r1}	V_{r2}	K	N	M
(a)	0.1~1	1	0.125	0.125	512	16
(b)		1	0.1725	0.125		
(c)		1	0.1725	0.17248		



(a) Ideal



(b) Without calibration



(c) With calibration

Normalized error in (c) is smaller than (b)

→ Self-calibration is effective

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Conclusion

- ✓ 2-step incremental ADC:
  - High accuracy and short conversion time
  - Small V_{r2} significantly reduces quantization error.
  - Mismatch of 2 reference voltages causes ADC nonlinearity.

- ✓ Proposed self-calibration method:
  - Small additional circuit
  - Long conversion time, but just once.
  - Reference voltages mismatch compensation

- ➢ Future work:

  Extension to 3-step and 4-step incremental ADCs

Q&A

Reference and standard are important !

Metric System at French Revolution

Thank you very much

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