2021 年 10 月 30 日

International Conference on Analog VLSI Circuits　参加記

人を知るものは知なり、自らを知るものは明なり

群馬大学　小林春夫

International Conference on Analog VLSI Circuits (AVIC) 2021 のキーノート 3 件のアナウンスを目にした際に、良い国際学会になるのではないかと思い、研究室から 6 件論文を投稿した。査読コメントをもらい、担当大学院生と原稿を修正し発表スライド作成・リハーサルを行う。6 件とも発表を無事行え、大きな教育効果があったと感じた。彼ら彼女らの就職活動にもプラスに働くと思う。

気が付くと、発表学生 6 人は　日本人 1 名、ラオス 1 名、中国 4 名と留学生がほとんどである。

他の機関からの発表を聴講し、世の中ではどのような研究が行われているのか、自分の立ち位置はどうなのかということを知ることができた。また共著者の参加もあった。これらはオンラインで行われたゆえに可能になった。

参加することで研究室は大きな恩恵を受け　学会主催者に感謝する次第である。

Monday October 18th	Tuesday October 19th	Wednesday October 20th	Thursday October 21st
Hybrid Mode, starting 8:30 France - 15:30 Japan			
8:15 - 8:30 Opening Ceremony			
8:30 - 9:30 Keynote Dr. Ryuichi Fujimoto Technical Challenges toward High-Bandwidth and Large-Capacity Storages with Low-Power Consumption	8:30 - 9:30 Keynote Dr. Keith O'Donoghue Precision Analog Design Challenges on "Big Digital" SoC	9:00 - 10:00 Keynote Victor Grimblatt Thinking Outside the CMOS Box	9:00 - 12:00 Student Event

Session A2: Analog-to-Digital Converter (ADC)

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A2.2 Second-order delta-sigma down-converting ADC with even harmonic mixer and noise-shaping dynamic element matching 50
Yuki Genkaku, Akira Yasuda, Michitaka Yoshino, Syuji Okage (Hosei University)*

A2.3 Dynamic element matching for successive approximation register and delta-sigma modulator two-step analog-to-digital converter with digital-to-analog converter and residual gain error 56
Rei Watanabe, Akira Yasuda, Michitaka Yoshino (Hosei University)*

A2.4 Designing opamp amplifiers for a 5th order CT CRFF ΔΣ ADC using model-based design paradigm and gm/ID methodology 61
Abderrahmane Ghimouz (Université Grenoble Alpes, Grenoble INP, CNRS, LPSC-IN2P3)*

A2.5 An 8-bit hybrid analog-to-digital converter combining flash with radix-3 and two-bit/cycle successive approximation resister analog-to-digital converter 65
Ryukichi Hirai, Ryo Kishida, Tatsuji Matsuura, Akira Hyogo (Tokyo University of Science)*

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A2.7 Two-step incremental ADC architecture with self-calibration of two reference voltages ratio 77
Lengkhang Nengvang, Shogo Katayama, Jianglin Wei, Lei Sha, Tri Minh Tran (Gunma University); Kazufumi Naganuma, Kiyoshi Sasai, Junichi Saito (Alps Alpine Co., Ltd.); Anna Kuwana, Haruo Kobayashi (Gunma University)*

International Conference on Analog VLSI Circuits

The Research Committee on Electronic Circuits of the Institute of Electrical Engineers of Japan (IEEJ) in cooperation with IMS Laboratory, the electronics research center of Univ. Bordeaux will hold 2021 International Conference on Analog VLS Circuits (AVIC) in Bordeaux, France on October 18-20, 2021 as an edition in hybrid mode: on-site and virtual.

AVIC is the successor of International Analog VLSI Workshop, which had been held for 24 years. The purpose of this conference is to discuss state-of-the-art ideas and results from researches on analog VLSI circuits and their applications. It has contributed to long-standing worldwide community of analog VLSI circuit experts in industry and academia.

Tuesday October 19, 2021

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Abderrahmane Ghimouz (Université Grenoble Alpes, Grenoble INP, CNRS, LPSC-IN2P3)*

B1.2 3.4 to 4.1 GHz wideband LNA with gain flatness and low noise figure 87
Dai Yoshioka, Takayuki Morisita, Kiyotaka Komoku, Nobuyuki Itoh (Okayama Prefectural University)*

B1.3 1.65/2.5/4.0-GHz triple-band concurrent low-noise amplifier 92
Shinichiro Seguchi, Takayuki Morishita, Kiyotaka Komoku, Nobuyuki Itoh (Okayama Prefectural University)*

B1.4 920 MHz low-power LNAs operated in moderate inversion region 97
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B1.7 Design of digital-to-analog converter architectures based on polygonal numbers 112
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Session C1: "RO/PLL" and "Integrated Circuit Technology"

C1.1 Ultra low power injection-locked ring oscillator architecture using FDSOI technology 158
Yuqing Mao, Yoann Charlon Florian Debieu, Zhaopeng Wei, Yves Leduc, Gilles Jacquemod (Université Côte d'Azur)*

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Yen Thi Phuong Tran (Université de Bordeaux), Toshihiro Nomura, Mohamed Salim Cherchali, Claire Tassin (Etudes et Production Schlumberger); Yann Deval, Cristell Maneux (Université de Bordeaux)*

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C1.4 A 138 Vpp amplitude and drivability tunable ultrasound pulser for a 3072 ch matrix probe 171
Toru Yazaki, Yutaka Igarashi, Takuma Nishimoto, Shinya Kajiyama, Yusaku Katsube (Hitachi, Ltd.); Yoshihiro Hayashi, Takuya Kaneko (FUJIFILM Healthcare Co.)*

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C1.6 Analog-to-feature converter optimization through power-aware feature selection 181
Antoine Back, Paul Chollet, Olivier Fercoq, Patricia Desgreys (Télécom Paris)*

C1.7 Analyse and design of a capacitive-isolation-based information transmission system 187
Ming Zhang (Université Paris-Saclay); Nicolas Llaser (DORIAN)*

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International Conference on Analog VLSI Circuits (AVIC)
Bordeaux, France 21st Oct. 2021

Folding ADC for Multi-bit ΔΣ AD Modulator

Xiongyan Li, T. Feng, L. Nengvang, S. Katayama, J. Wei
H. Lin, A. Kuwana, H. Kobayashi
K. Nagamuma, K. Sasai, J. Saito

Gunma University
Alps Alpine Co., Ltd.

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Gunma University

Q&A

Think of a difficult problem
in small pieces.

René Descartes
1596-1650

Thank you very much

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Oct.2021
International Conference on Analog VLSI Circuits

Code Selective Histogram Method: Two-Tone Signal for ADC Linearity Test Time Reduction

Yujie Zhao, A. Kuwana, S. Katayama, J. Wei,
H. Kobayashi, K. Hatayama, T. Nakatani,
K. Sato, T. Ishida,
T. Okamoto, T. Ichikawa
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ROHM Semiconductor

ROHM SEMICONDUCTOR

群馬大学 GUNMA UNIVERSITY

Start with the simplest and
reach the complex.

René Descartes

Thanks for your attention.

International Conference on Analog VLSI Circuits
Bordeaux, France, 18th Oct. 2021 2021/9/27

Two-Step Incremental ADC Architecture With Self-Calibration of Two Reference Voltages Ratio

Lengkhang Nengvang,
S. Katayama, J. Wei, L. Sha , T. M. Tran, A. Kuwana,
K. Naganuma , K. Sasai, J. Saito, H. Kobayashi

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Q&A 25/25

Reference and standard
are important !

Metric System at French Revolution

Thank you very much

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International Conference on Analog VLSI Circuits (AVIC)
Bordeaux, France 19th Oct. 2021

Segmented DAC Unit Cell Selection Algorithm and Layout/Routing Based on Euler's Knight Tour

Dan Yao, X. Bai, A. Kuwana, K. Kawauchi,
M. Higashino, H. Kobayashi
A. Suzuki, S. Yamada, T. Kato, N. Ono,
K. Miura, K. Hirai, R. Kitakoga

Gunma University
Jedat Inc.

Kobayashi Laboratory

Magic Squares by
French Mathematician
Bernard Frénicle de Bessy

ご清聴ありがとうございました

Thank you for listening

謝謝

Merci de votre attention

International Conference on Analog VLSI Circuits (AVIC)
Bordeaux, France 19th Oct. 2021

A Proposal of Digital-to-Analog Converter Architectures Based on Polygonal Numbers

Xueyan Bai, D. Yao, Y. Du, T. Tran,
A. Kuwana, H. Kobayashi,
K. Kubo
Gunma University
Oyama National College of Technology

Kobayashi Laboratory

Kobayashi Laboratory 47/47

Fermat polygonal number theorem
was finally proven in 1813,
by Augustin-Louis Cauchy.

1789 –1857

ご清聴ありがとうございました

Thank you for listening

謝謝

Merci de votre attention

International Conference on Analog VLSI Circuits (AVIC)
Bordeaux, France Oct. 2021

Design Considerations for MOS Peaking Current Sources Insensitive to Supply Voltage and Temperature

Takafumi Kamio, T. Hosono , S. Yamamoto , J. Matsuda
S. Katayama, A. Kuwana, A. Suzuki , S. Yamada
T. Kato, N. Ono, K. Miura, H. Kobayashi
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Q&A 29/29

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Japan
Gunma