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Revisit to Hopfield Network for Asynchronous SAR ADC and DAC

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Gunma University

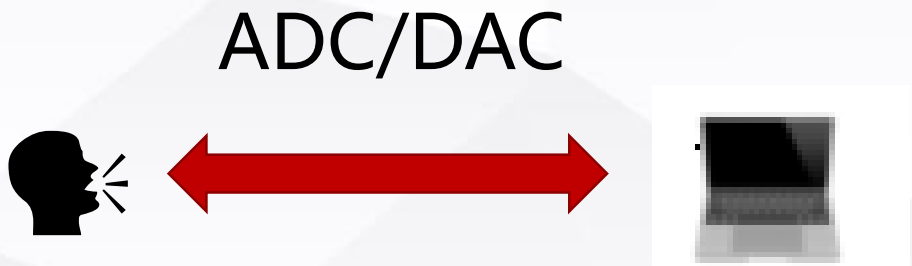
Contents

Contents

Value of ADC DAC Research

- Analog signals are everywhere

- Digital signals are useful for computer processing



Analog-digital interface circuits are important.

Revisit to Hopfield neural net ADC

- Traditional Hopfield neural network ADC.

- Elements of “interest” are used as ADC design with realistic competitiveness.
- Local minima problem
  - Sometimes wrong output

- Revisit because of
  - Very fast SAR ADC
  - Non-binary SAR ADC as well as binary
  - Simple design

Prof. John Joseph Hopfield
California Institute of Tech.
Princeton University

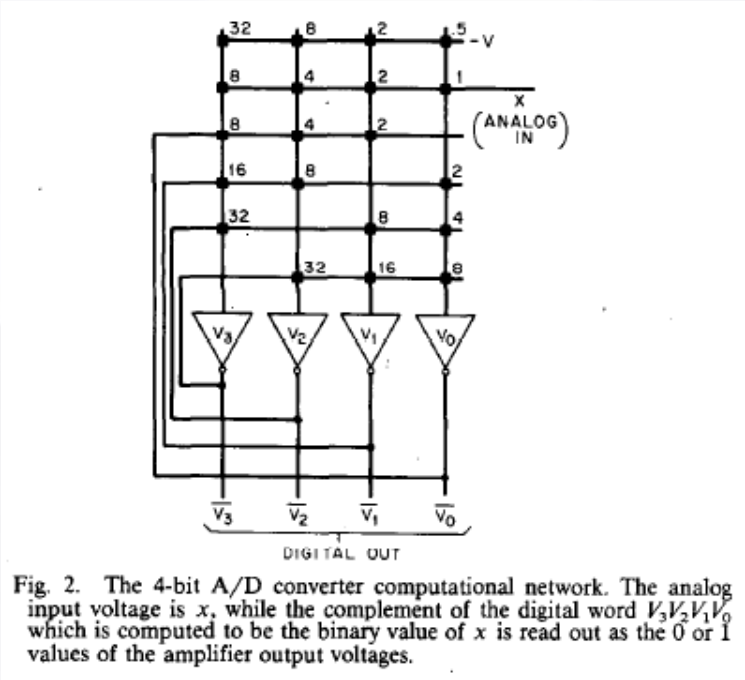


Fig. 2. The 4-bit A/D converter computational network. The analog input voltage is x, while the complement of the digital word $V_3V_2V_1V_0$ which is computed to be the binary value of x is read out as the 0 or 1 values of the amplifier output voltages.

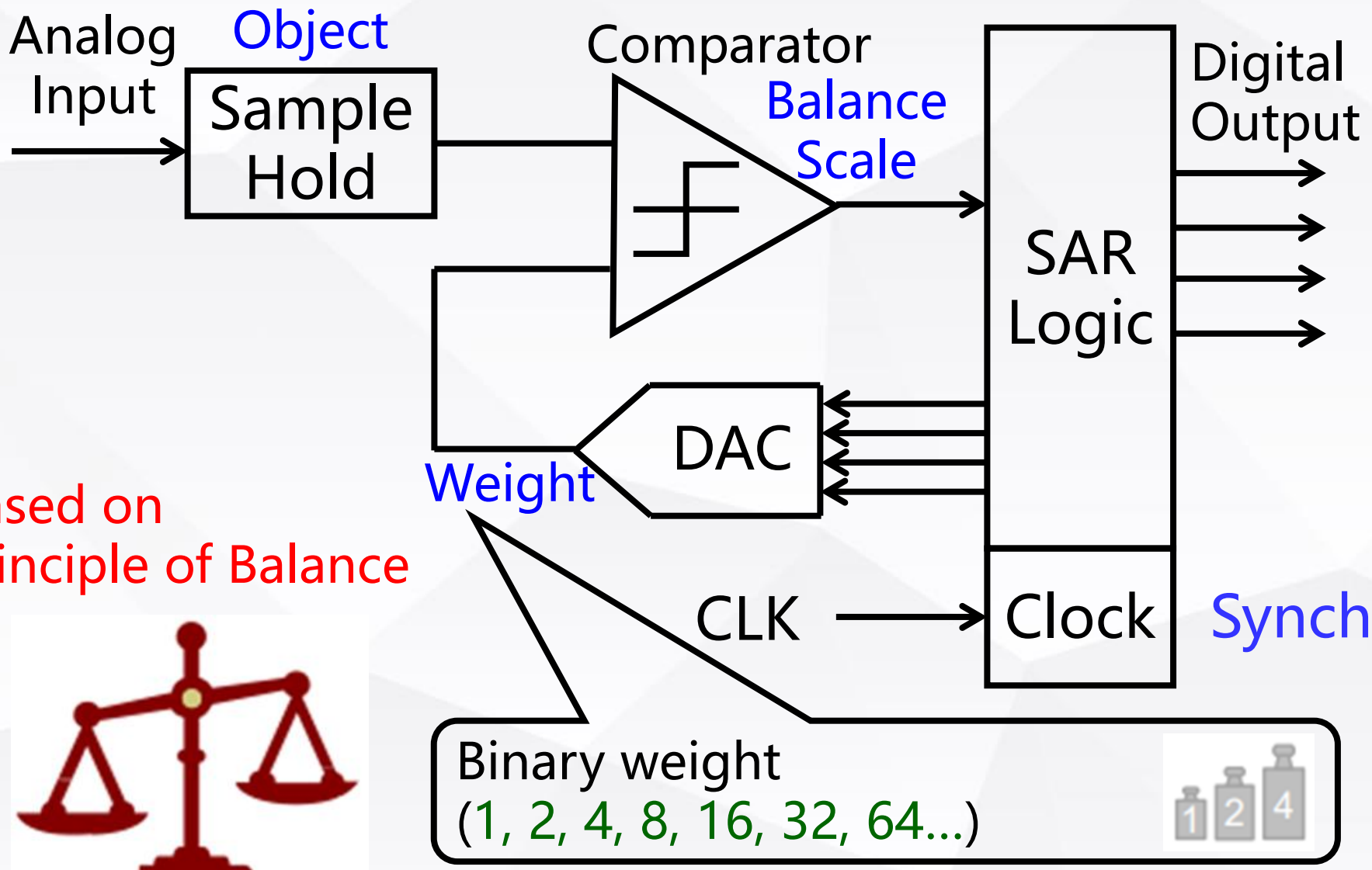
Improvement of Hopfield neural network ADC

- Discard feedback from lower bits
- All feed-forward configuration

- No local minima
  - Always correct output
- Realization of asynchronous SAR ADC
  - Very fast
  - No high frequency clock required
  - Small hardware
- Proposal of Non-binary asynchronous SAR ADC

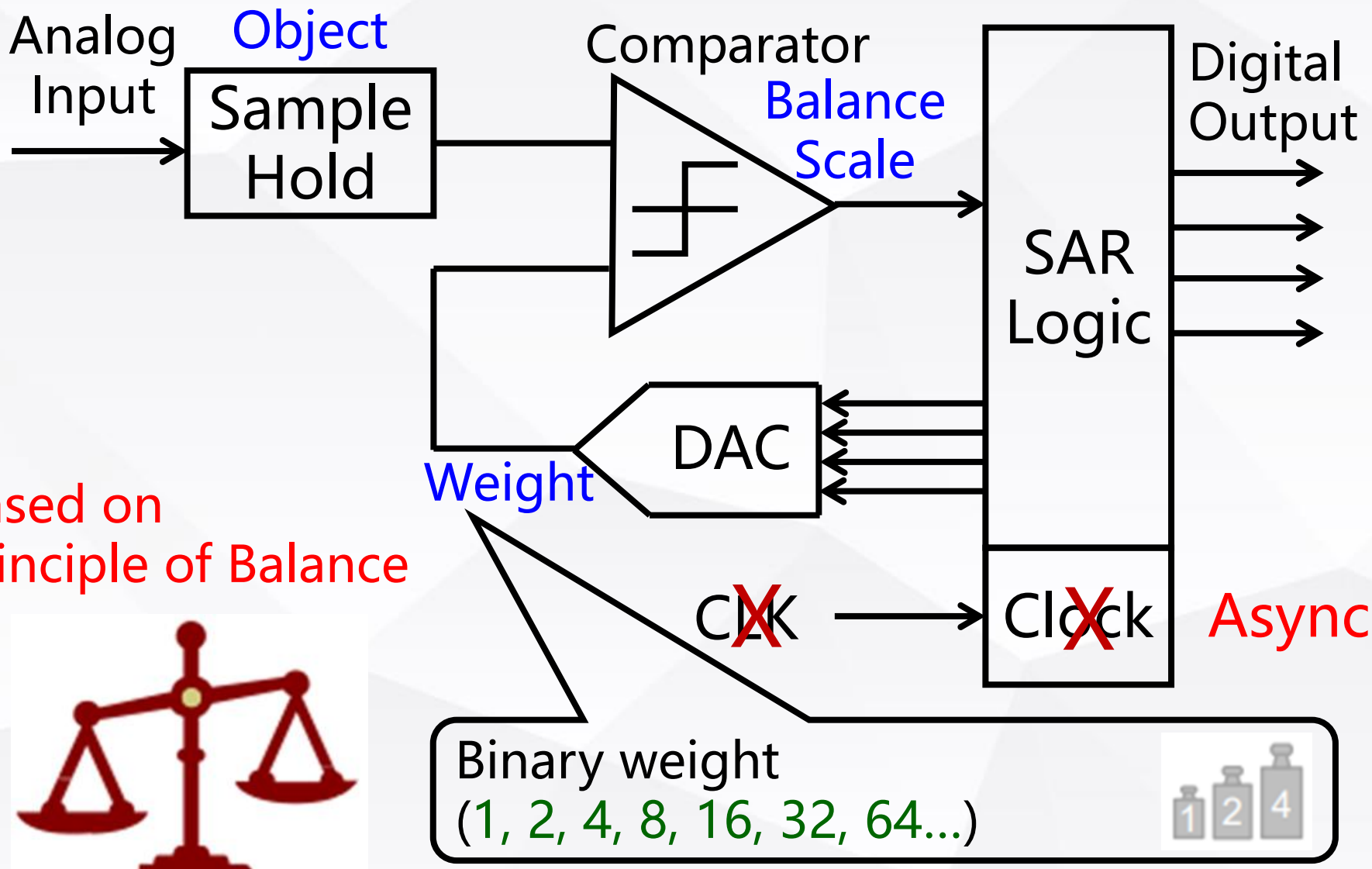
Contents

Binary Weighted SAR ADC



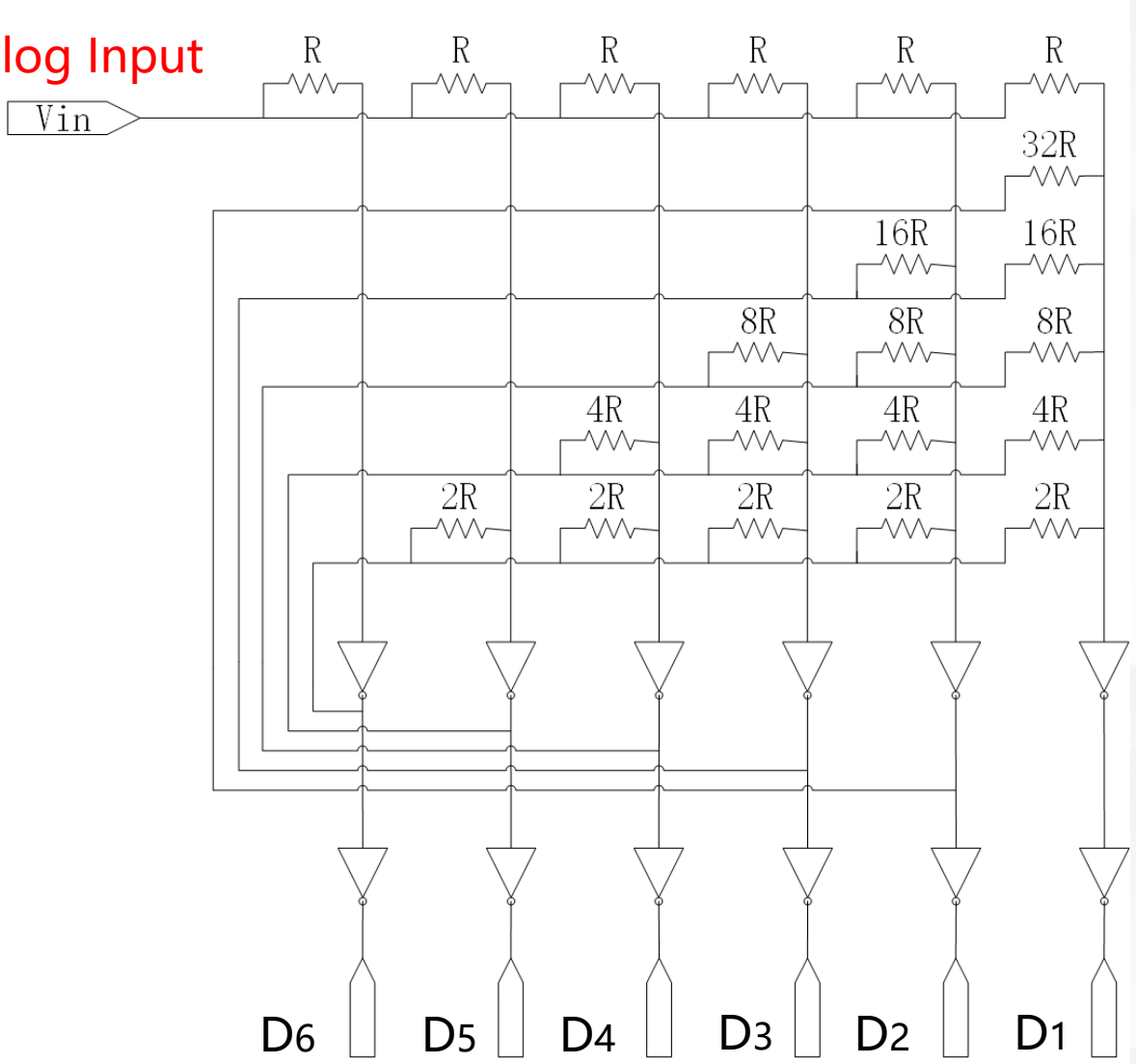
Based on
Principle of Balance

Asynchronous Binary Weighted SAR ADC



Investigated Network

6-bit SAR ADC case



Improvement of Hopfield neural network ADC

- Discard feedback from lower bits
- All feed-forward configuration
- No local minima

Asynchronous SAR ADC

- Very fast
- No high frequency clock
- Small hardware

10-bit binary weighted SAR ADC

Step	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	output
Weight	516	256	128	64	32	16	8	4	2	1	

Decimal digital output :

$$Data = (1/R)\,D_{10} + (1/R_9)\,D_9 + (1/R_8)D_8 + (1/R_7)D_7 + (1/R_6)D_6$$

$$+ (1/R_5)D_5 + (1/R_4)D_4 + (1/R_3)D_3 + (1/R_2)D_2 + (1/R_1)D_1$$

Here

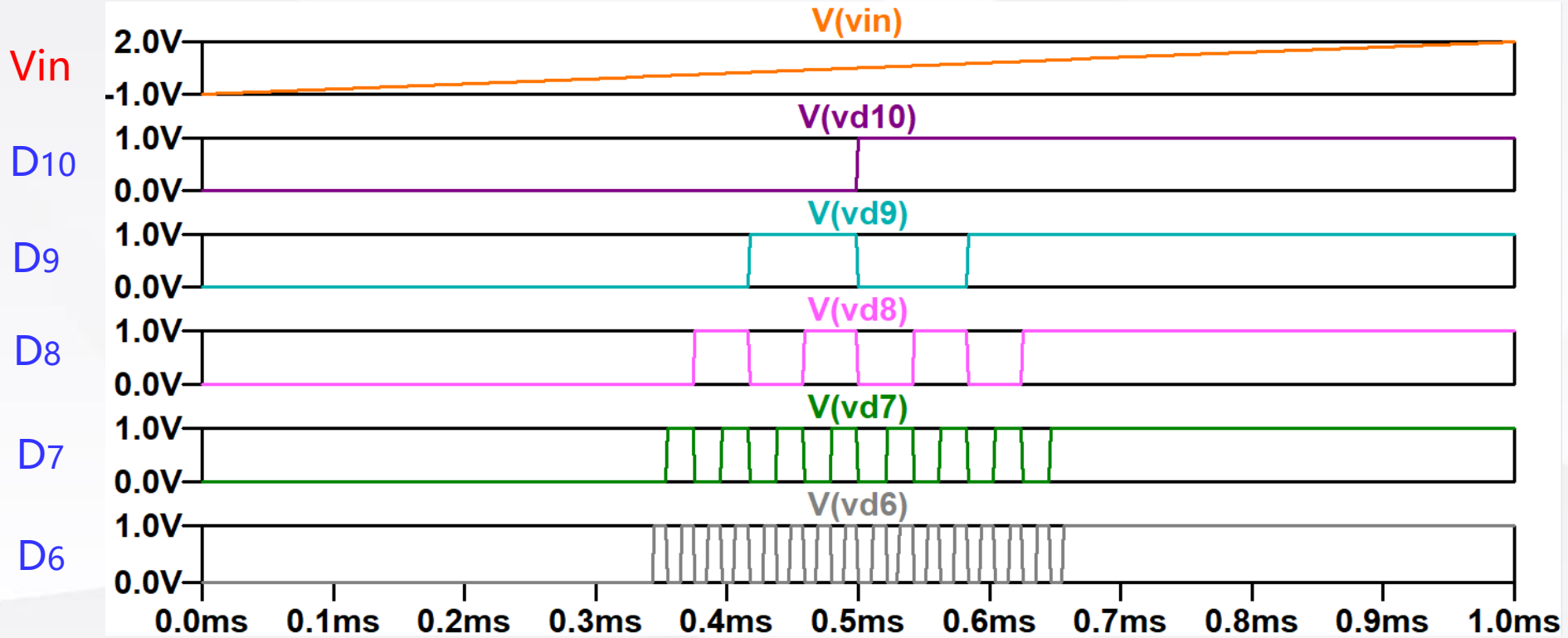
$1/R = 512,\ 1/R_9 = 256,\ 1/R_8 = 128,\ 1/R_7 = 64,\ 1/R_6 = 32$

$1/R_5 = 16,\ 1/R_4 = 8,\ 1/R_3 = 4,\ 1/R_2 = 2,\ 1/R_1 = 1$

Binary weighted

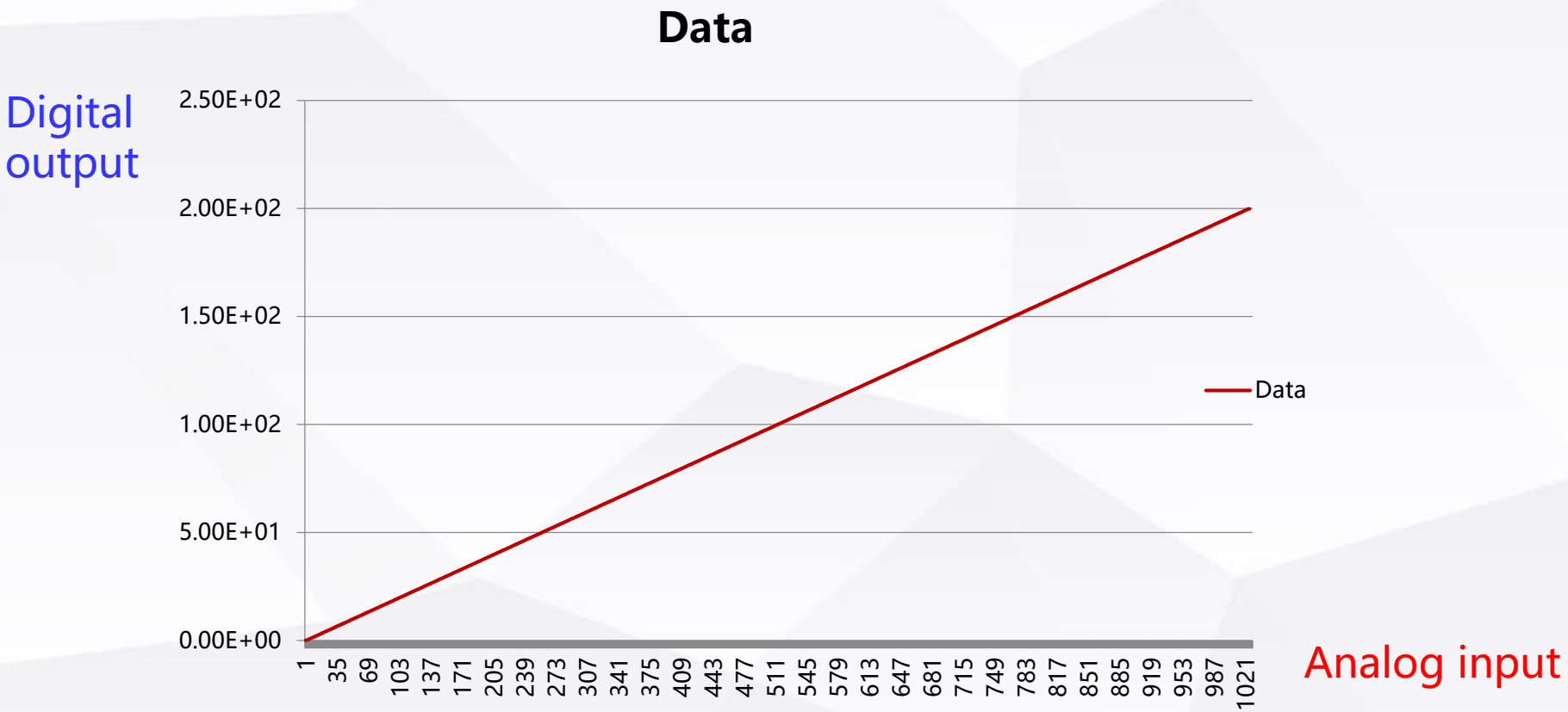
10-bit asynchronous binary-weighted SAR ADC with improved Hopfield network

Ramp input



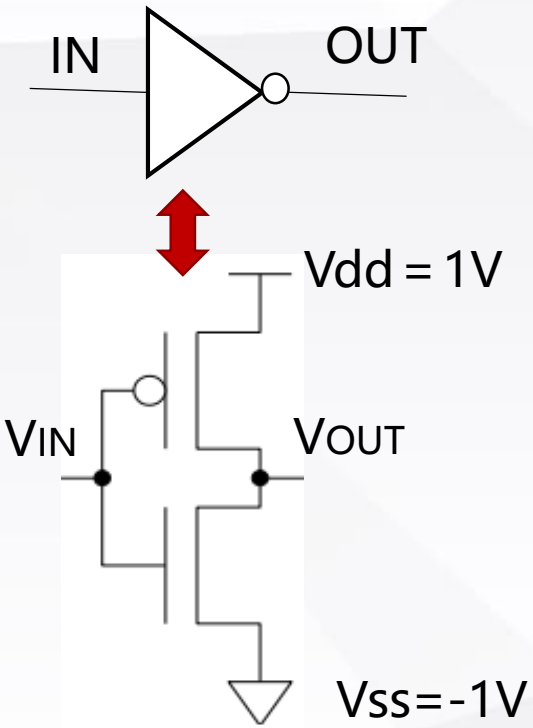
Decimal Data Calculation

$$Data = (1/R)\,D_{10} + (1/R_9)\,D_9 + (1/R_8)D_8 + (1/R_7)D_7 + (1/R_6)D_6 + (1/R_5)D_5 + (1/R_4)D_4 + (1/R_3)D_3 + (1/R_2)D_2 + (1/R_1)D_1$$

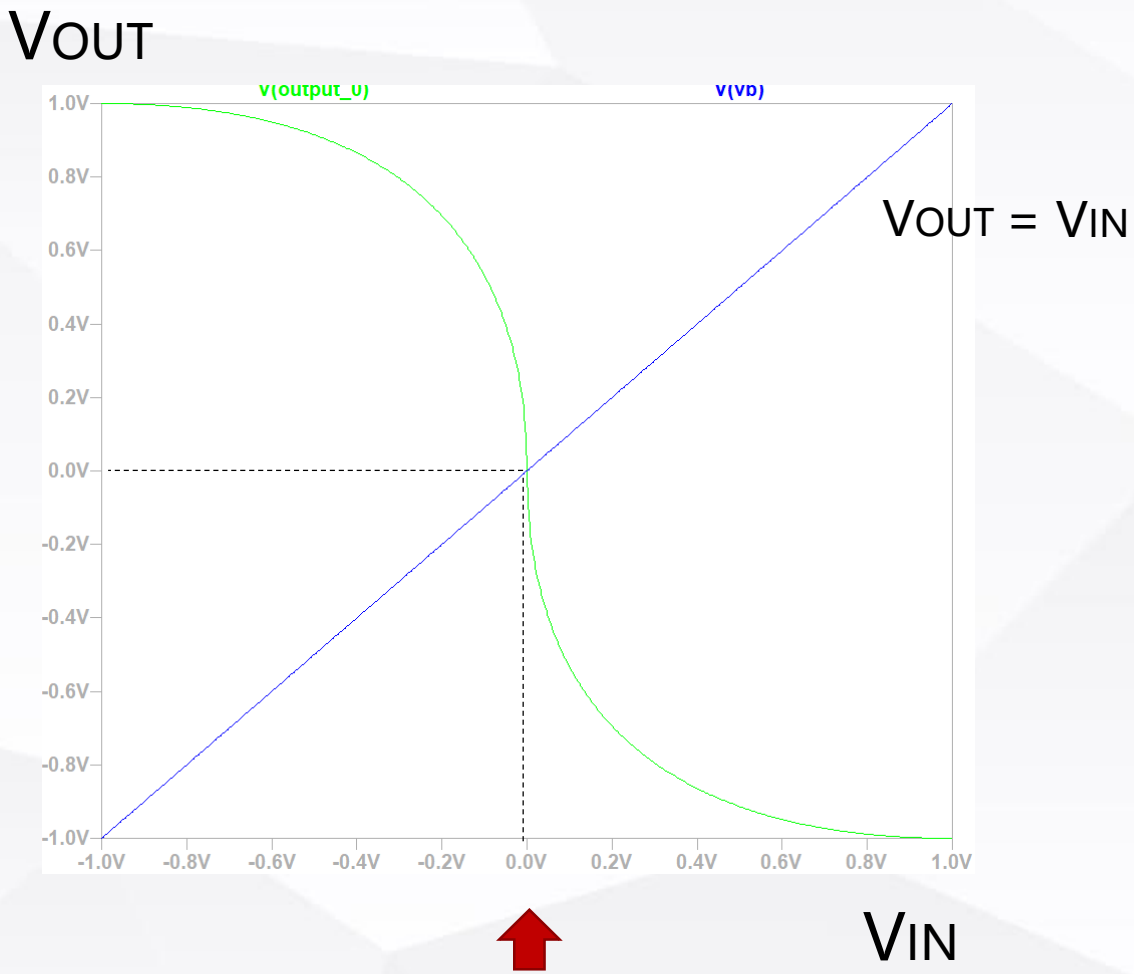


- Operation has been confirmed.
- Amazingly simple design can realize a 10-bit SAR ADC

CMOS inverter



SPICE simulation



CMOS inverter threshold voltage

⇒ Affected by PVT variation

⇒ ADC nonlinearity

Asynchronous SAR ADC with Hopfield network

Advantage: High speed, small chip area

Disadvantage: ADC nonlinearity

due to resistors mismatch, inverter threshold voltage variation

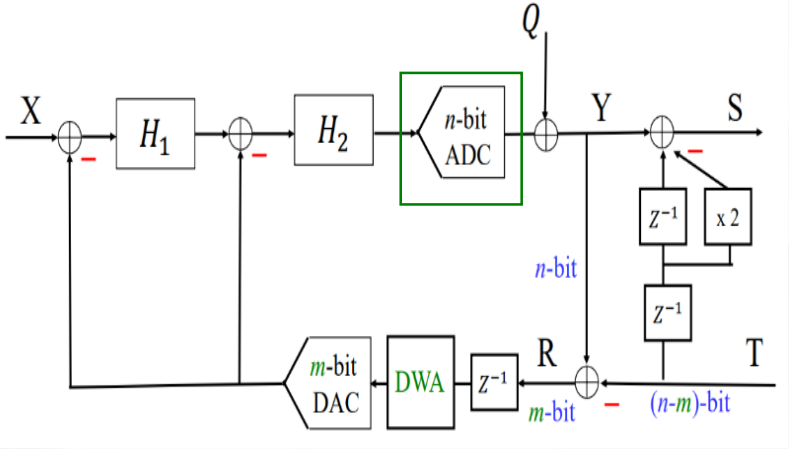
Proposed killer application

Usage inside multi-bit ΔΣ ADC

Currently, 3-bit flash ADC is used.

More than 6-bit Hopfield asynchronous SAR ADC can be used.

Its nonlinearity is noise-shaped inside the modulator.



Extended Leslie-Singh Architecture

Contents

Definition (n=0,1,2,3…)

$$F_0 = 0$$
$$F_1 = 1$$
$$F_{n+2} = F_n + F_{n+1}$$

Example of numbers(Fibonacci number)

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89…

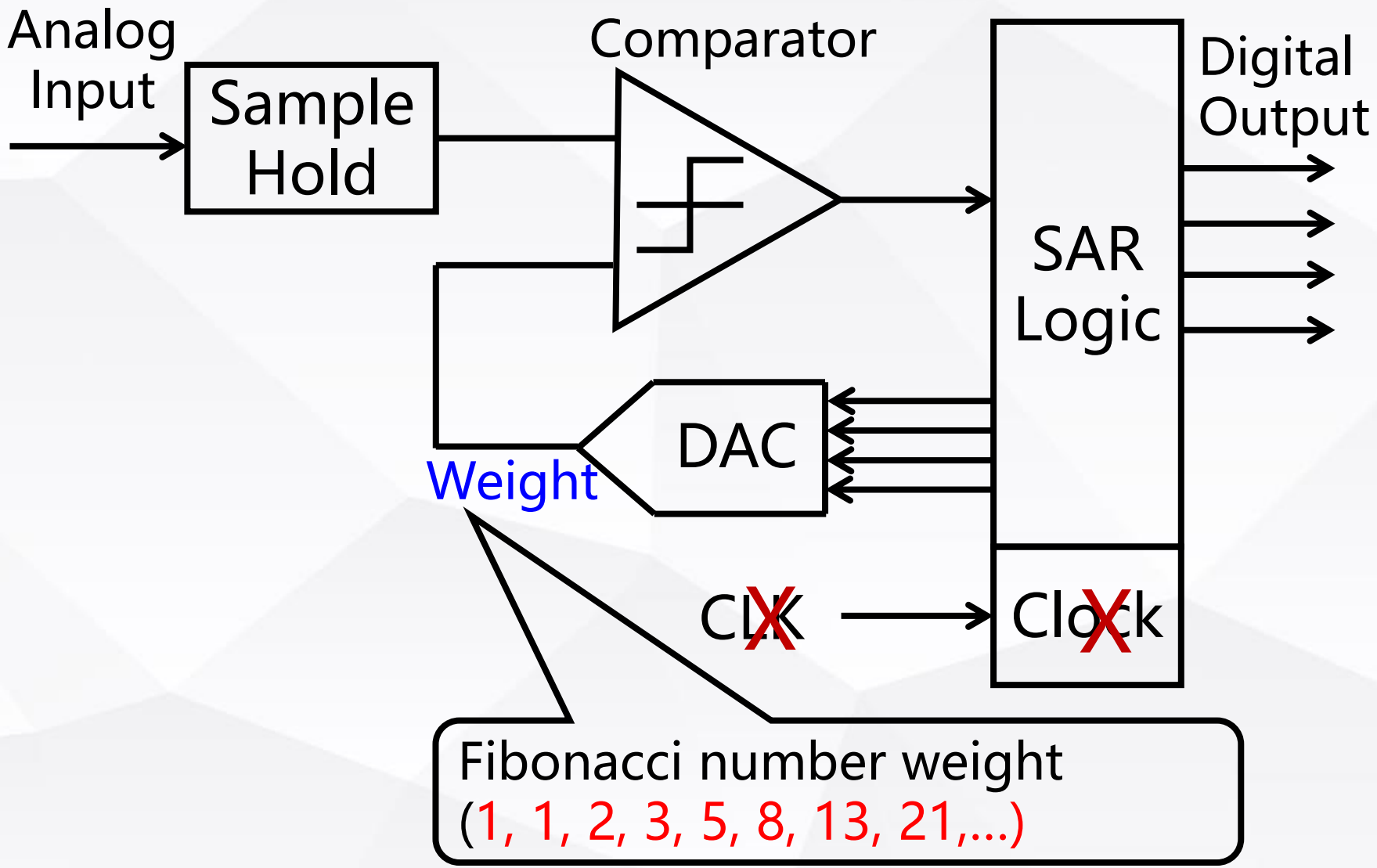
Leonardo Fibonacci
(around 1170-1250)

Property

The closest terms ratio converges to *"Golden Ratio"* !

$$\lim_{n\to\infty} \frac{F_n}{F_{n-1}} = 1.618033988749895 = \varphi$$

Fibonacci number weighted SAR ADC



Radix ≒ 1.62

Redundancy

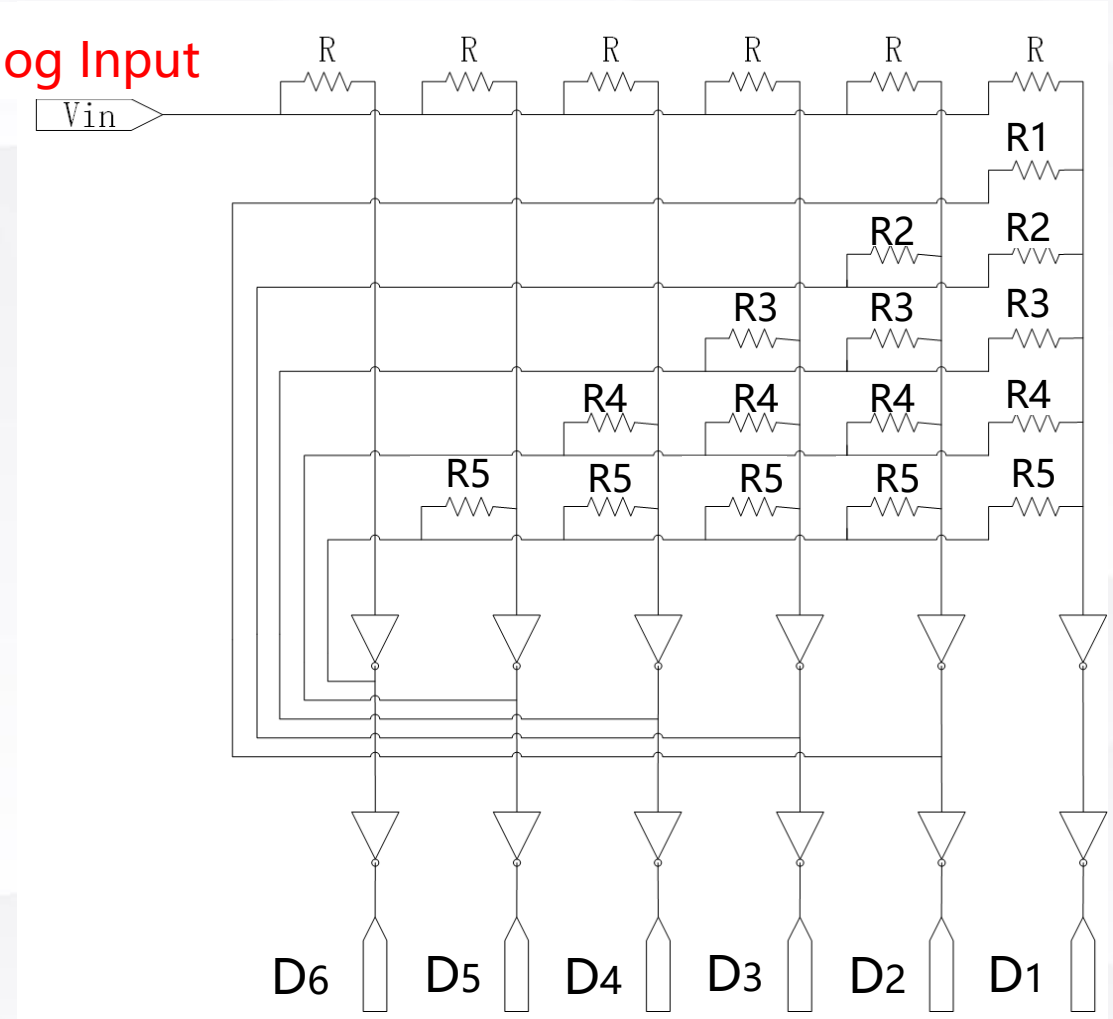
⬇

Reliability

[1] Y. Kobayashi, H. Kobayashi, et. al., "SAR ADC Design Using Golden Ratio Weight Algorithm," ICSCIT (Oct. 2015)

Fibonacci number weighted SAR ADC

Radix ≒ 1.62



$R : R_5 = 8 : 16$

$R : R_4 = 5 : 16$

$R : R_3 = 3 : 16$

$R : R_2 = 2 : 16$

$R : R_1 = 1 : 16$

Fibonacci number

10-bit Fibonacci weighted SAR ADC

Step	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	output
Weight	89	55	34	21	13	8	5	3	2	1	

Decimal digital output :

$$Data = (1/R)\,D_{10} + (1/R_9)\,D_9 + (1/R_8)D_8 + (1/R_7)D_7 + (1/R_6)D_6$$

$$+ (1/R_5)D_5 + (1/R_4)D_4 + (1/R_3)D_3 + (1/R_2)D_2 + (1/R_1)D_1$$

Here

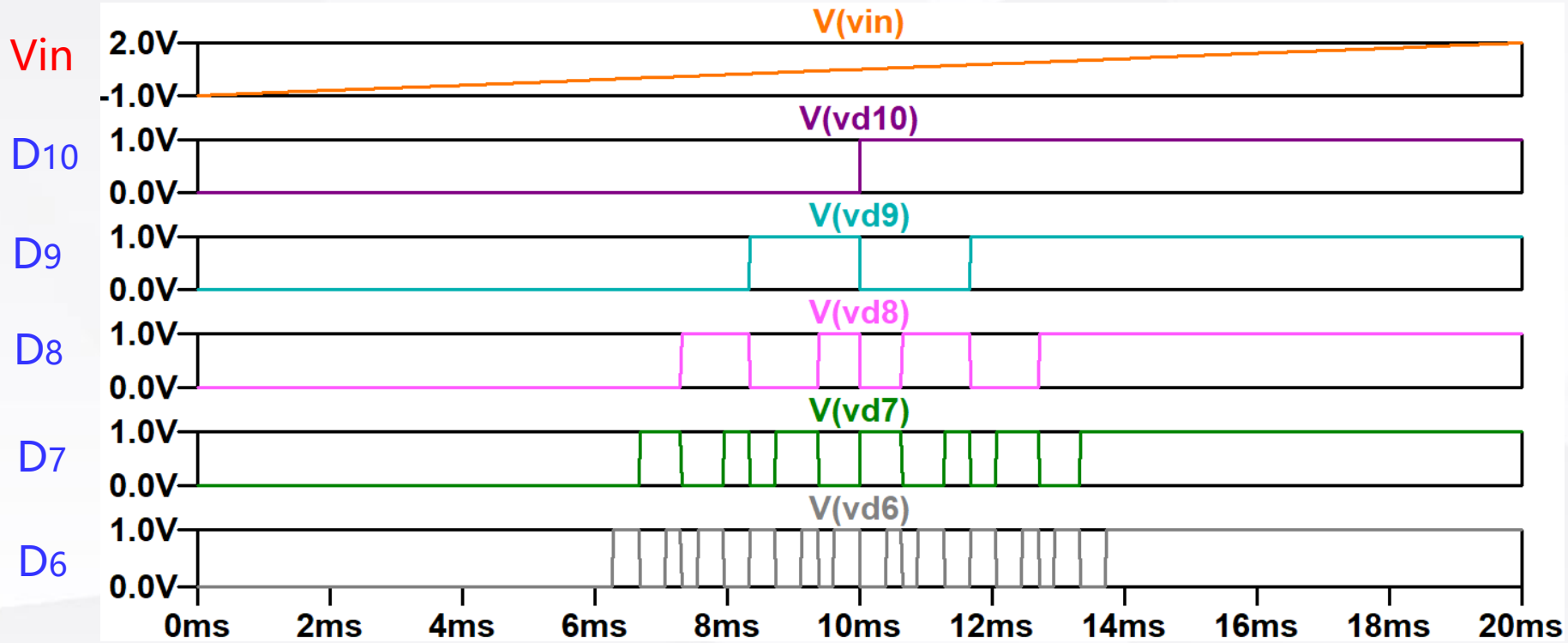
$1/R = 89$, $1/R_9 = 55$, $1/R_8 = 34$, $1/R_7 = 21$, $1/R_6 = 13$

$1/R_5 = 8$, $1/R_4 = 5$, $1/R_3 = 3$, $1/R_2 = 2$, $1/R_1 = 1$

Fibonacci number weighted

10-bit asynchronous Fibonacci number weighted SAR ADC with improved Hopfield network

Ramp input



Higher 5 bits

10-bit asynchronous Fibonacci number weighted SAR ADC with improved Hopfield network

Ramp input

Vin

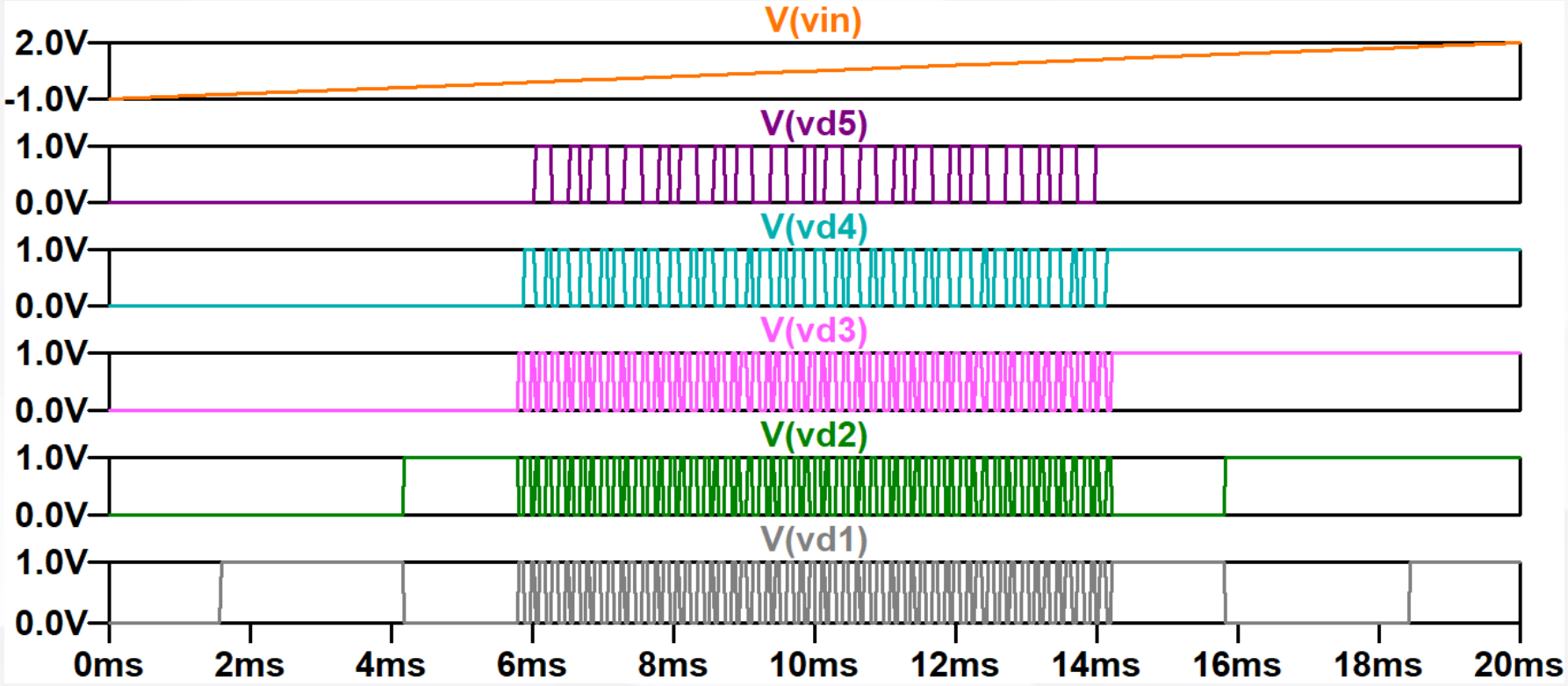
D5

D4

D3

D2

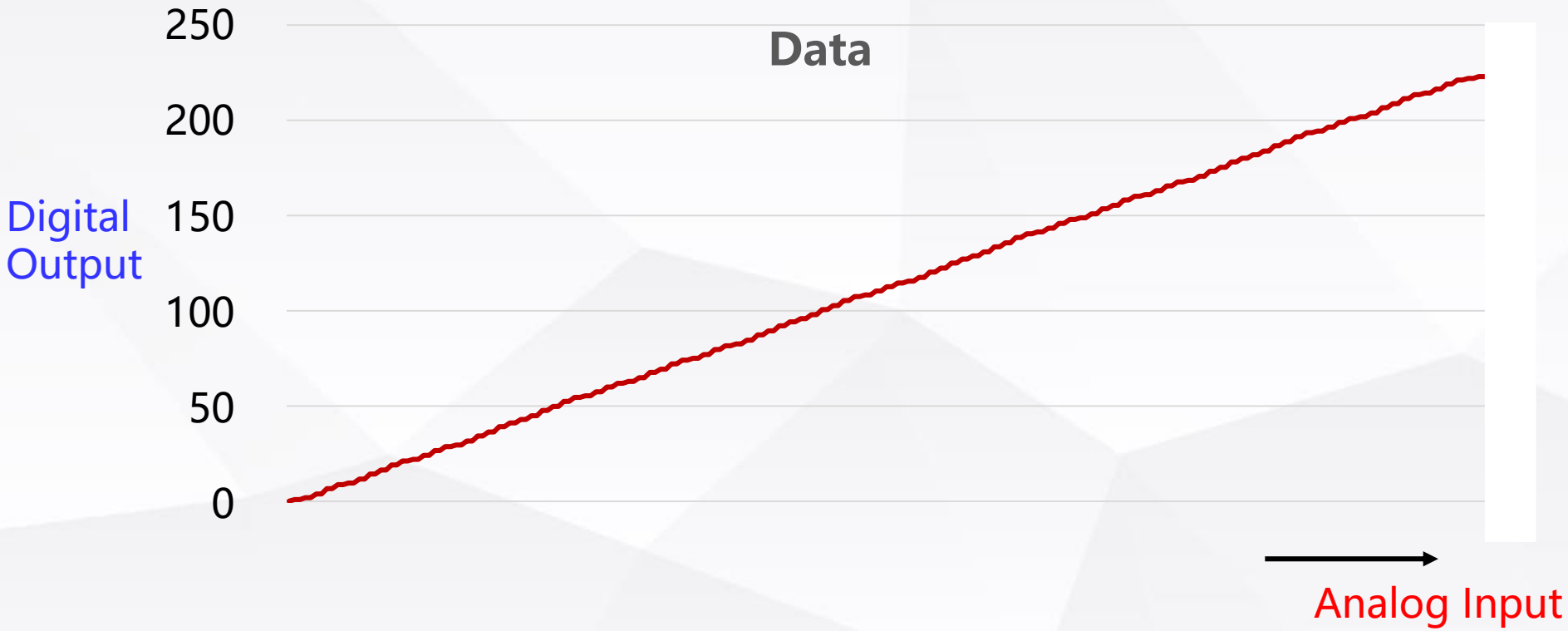
D1



Lower 5 bits

Decimal Data Calculation

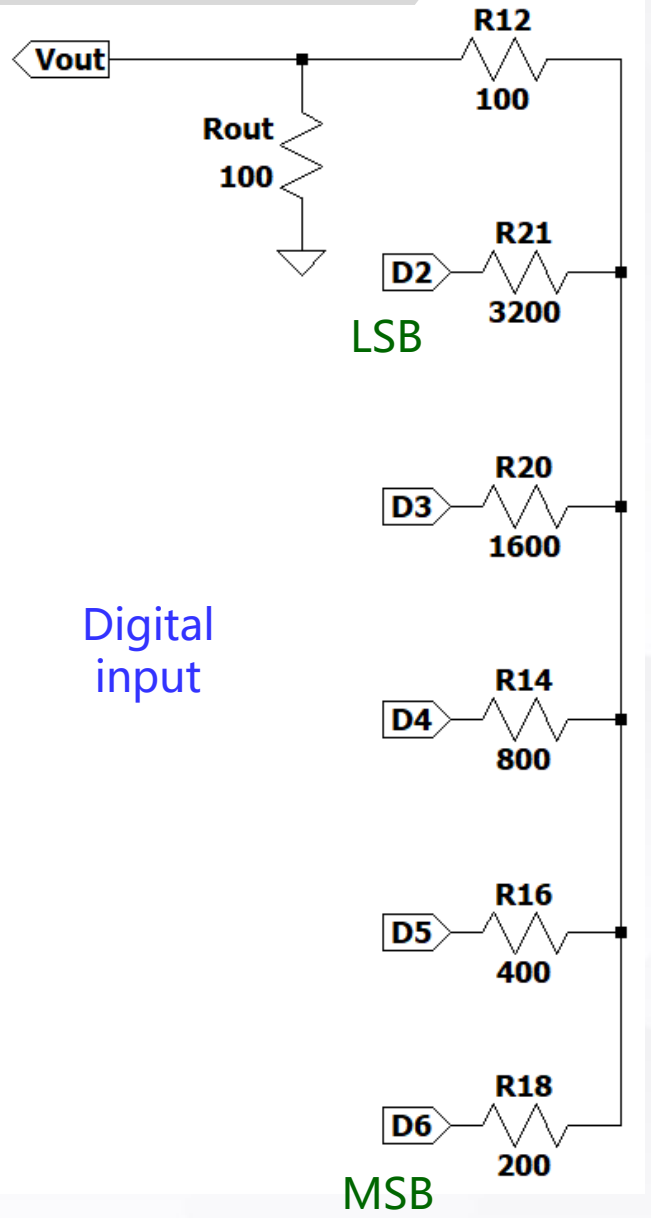
$$Data = (1/R)\,D_{10} + (1/R_9)\,D_9 + (1/R_8)D_8 + (1/R_7)D_7 + (1/R_6)D_6 + (1/R_5)D_5 + (1/R_4)D_4 + (1/R_3)D_3 + (1/R_2)D_2 + (1/R_1)D_1$$

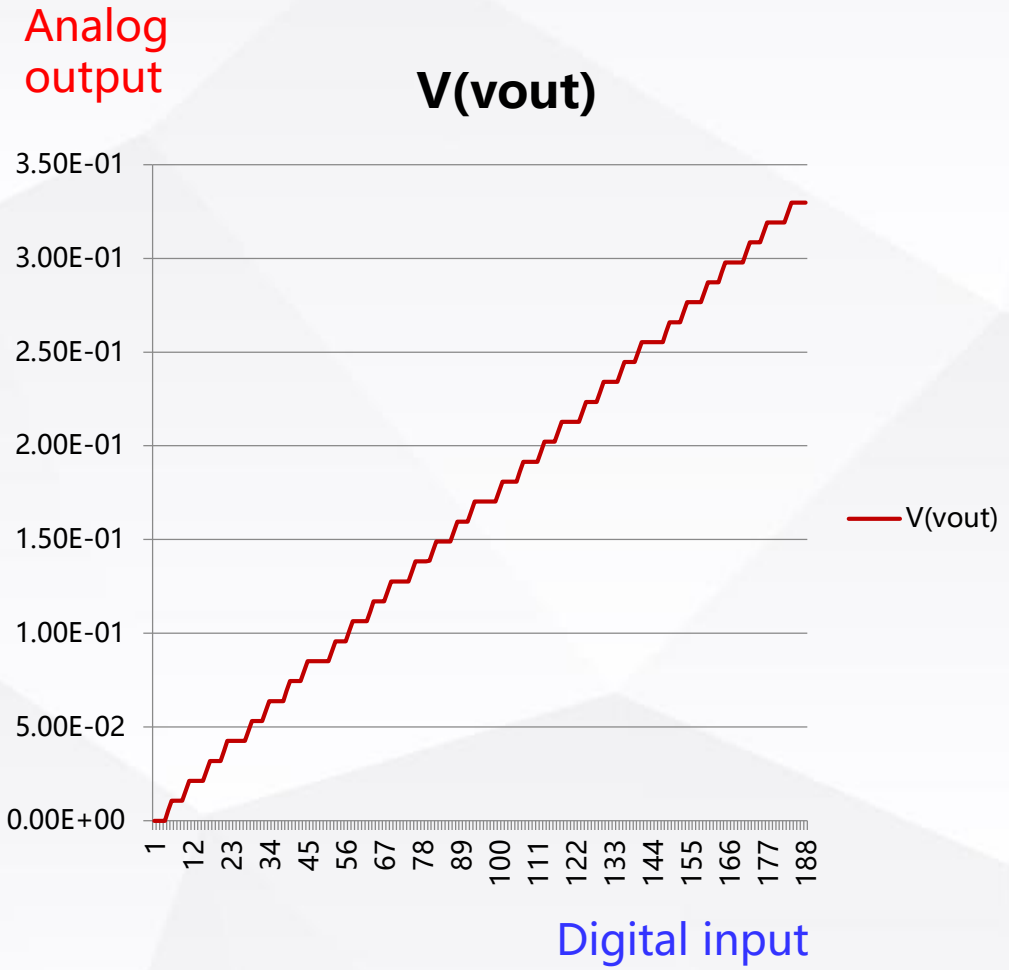


- Operation has been confirmed.

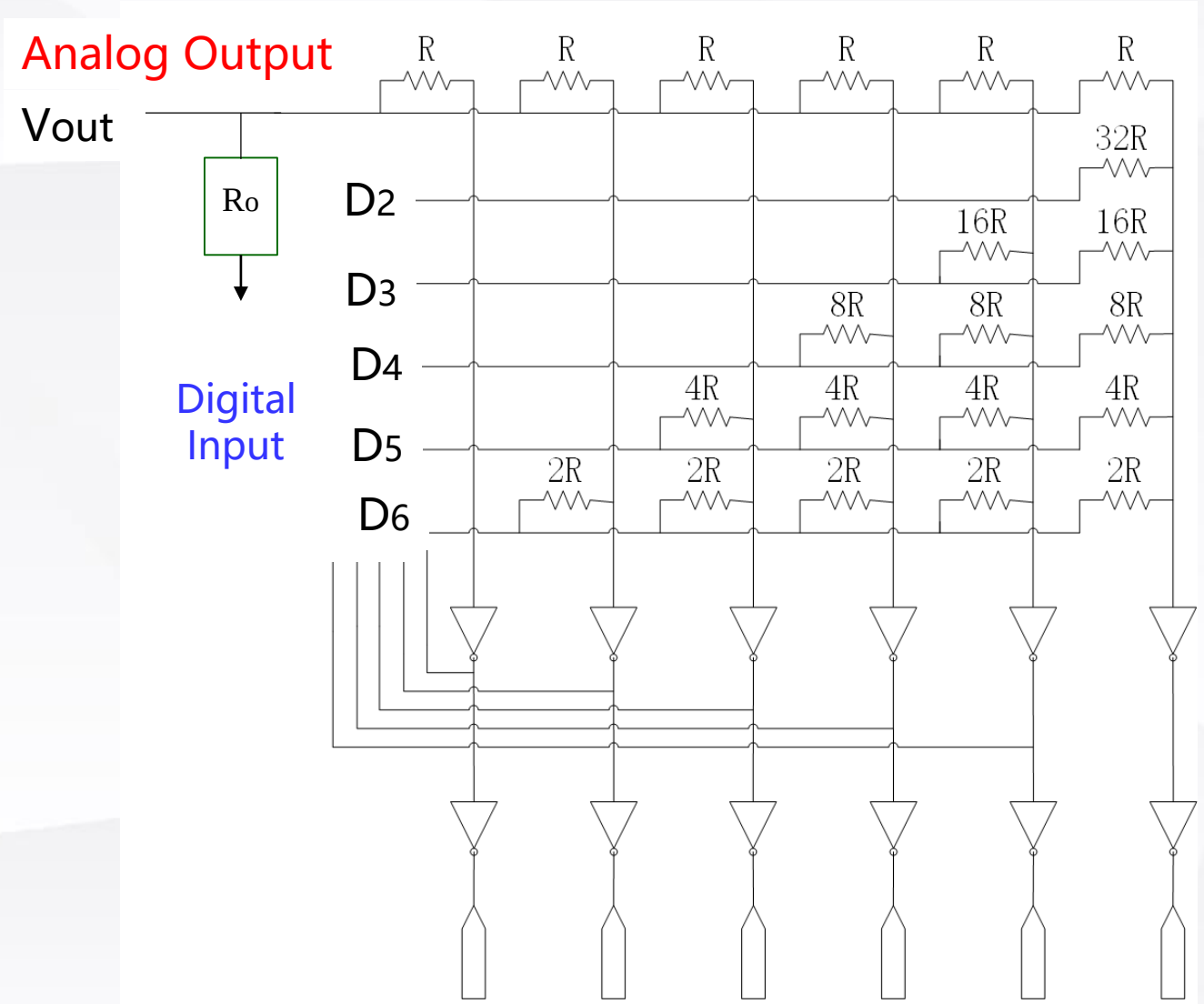
Contents

DAC inside Hopfield network

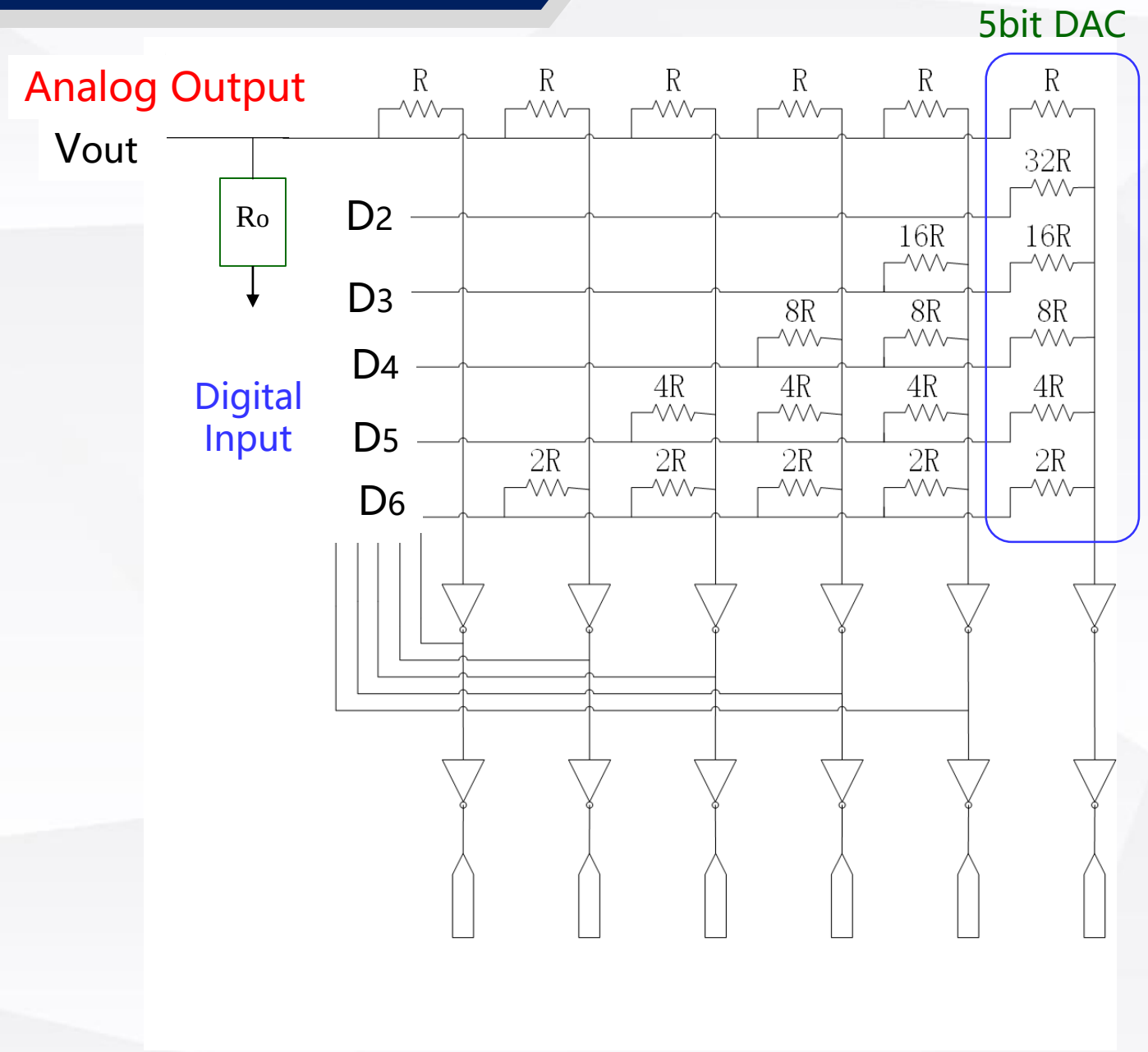




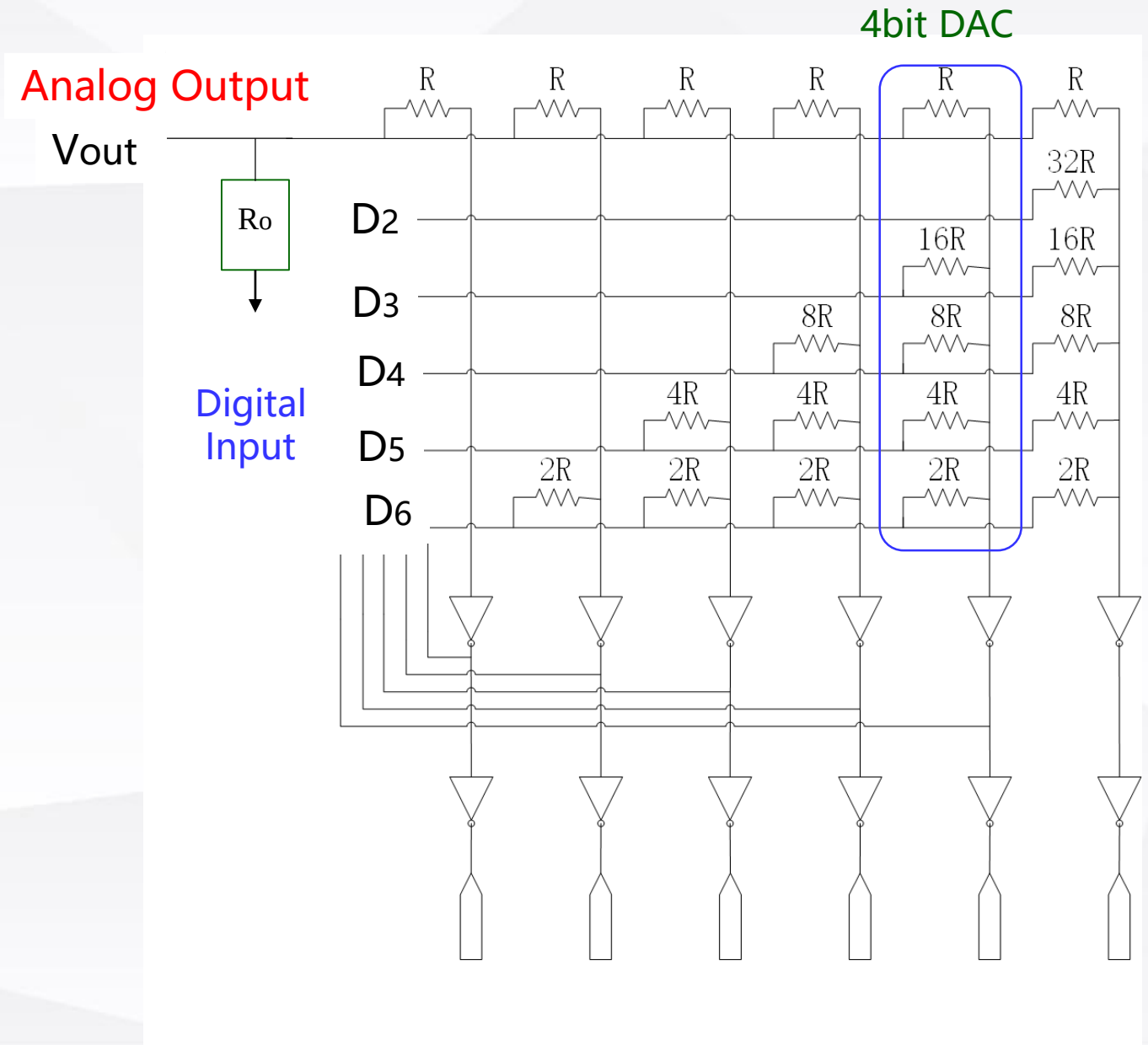
DAC array inside network



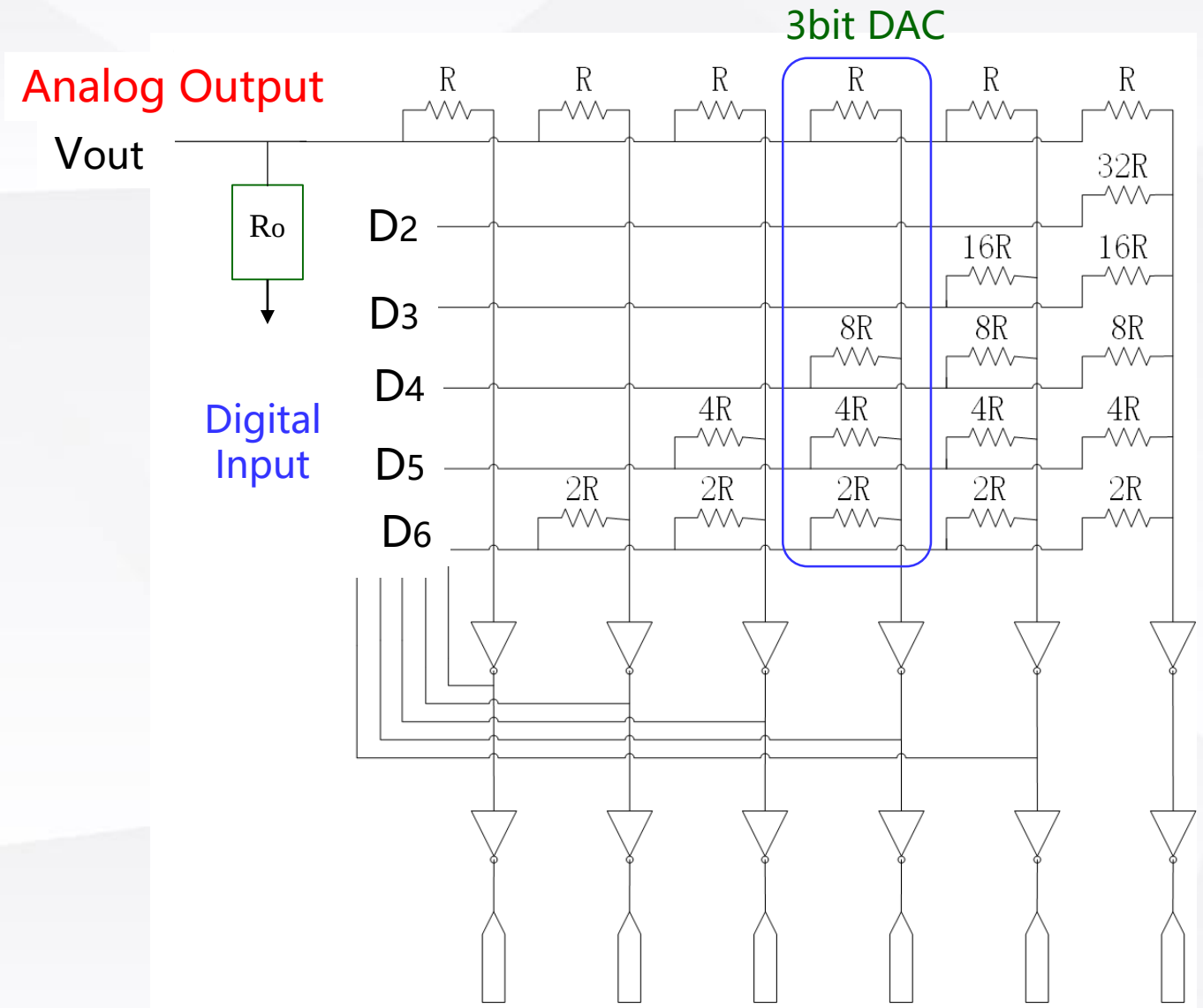
DAC array inside network



DAC array inside network



DAC array inside network



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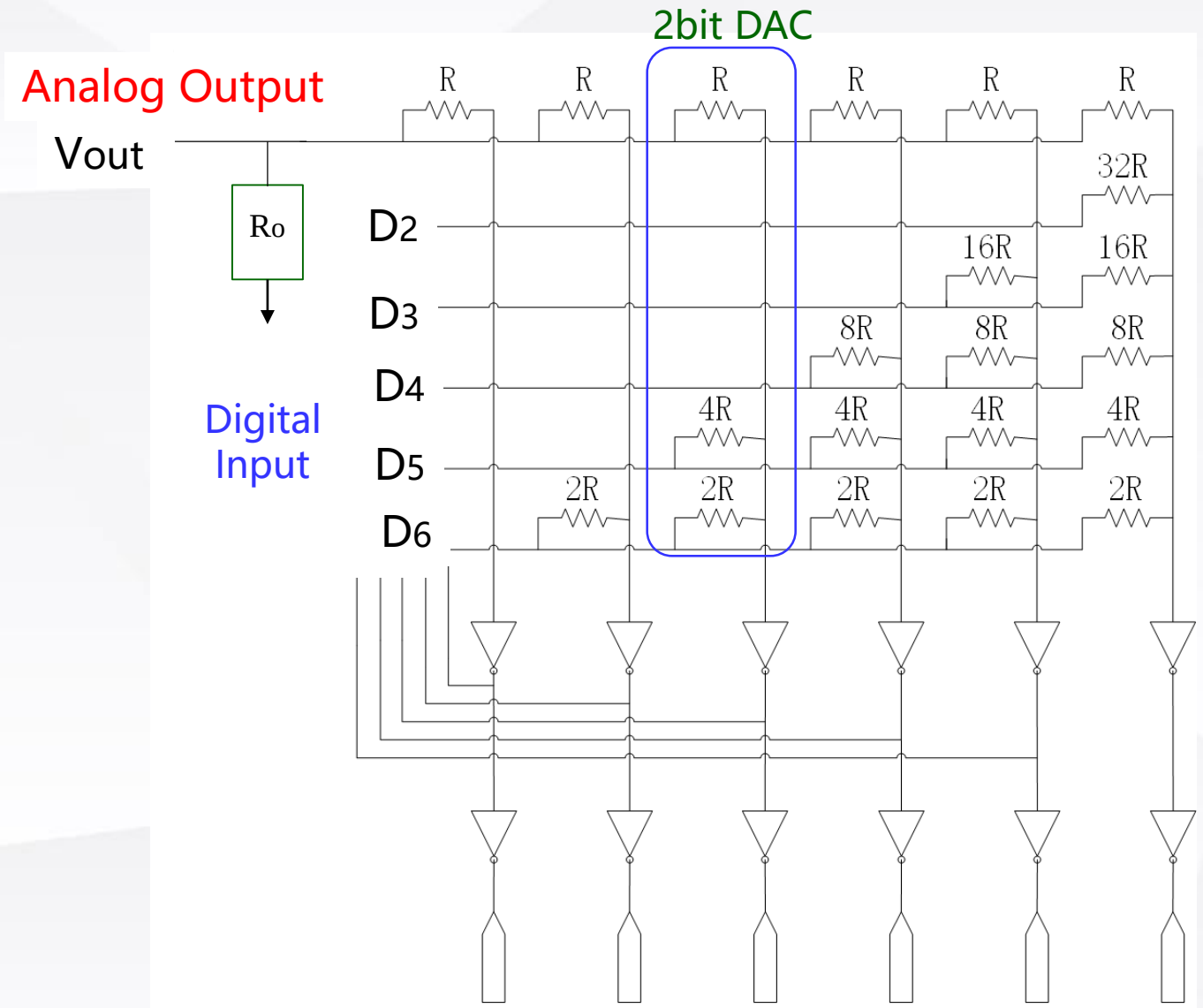
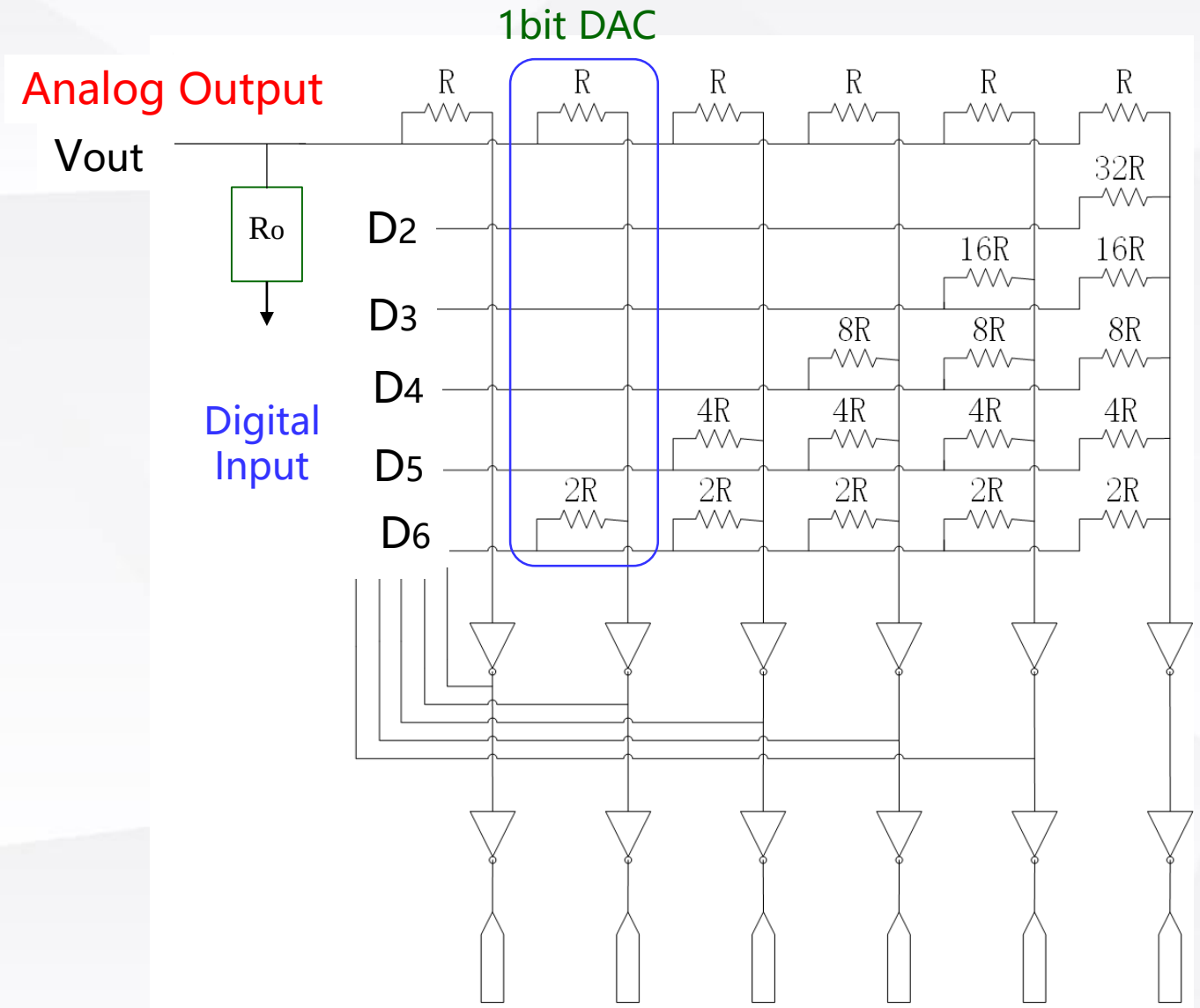


DAC array inside network



Contents

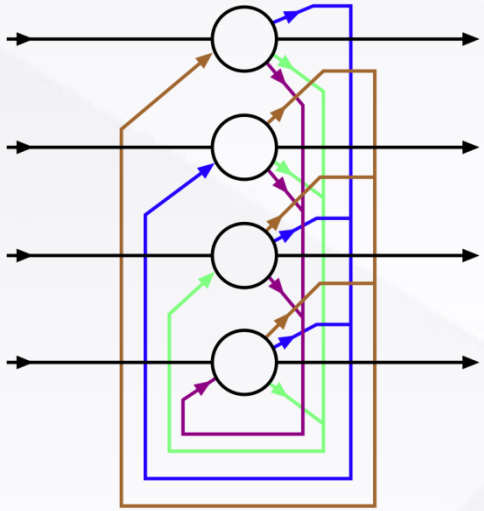
Conclusion

- Improved Hopfield network ADC
- Asynchronous SAR ADC
  - Very fast
  - Simple design
  - Non-binary as well as binary configurations
  - Competitive to state-of-the-art SAR ADC
  - Verified by SPICE simulation
- Large resistors with good matching and small chip area

  ⇒ Technology development is expected

A Hopfield network is a form of recurrent artificial neural network and a type of spin glass system popularized in 1982.

- John Hopfield



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谢谢您的倾听

Thank you for listening

ご清聴ありがとうございました