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CMOS Nagata Current Sources with Self-Bias Configuration Insensitive to Supply Voltage and Temperature

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Outline

- Research Objective
- Nagata Current Source
- Drain Current Temperature Characteristics
- Multiple-peak Current Sources
- Single-Peak Current Sources
- Conclusion

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Research Background

Analog ICs require

Reference current / voltage source

Stable against PVT variation

P: Process
V: Supply voltage
T: Temperature

Bandgap reference circuit

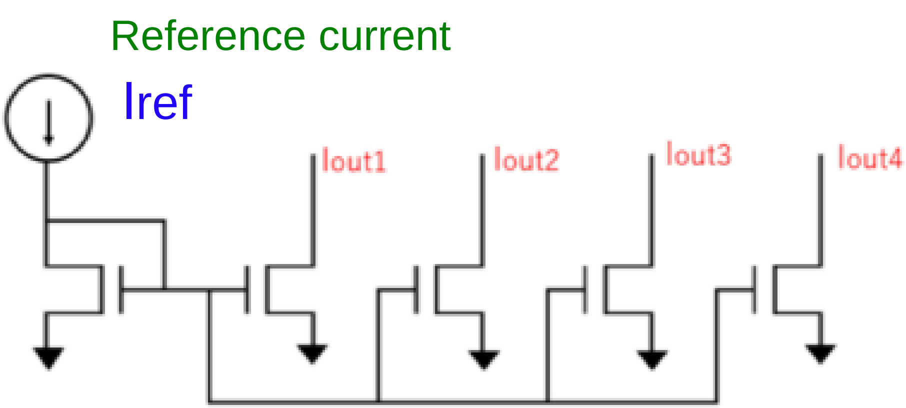
- Complicated
- Large chip area

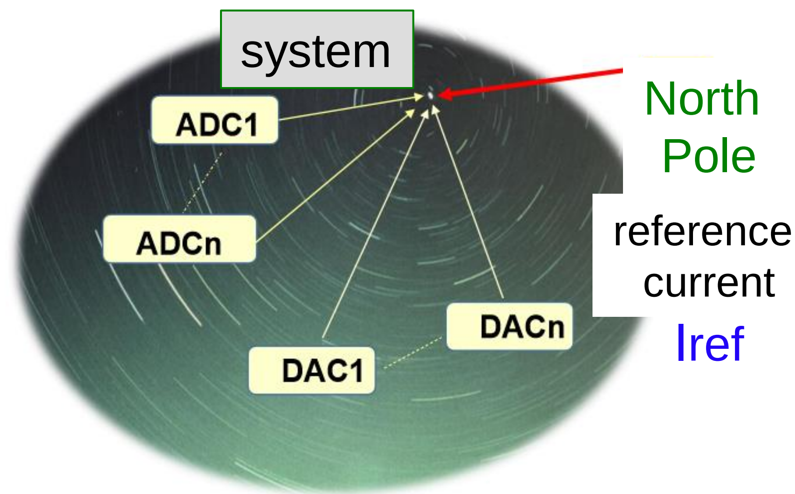
Nagata current source

- Simple
- Insensitive to supply voltage

Research Objective

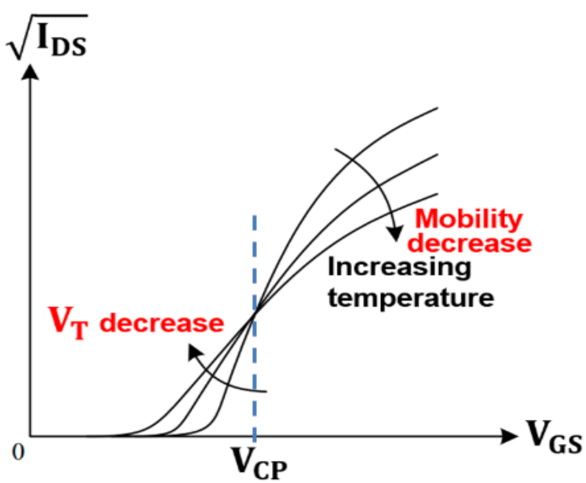
Development of reference current source insensitive to temperature and supply voltage with simple CMOS circuit.



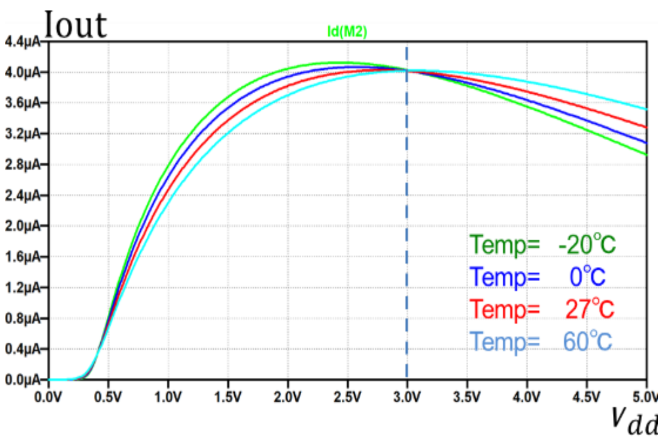


Our Approach

- MOS peaking current sources
  - Self-bias ➡ - Insensitive to wide range of supply voltage
    - No need for large input resistor
  - Focus on cross-point gate voltage (VCP) in drain current temperature characteristics
    ➡ Insensitive to temperature



NMOS drain current



Current source insensitive to temperature and supply voltage

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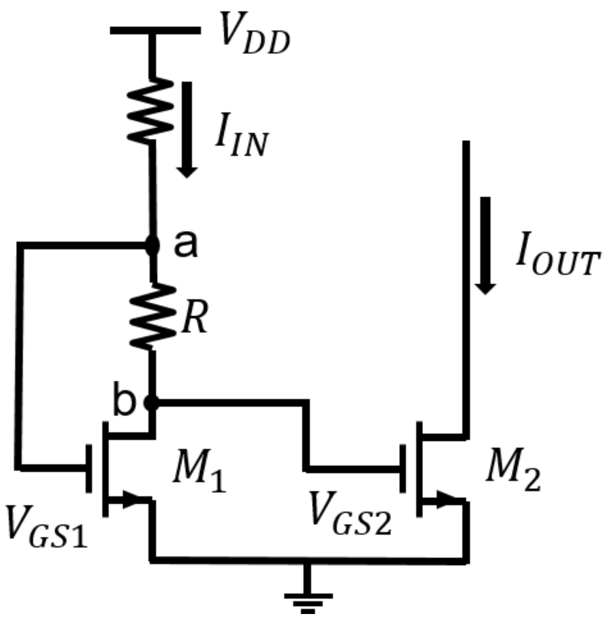
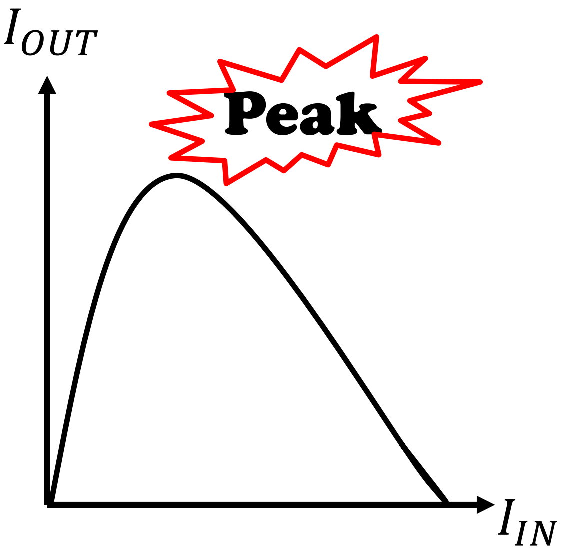
Original Nagata Current Source



MOS Nagata Current Source



Peaking current characteristics

At peak vicinity

Small I_{OUT} change against I_{IN} change

Simple → Widely used. Ex: in DC-DC converter ICs

Japanese Invention

Peaking current source
(Nagata current mirror)
was invented by
Dr. Minoru Nataga,
Japanese,
worked for Hitachi Ltd.
In 1964.

[1] Chris Mangelsdorf,
"Stupid FET Tricks: The Zero-Gain Amplifier",
IEEE Solid-State Circuits Magazine
(Aug. 2021)

A MIRROR THAT REFLECTS WELL ON ITS INVENTOR

FIGURE S1: Dr. Minoru Nagata.

Within the Asian circuits community, the inventor of the Nagata current mirror is about as close to a legend as you can get in our business. Even if you don't spend much time in Asia, there's a good chance you've encountered Dr. Minoru Nagata (Figure S1). He is in high demand as a panelist and presenter around the world because of his unique ability to charm the socks off even the most aloof international audiences.

Dr. Nagata may be best known for his widely used textbooks and his work on the Japanese language version of the Gray and Meyer text. He is a cofounder of the VLSI Circuits Symposium and served as its very first program chair. He has had a long, distinguished career at Hitachi Ltd., where he ultimately held the post of Director and Senior Chief Engineer of Corporate Technology. Among his many accolades are the IEEE Fredrick Philips Award and the National Medal of Honor from the Emperor of Japan.

And the mirror? It set the bias for the first analog IC designed and produced in Japan, the Hitachi HA1303 amplifier (Figure S2).

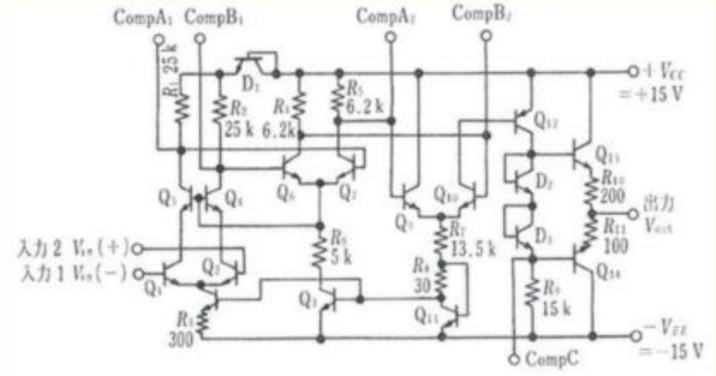
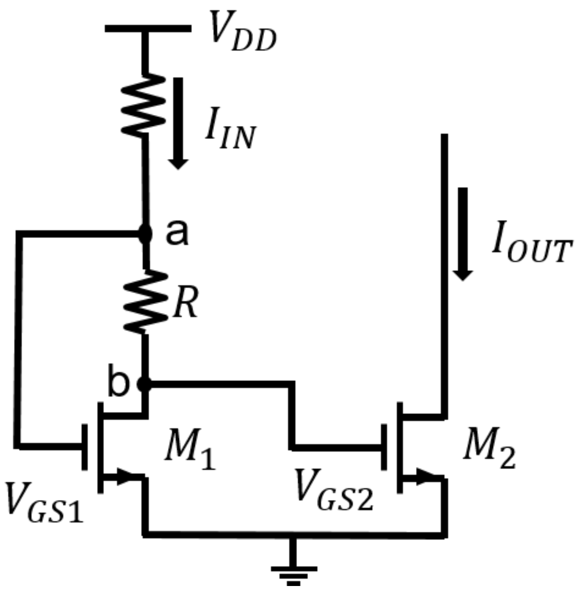


図 9.32　IC 演算増幅器の回路例（2）（HA 1303）
（カスコード増幅回路，同相負帰還回路および安定化された定電流回路などが使用されている）

FIGURE S2: The schematic for the Hitachi HA1303 amplifier.

Circuit Configuration and Operation (1)

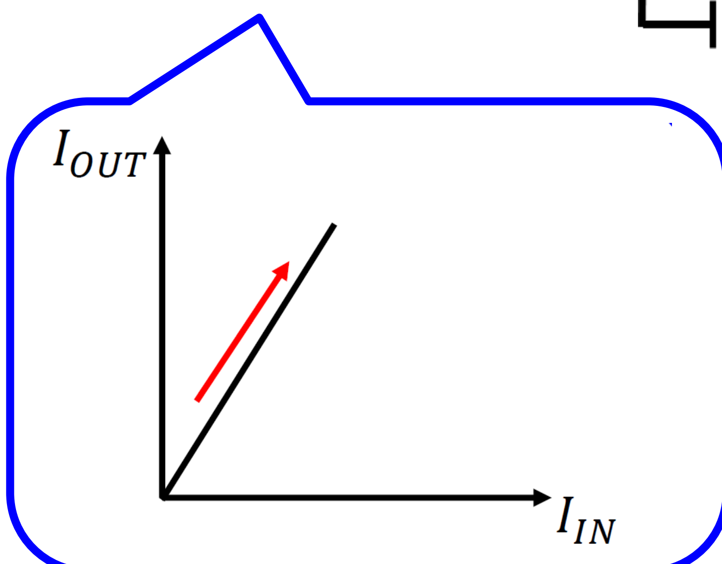


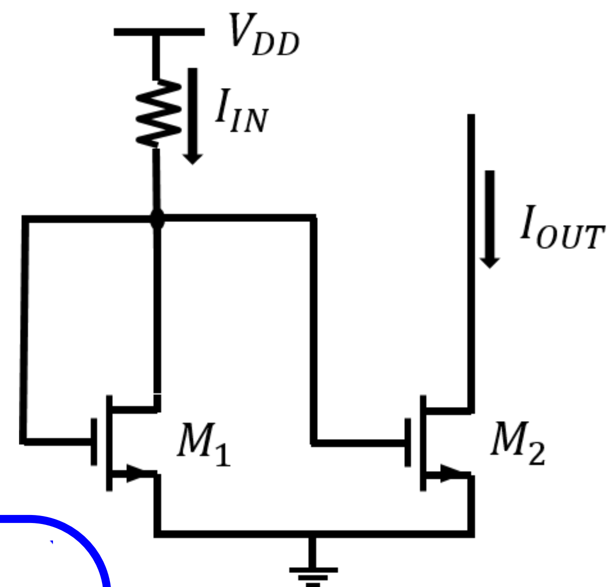
Nagata current source

I_{IN}: small

RI_{IN}: small

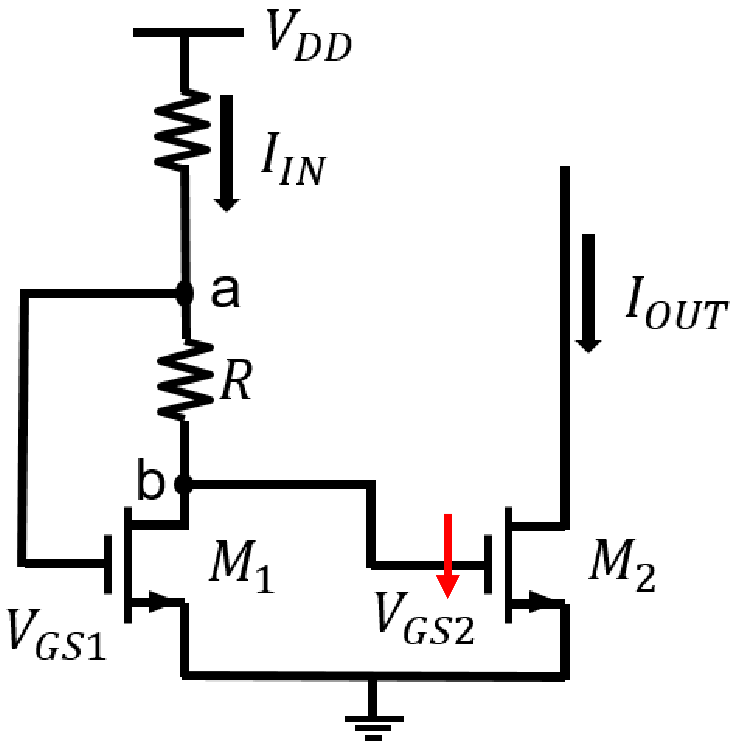
$$I_{IN} = I_{OUT}$$





Current Mirror

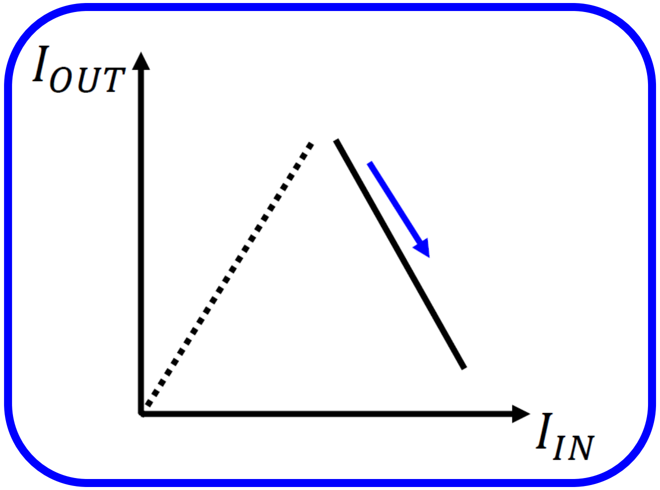
Circuit Configuration and Operation (2)



I_{IN}: large

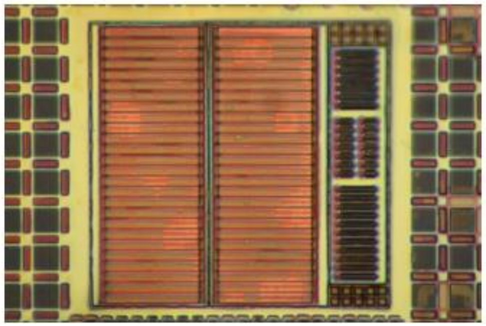
→ RI_{IN}: large

→ V_{GS2} becomes smaller

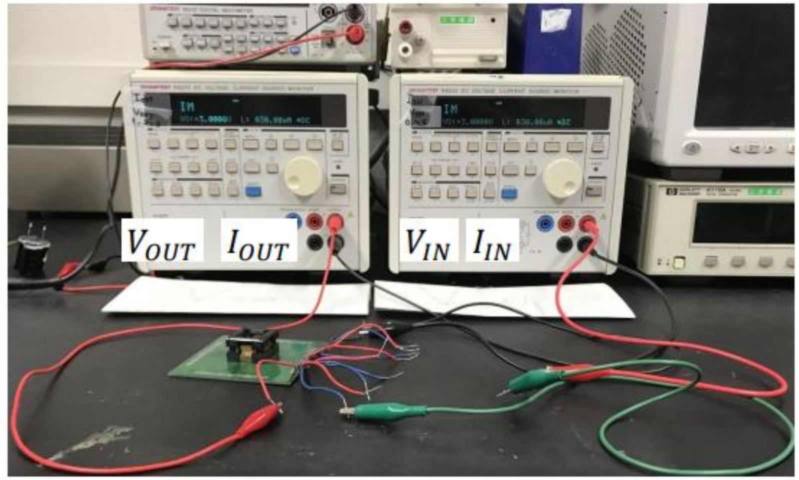


Need Care for Temperature

Layout by
ASO Corp.



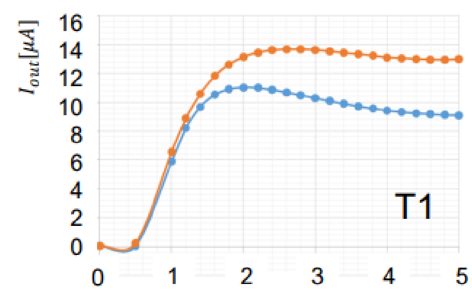
Our first prototype chip

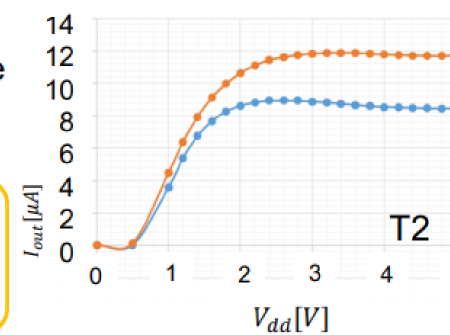


Measurement environment

Insensitive to supply voltage

Sensitive to temperature





Room temperature

High temperature

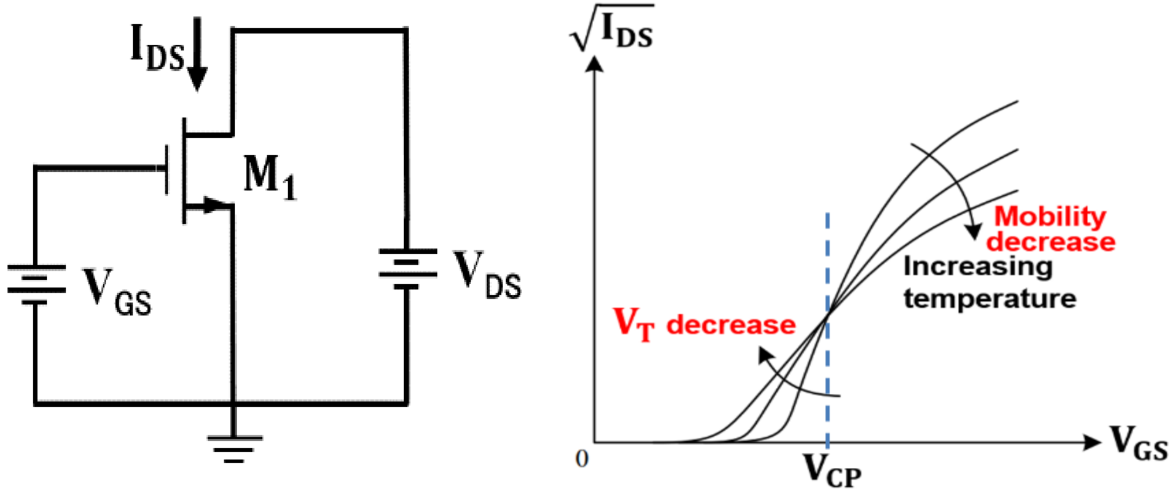
Use a hair dryer

Our previous work

[2] M. Hirano, N. Kushita, Y. Moroshima, H. Harakawa, T. Oikawa, N. Tsukiji, T. Ida, Y. Shibasaki, H. Kobayashi, "Silicon Verification of Improved Nagata Current Mirrors", IEEE ICSICT(Nov. 2018)

Outline

Drain Current Temperature Characteristics



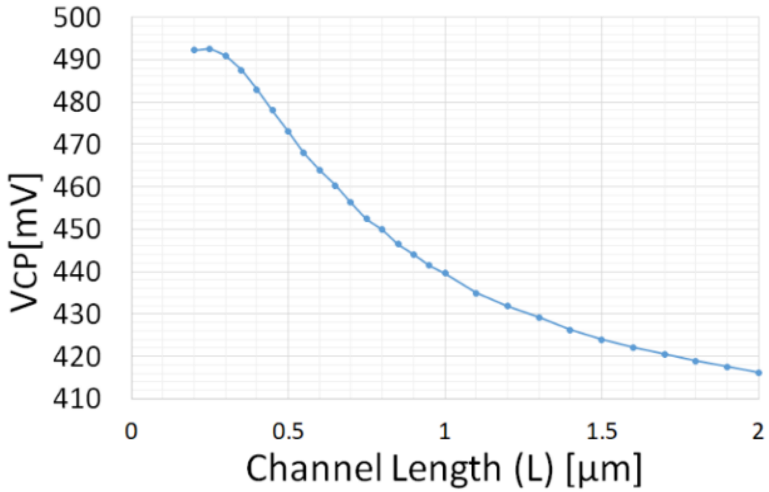
NMOS drain current temperature characteristics

- For $V_{GS} = V_{CP}$, I_{DS} ⇨ Insensitive to temperature.
- At high temperature,

For $V_{GS} < V_{CP}$, I_{DS} ⇨ larger

For $V_{GS} > V_{CP}$, I_{DS} ⇨ smaller.

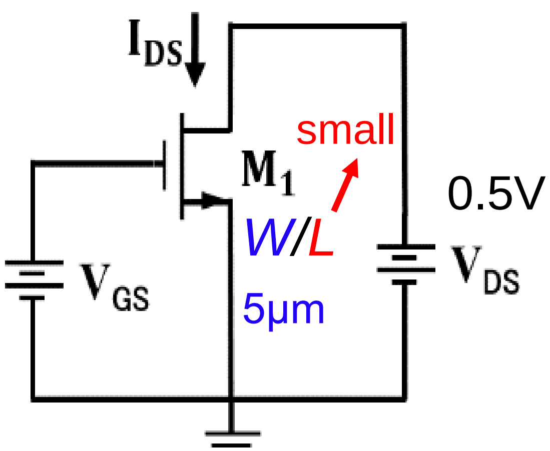
VCP and Small Channel Length *L*

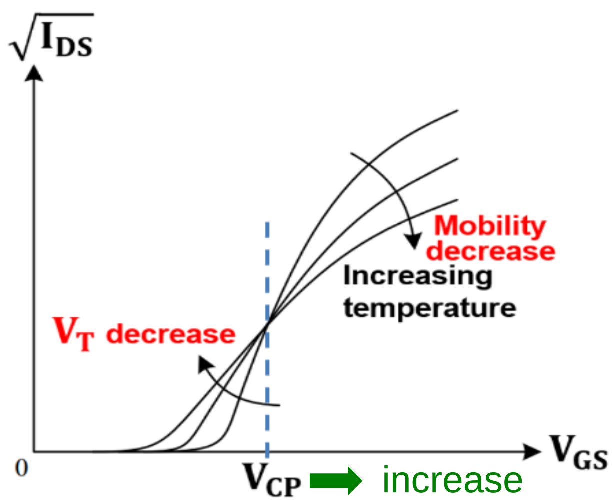


SPICE simulation
with BSIM3v3 model parameters

L → small ➡ VCP → increase

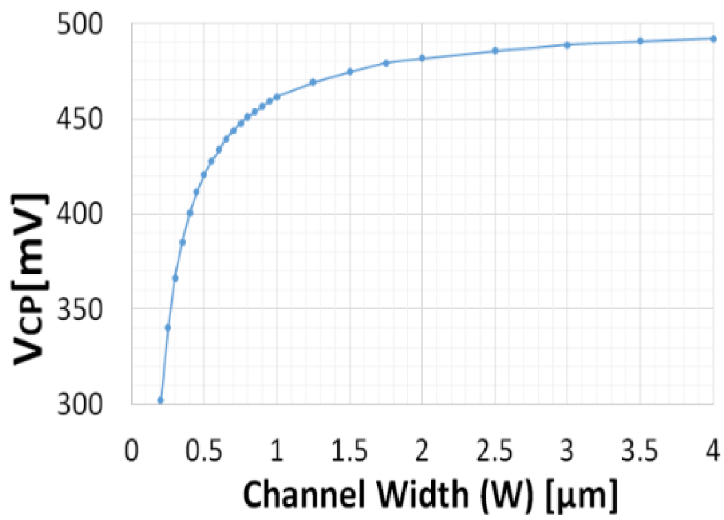
Explained by short channel effect





NMOS drain current temperature characteristics

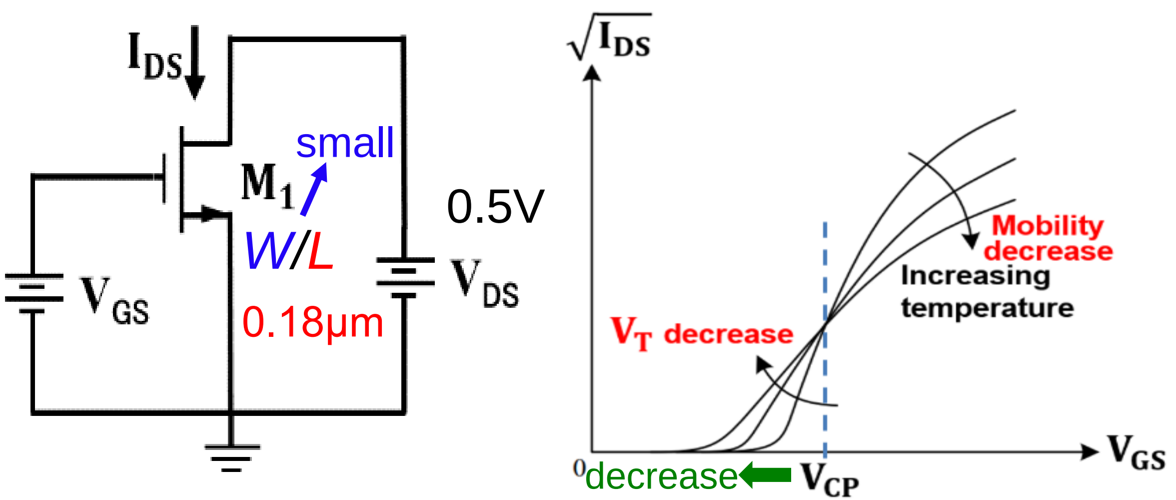
V_{CP} and Small Channel Width W



SPICE simulation result
with BSIM3v3 model parameters

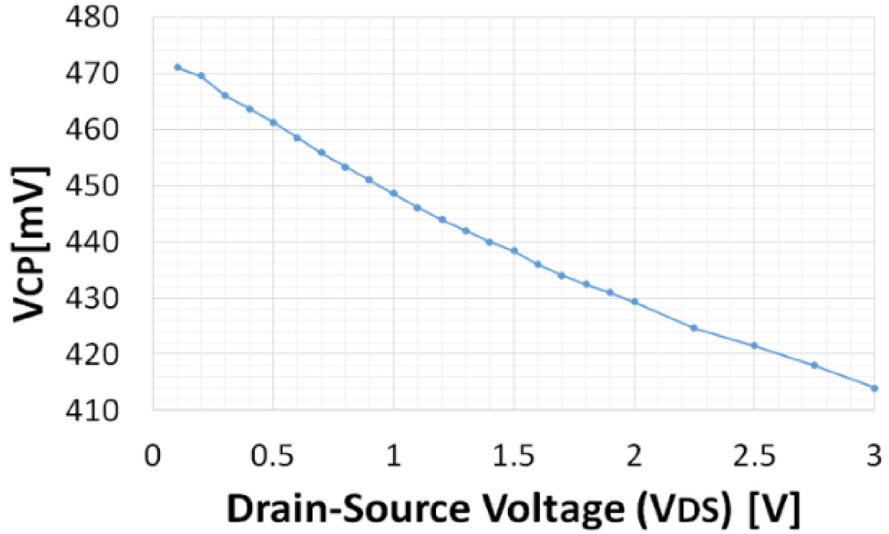
W → small ➡ V_{CP} → decrease

Explained by narrow channel effect



NMOS drain current temperature characteristics

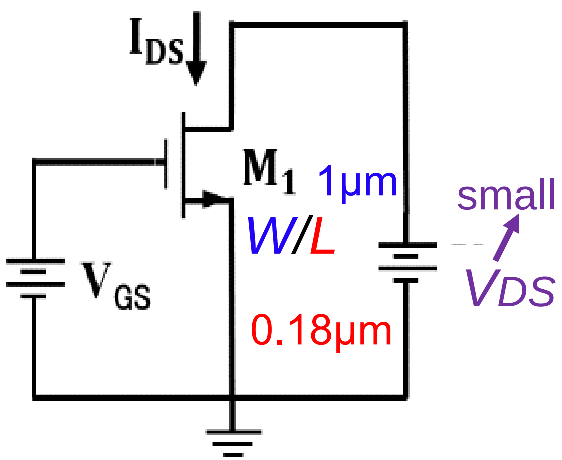
V_{CP} and Drain-Source Voltage V_{DS}

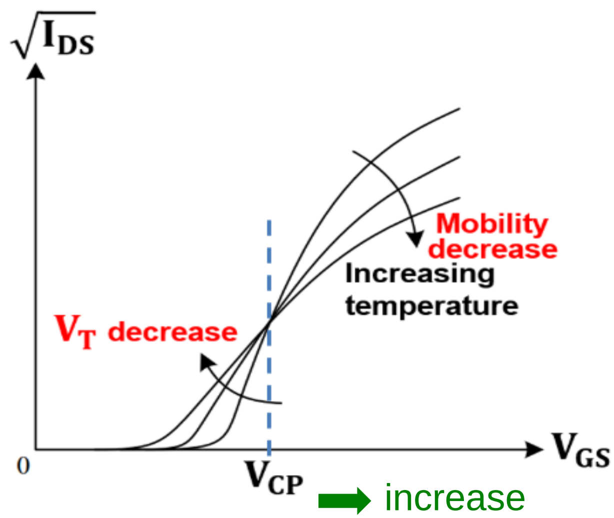


SPICE simulation result
with BSIM3v3 model parameters

V_{DS} → small ➡ V_{CP} → increase

Explained by
drain induced barrier lowering *(DIBL)*





NMOS drain current temperature characteristics

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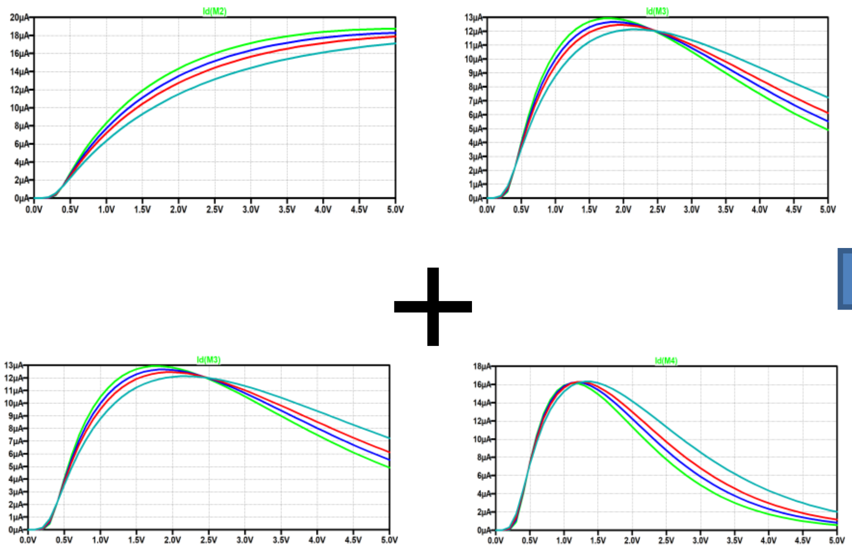
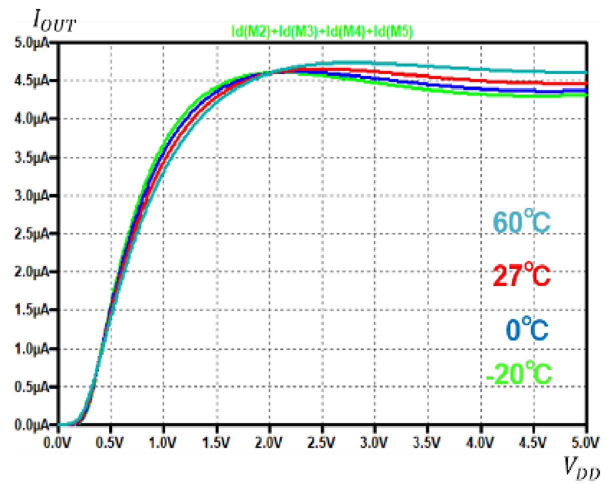
Multiple-Peak Circuit Design

Use of multiple peaking current sources

Current source design → relatively easy

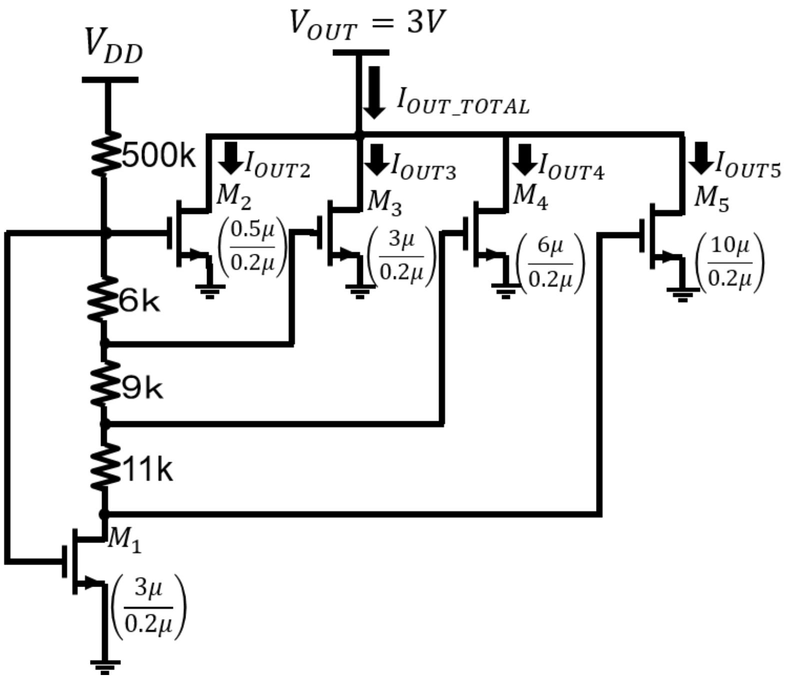


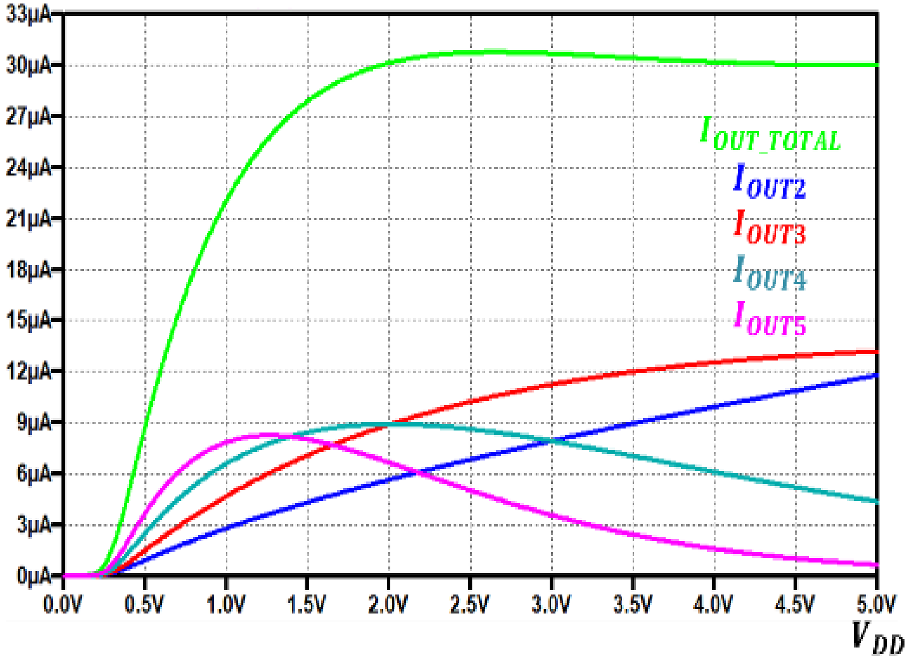


Multiple peaks

⇒ Total output current : Insensitive to supply voltage and temperature

NMOS Multiple-Peaking Current Sources

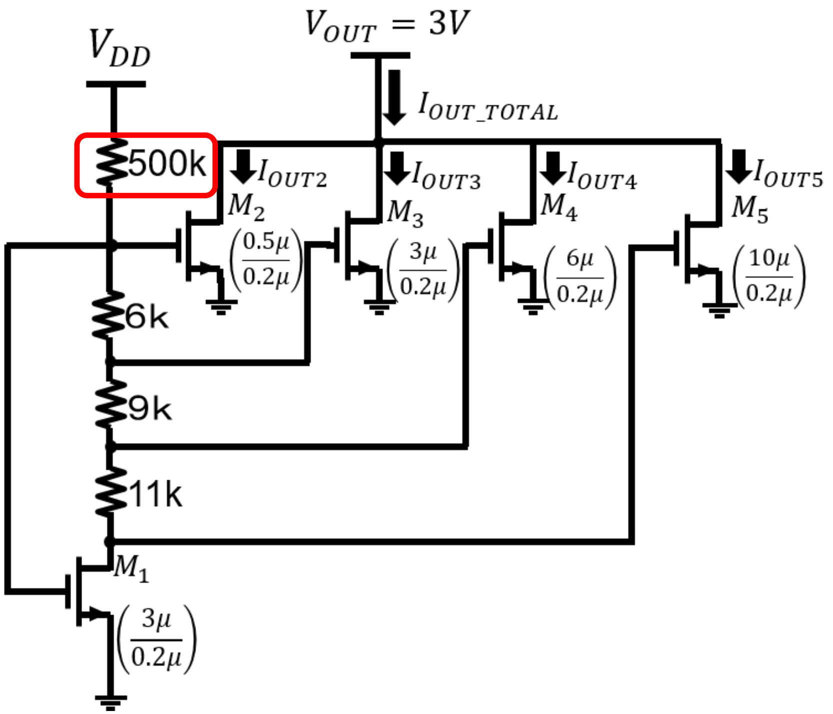


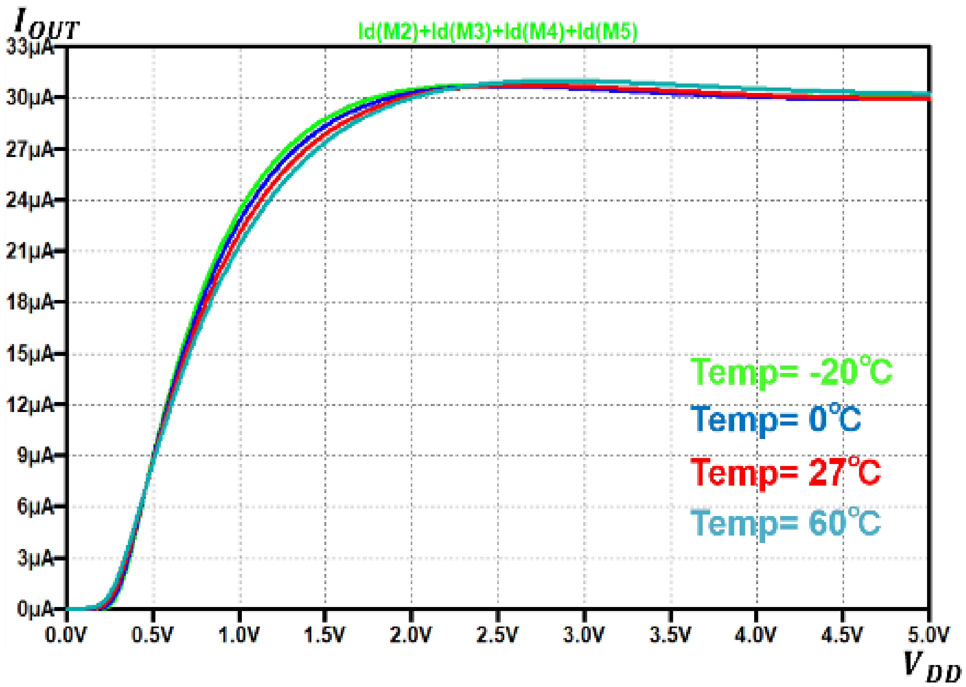


Total output current

→ Constant over wide range of supply voltage

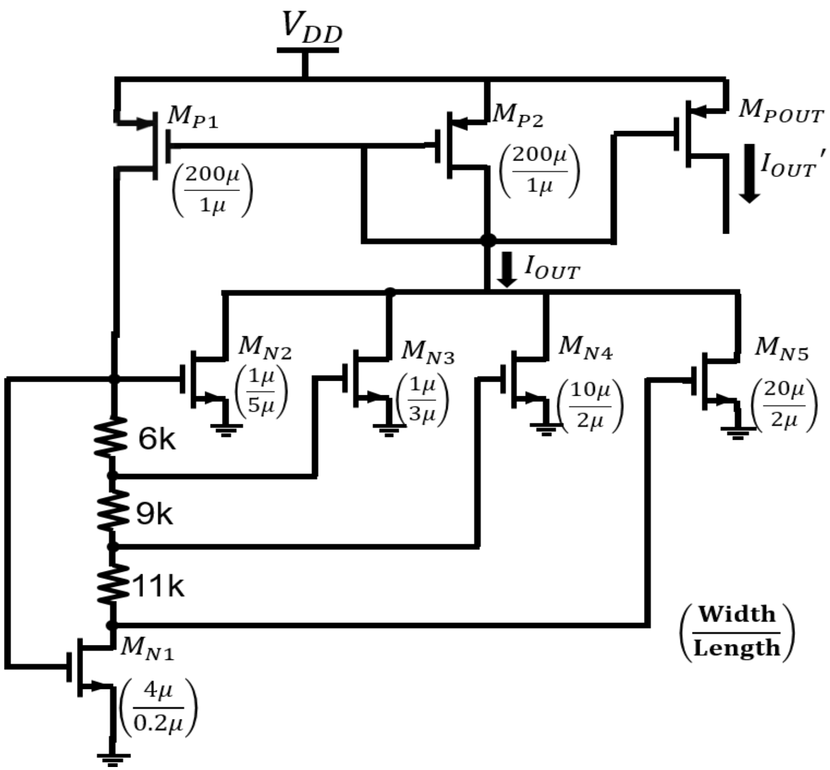
Temperature Characteristics

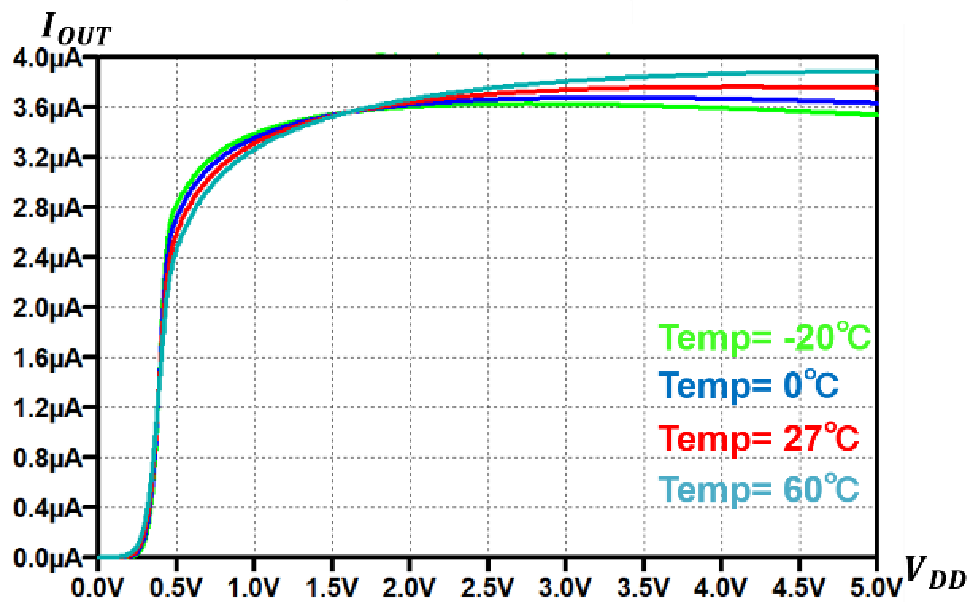




- Insensitive temperature characteristics
- Need large resistor to generate µA-order input current

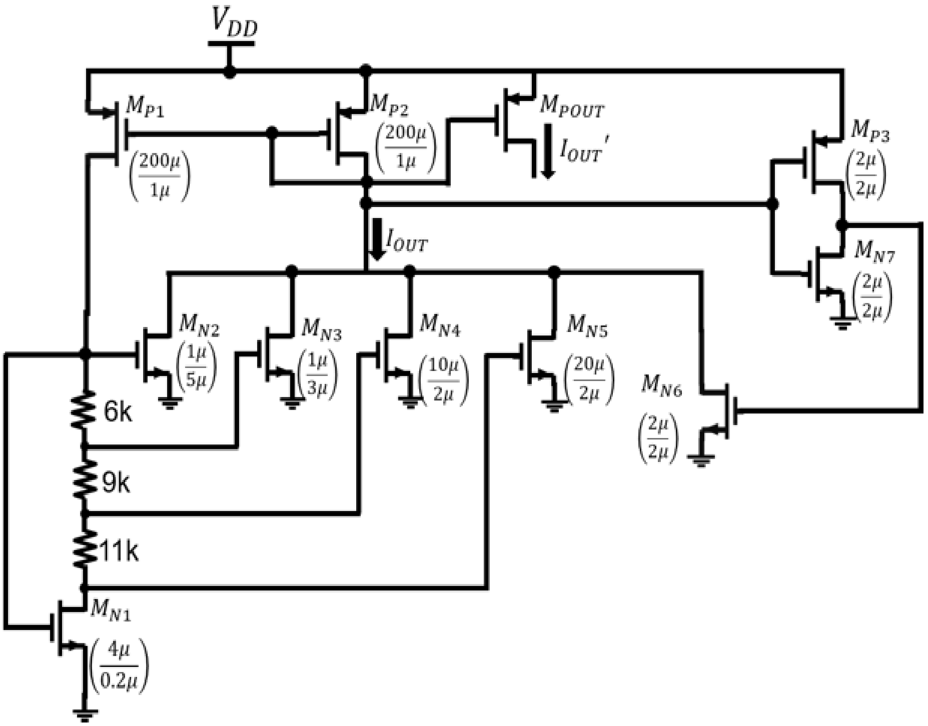
Self-Bias Configuration

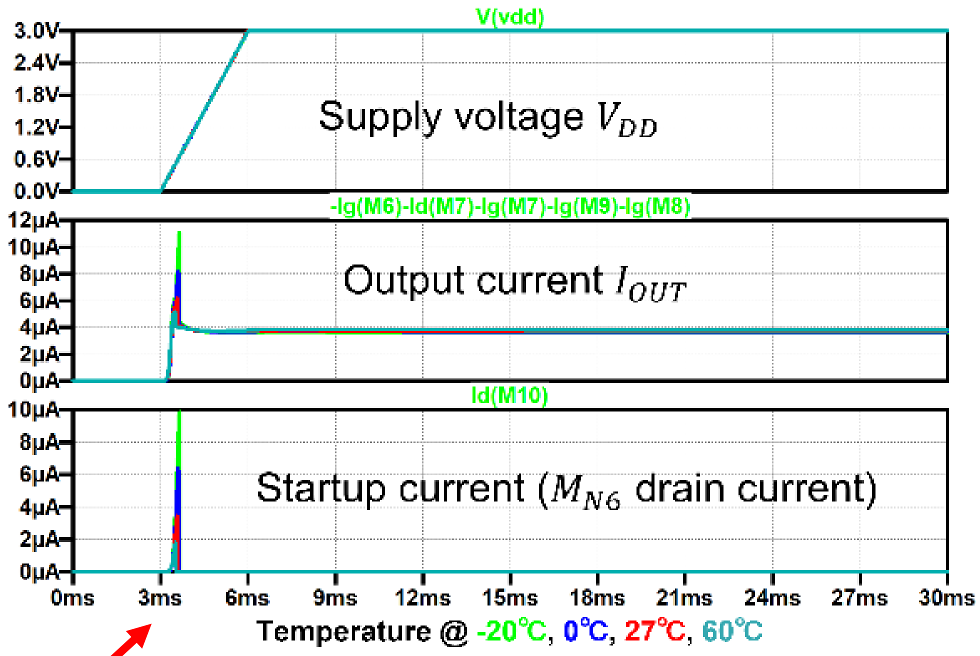




Use self-bias configuration → No need for large resistor

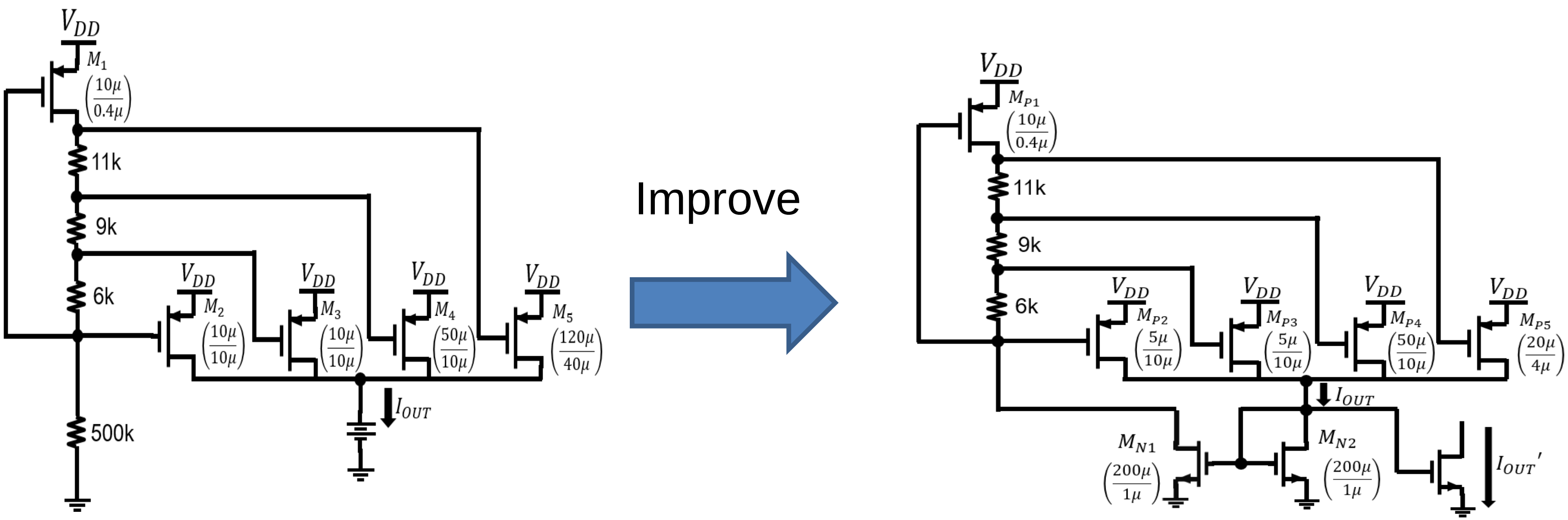
Start-up Circuit





Start-up circuit is working

PMOS Multiple-Peaking Current Sources



Also in PMOS case,

No need for large input resistor by self-bias configuration

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- **Single-Peak Current Sources**
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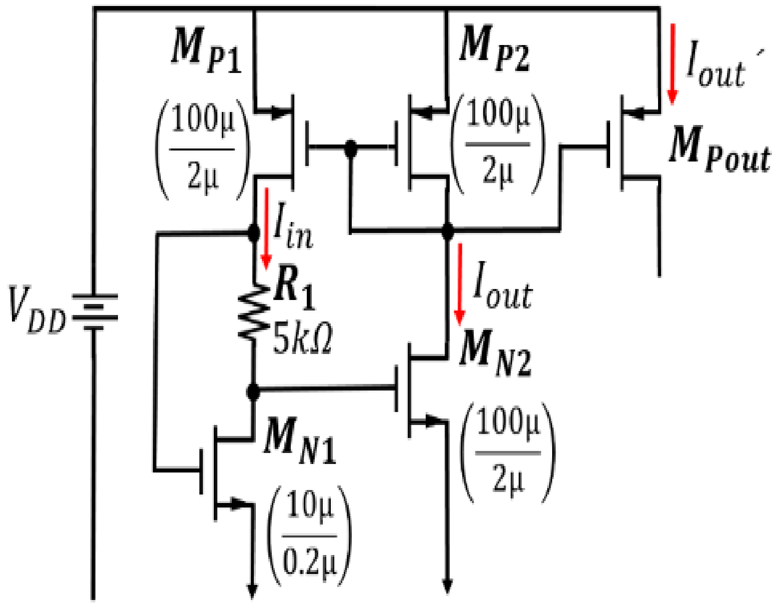
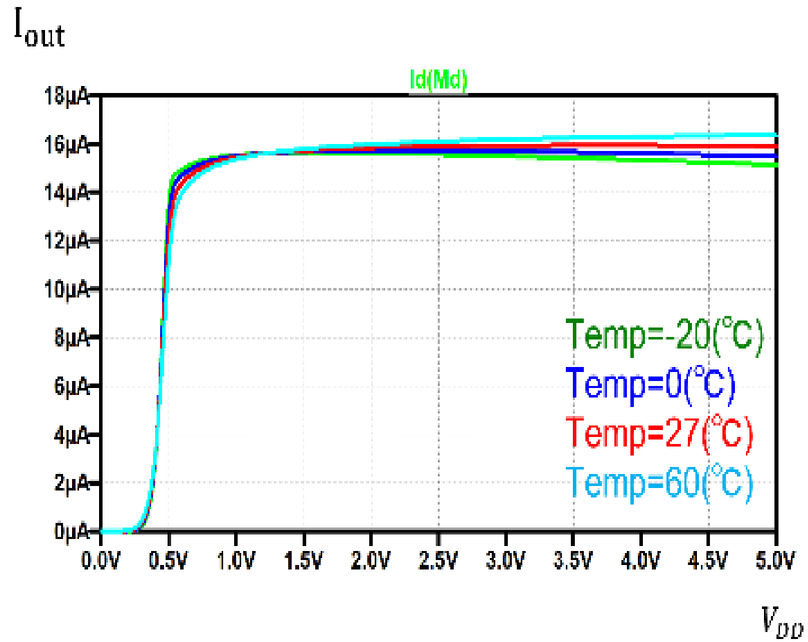
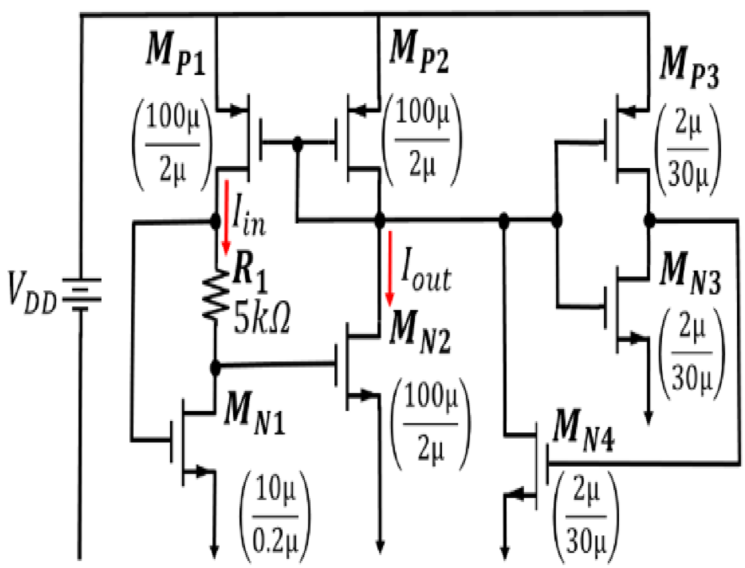
Self-Bias NMOS Single-Peak Current Source

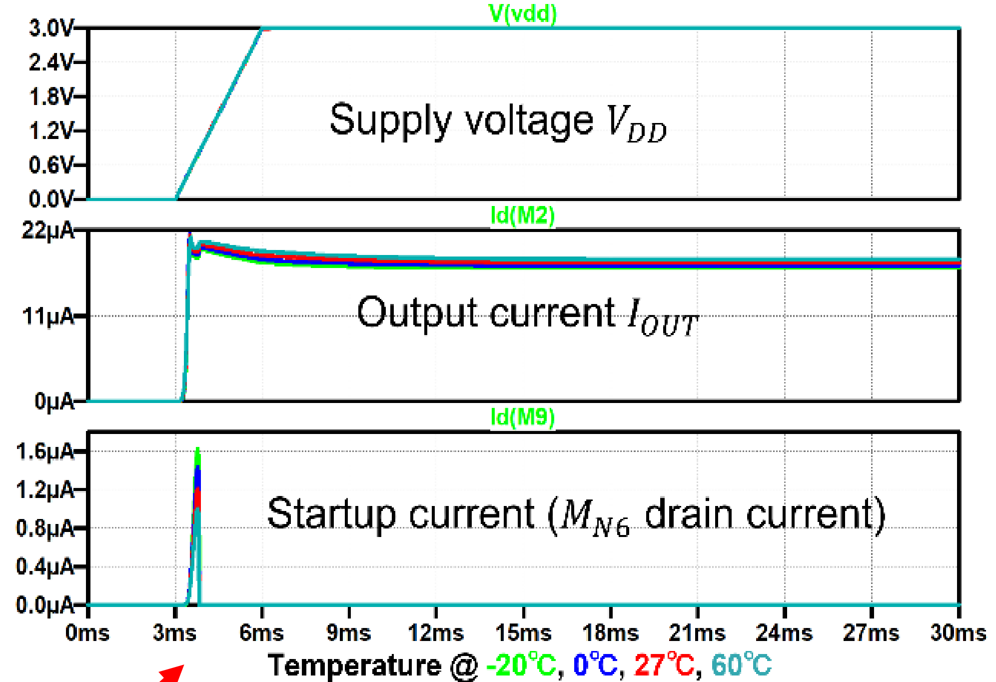




Self-bias configuration → VDD insensitivity range → Widened

Single-Peak Current Source with Startup Circuit



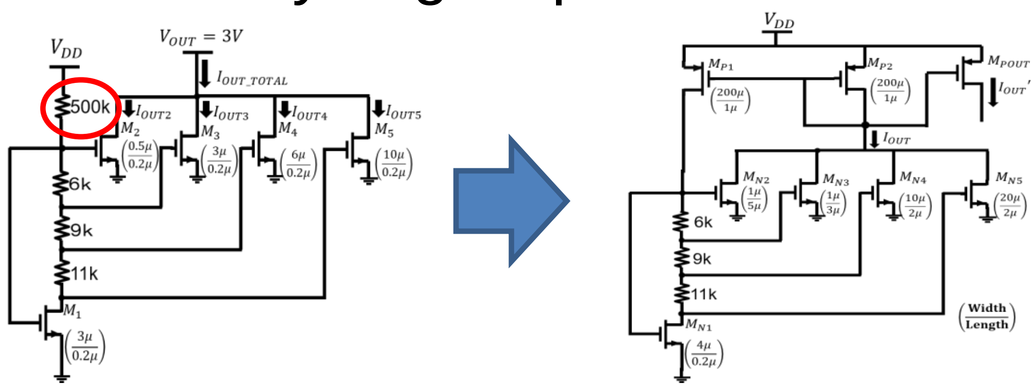


Start-up circuit is working

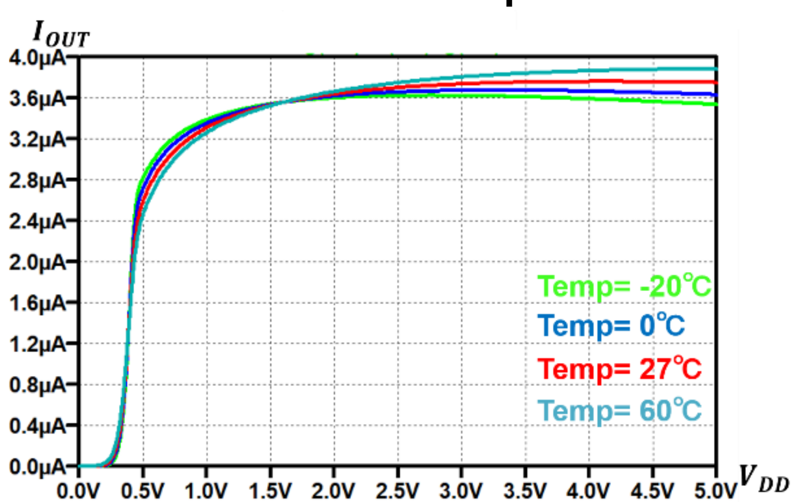
Why Self-Bias Configuration ?

Because

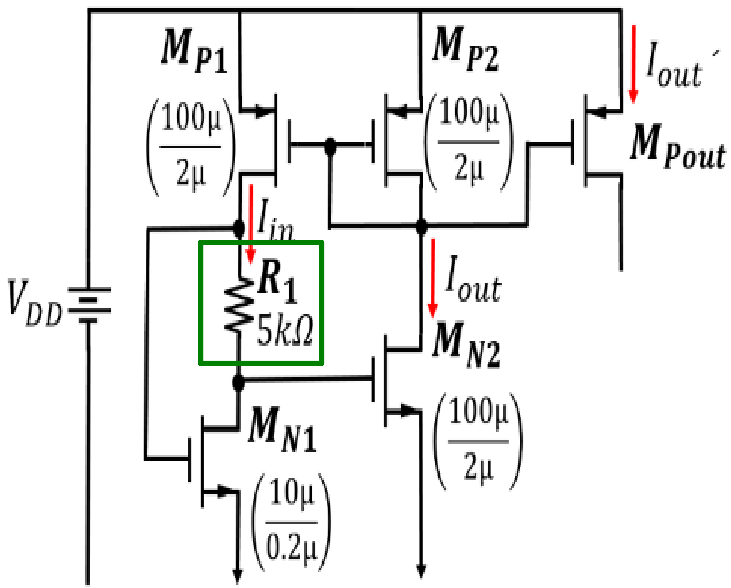
- Not need very large input resistor

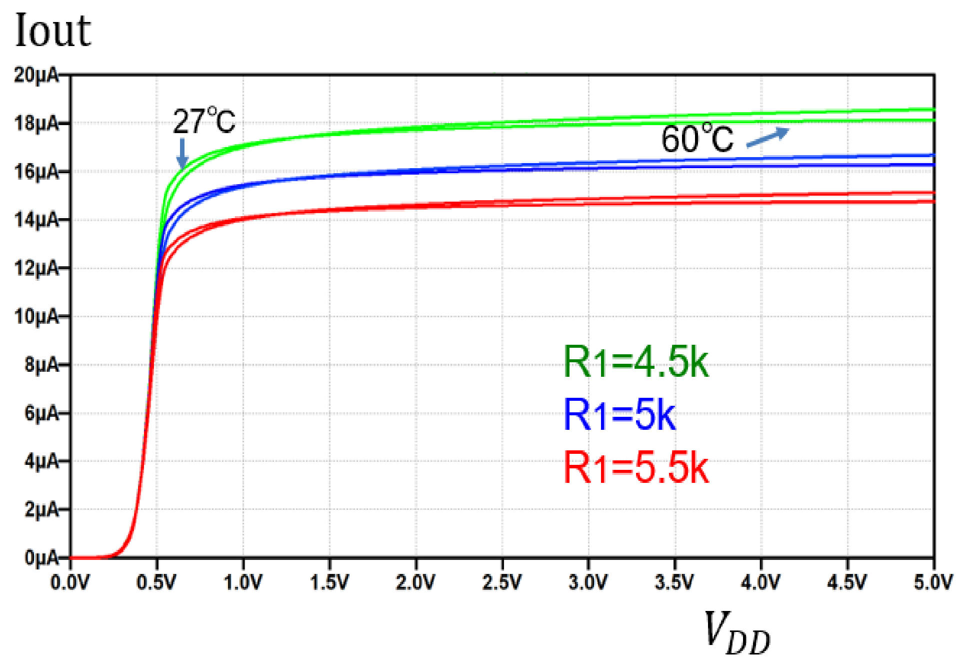


- Obtain wide range of VDD insensitivity easily and temperature insensitivity



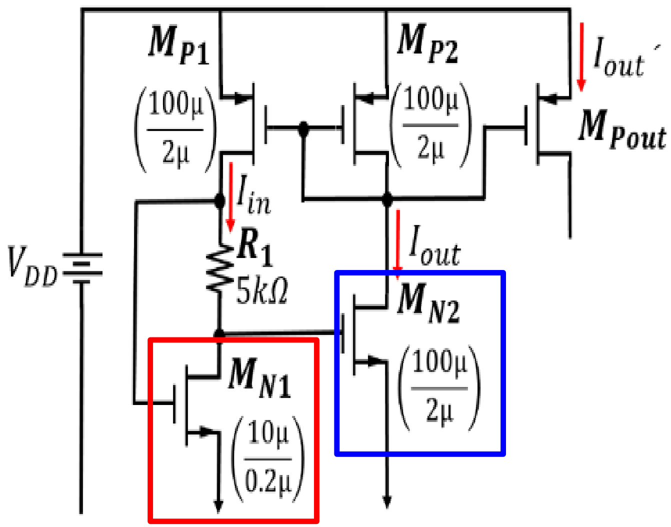
R1 Variation Effects

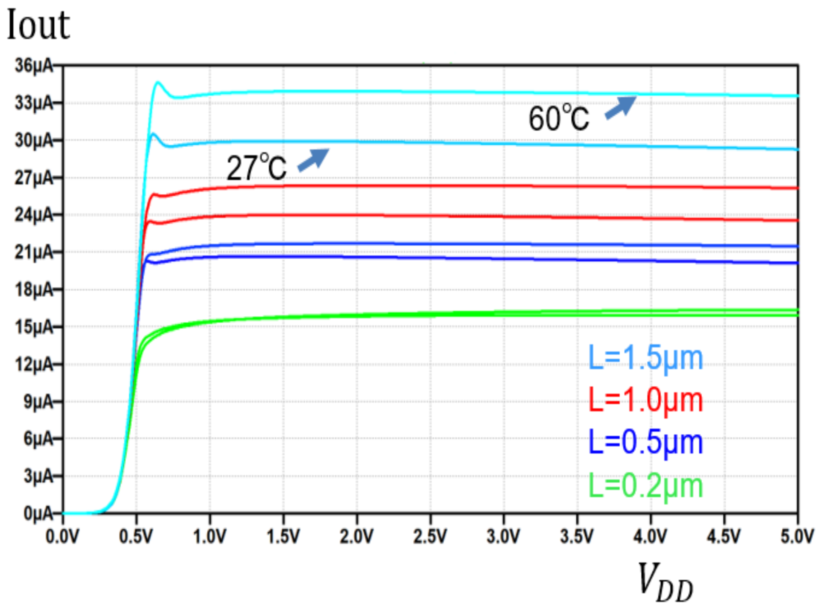




- In all cases, supply voltage and temperature insensitive
- IOUT → Inversely proportional to R1 value

Effects of MN1 Channel Length



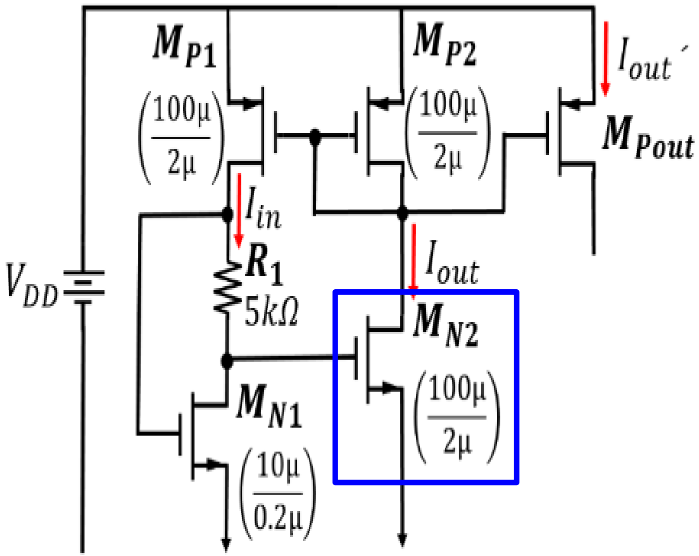


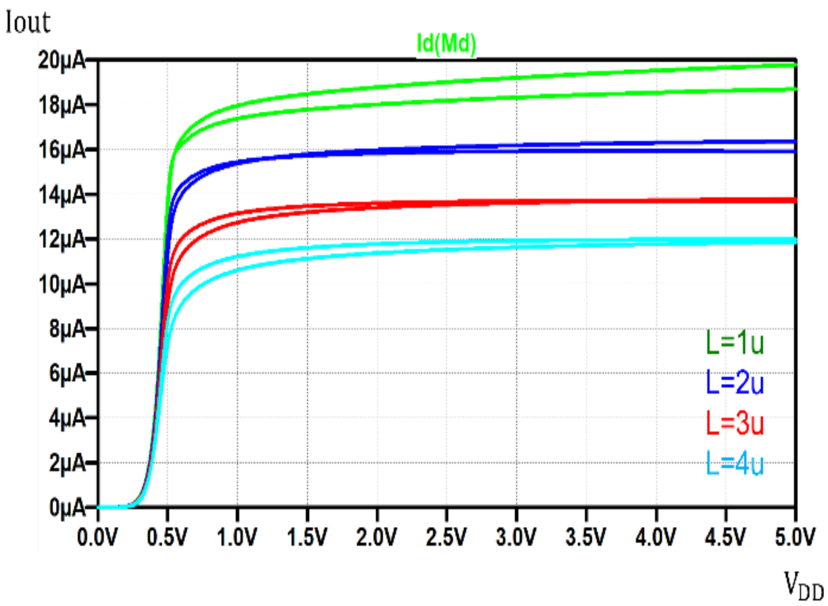
- In all cases. supply voltage insensitivity

- As MN1 channel length exceeds 0.2 µm,
  IOUT ⇒ increase
  ⇒ sensitive to temperature.

Reason: MN2 gate voltage increases

Effects of MN2 Channel Length





- In all cases, supply voltage insensitive
- Temperature insensitivity holds for L= 2μm, 3μm and 4μm
  ⇔ Sensitive as L decreases below 2μm

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Conclusion

Simple CMOS reference current sources

- Both NMOS and PMOS types
- Insensitive to supply voltage and temperature
- Multiple and single peaking current sources
- Self-biasing configuration
- No need for large input resistor
- Simple start-up circuit works well.
- Resistor temperature coefficients can be positive, zero or negative if a priori known.

Q&A

JEDAT® Japan EDA Technologies

Kobayashi Laboratory

群馬大学 GUNMA UNIVERSITY

Thank you very much