Generalized Leslie-Singh Architecture of 1st order Delta-Sigma AD Modulator with Different Resolutions of ADC and DAC

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OUTLINE

- Research Background and Objective
- Leslie-Singh Architecture 1st order ΔΣAD Modulator:
  - Circuit Configuration
  - STF and NTF
- Simulation Results:
  - Multi-bit ADC, Single-bit DAC
    - OSR-SQNDR
    - SQNDR@OSR= 2^5
  - Multi-bit ADC, Multi-bit DAC
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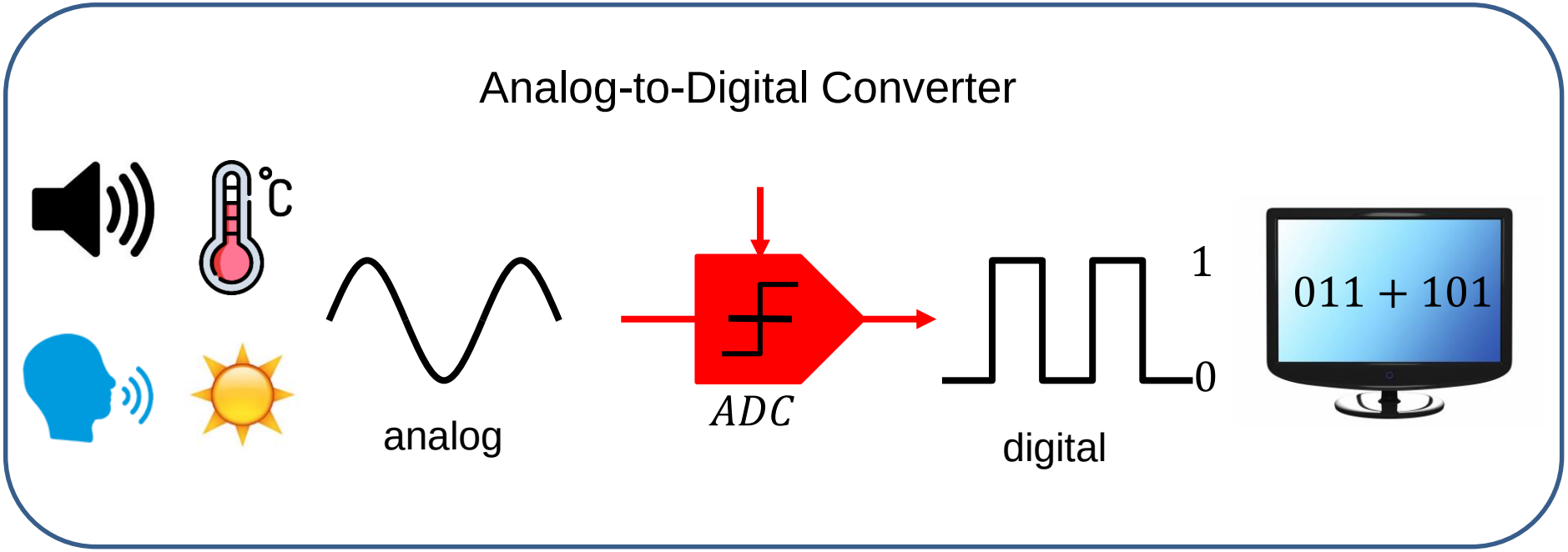
Research Background

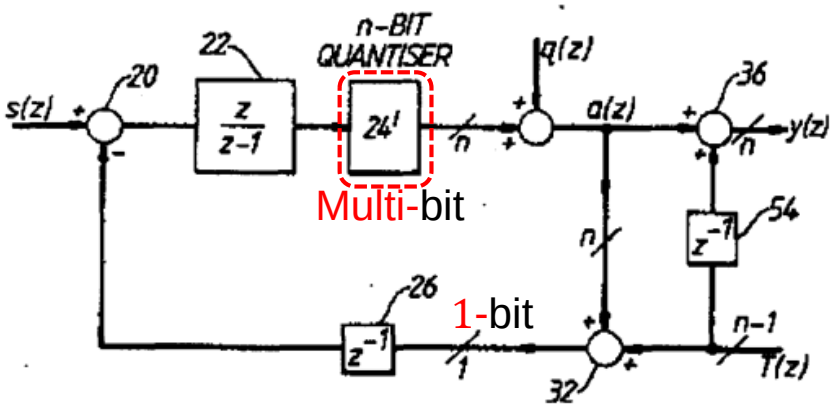


- Natural signals are analog signals
- Digital signals are suitable for signal processing

Analog-to-digital interface circuits are important

Research Background

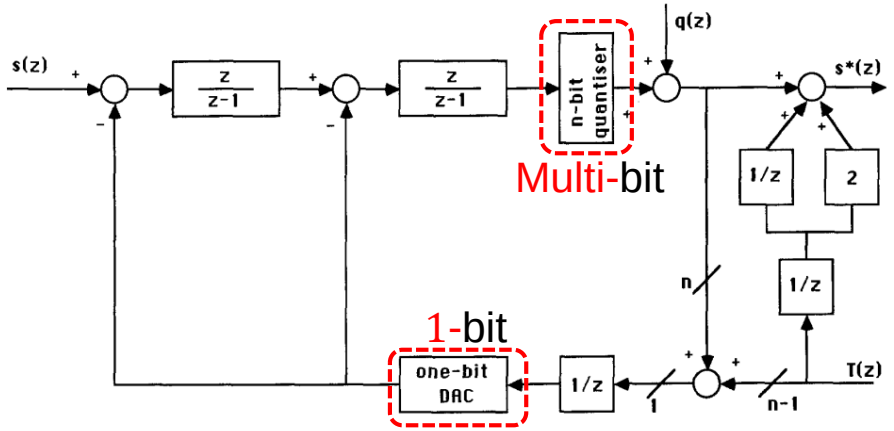
Yoshitome-Uchiyama ΔΣ AD modulator [1]



Both architectures use

- multi-bit ADC
- single-bit DAC

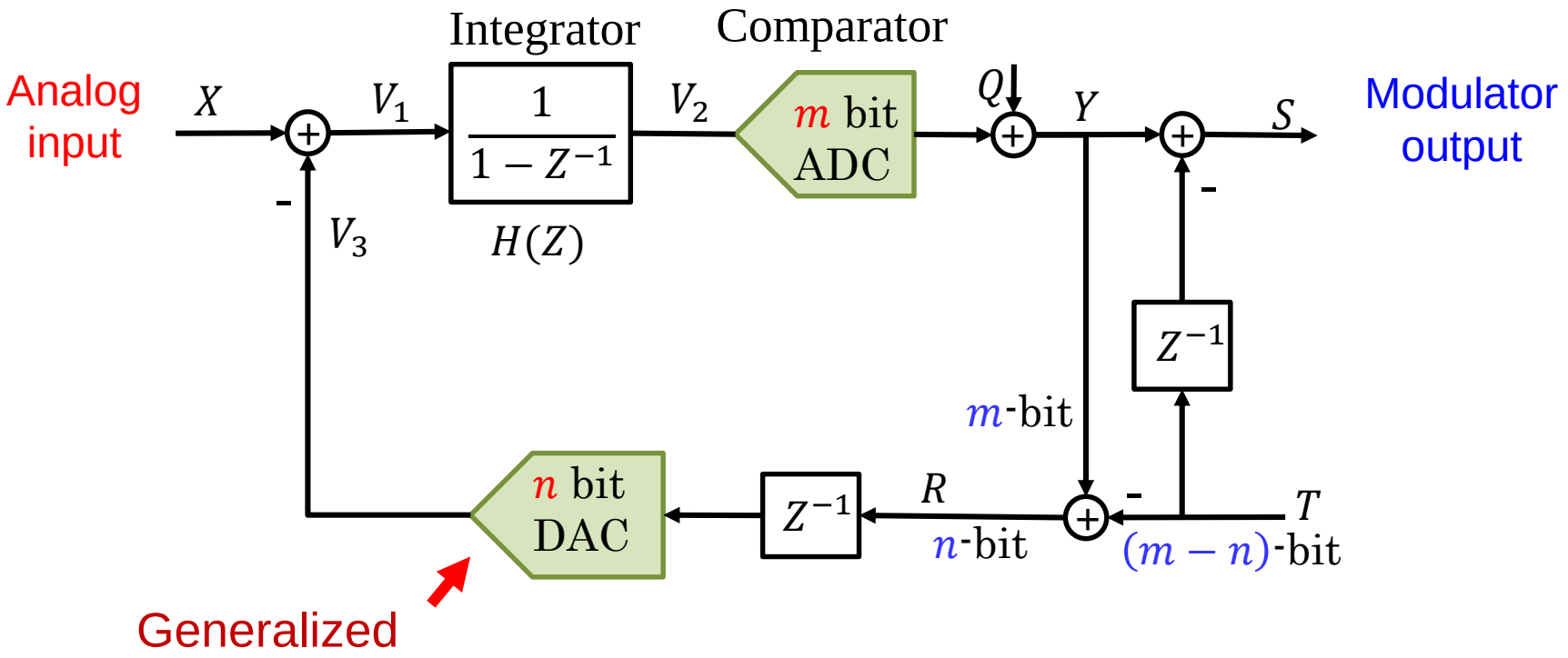
Leslie-Singh ΔΣ AD modulator [2]



[1] T. Yoshitome, K. Uchimura, "Quantization Noise Reduction in 1-bit Oversampling A-to-D Converter", *IEICE General Conference in Spring*, A-126, Mar. 1988

[2] T. C. Leslie, B. Singh, "An Improved Sigma-delta Modulator Architecture", ***IEEE*** *International Symposium on Circuit and Systems*, pp372-375, May 1990.

Objective



Objective

Investigate the improvement of SQNDR using various (m, n)

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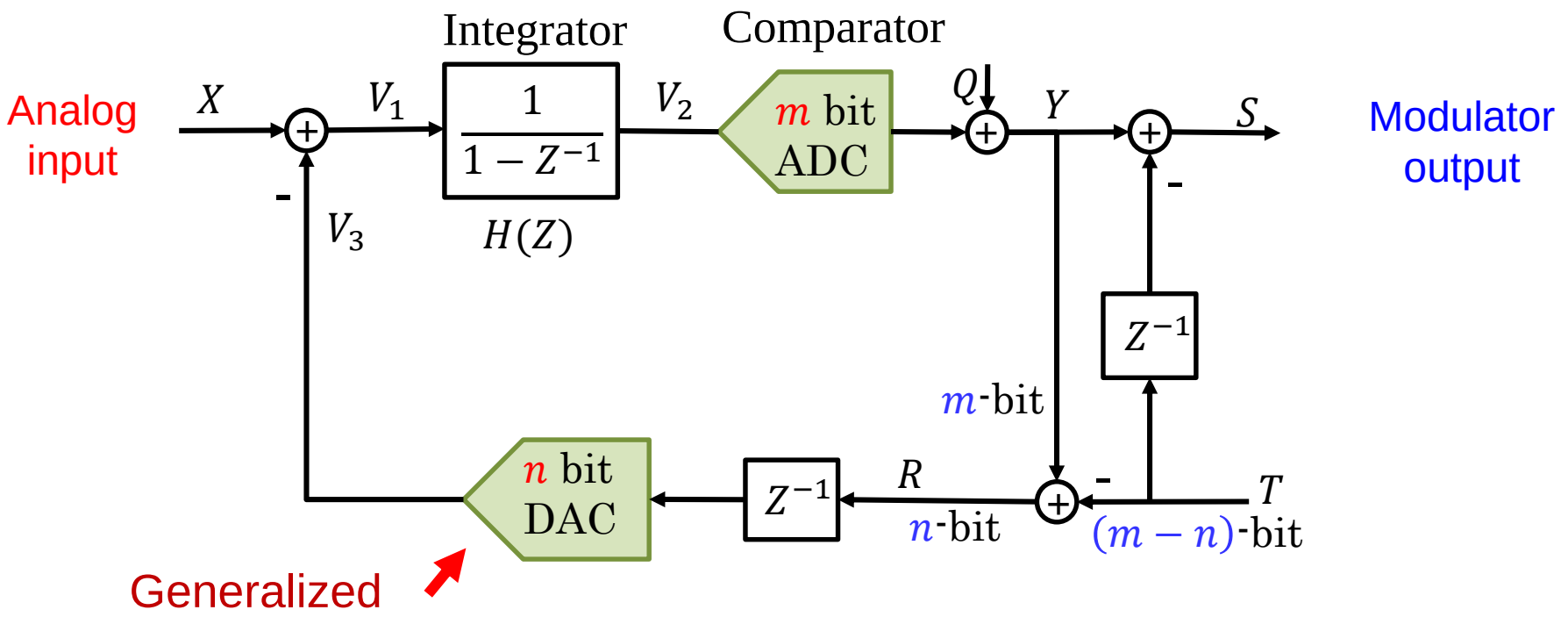
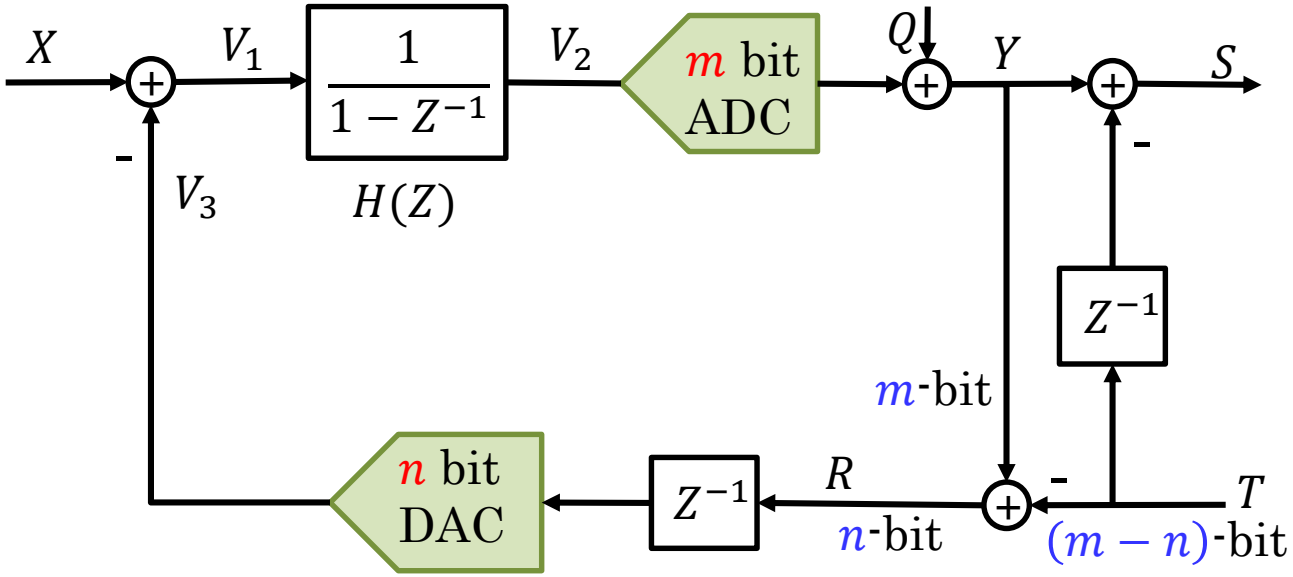
Circuit Configuration



- X(Z): Input signal
- Y(z): m-bit ADC output
- Q(Z): Quantization noise
- H(Z): Integrator
- S(Z): Modulator output
- R(Z): Upper n bits of Y(Z)
- T(z): Lower (m-n) bits of n-bit DAC

  Here, $T(Z) = Y(Z) - R(Z)$

STF, NTF



- m-bit ADC output:

$$Y(Z) = Q(Z) + V_2(Z)$$
$$= \frac{1}{1 - Z^{-1}}\{X(Z) - Z^{-1}[Y(Z) - T(Z)]\} + Q(Z)$$
$$\therefore Y(Z) = X(Z) + Z^{-1}\,T(Z) + (1 - Z^{-1})Q(Z)$$

- Modulator output:

$$S(Z) = Y(Z) - Z^{-1}T(Z)$$
$$\therefore S(Z) = 1 \cdot X(Z) + (1 - Z^{-1})Q(Z)$$

- Signal Transfer Function ($STF = 1$)
- Noise Transfer Function ($NTF = 1 - Z^{-1}$) ➡ 1st order noise shaped

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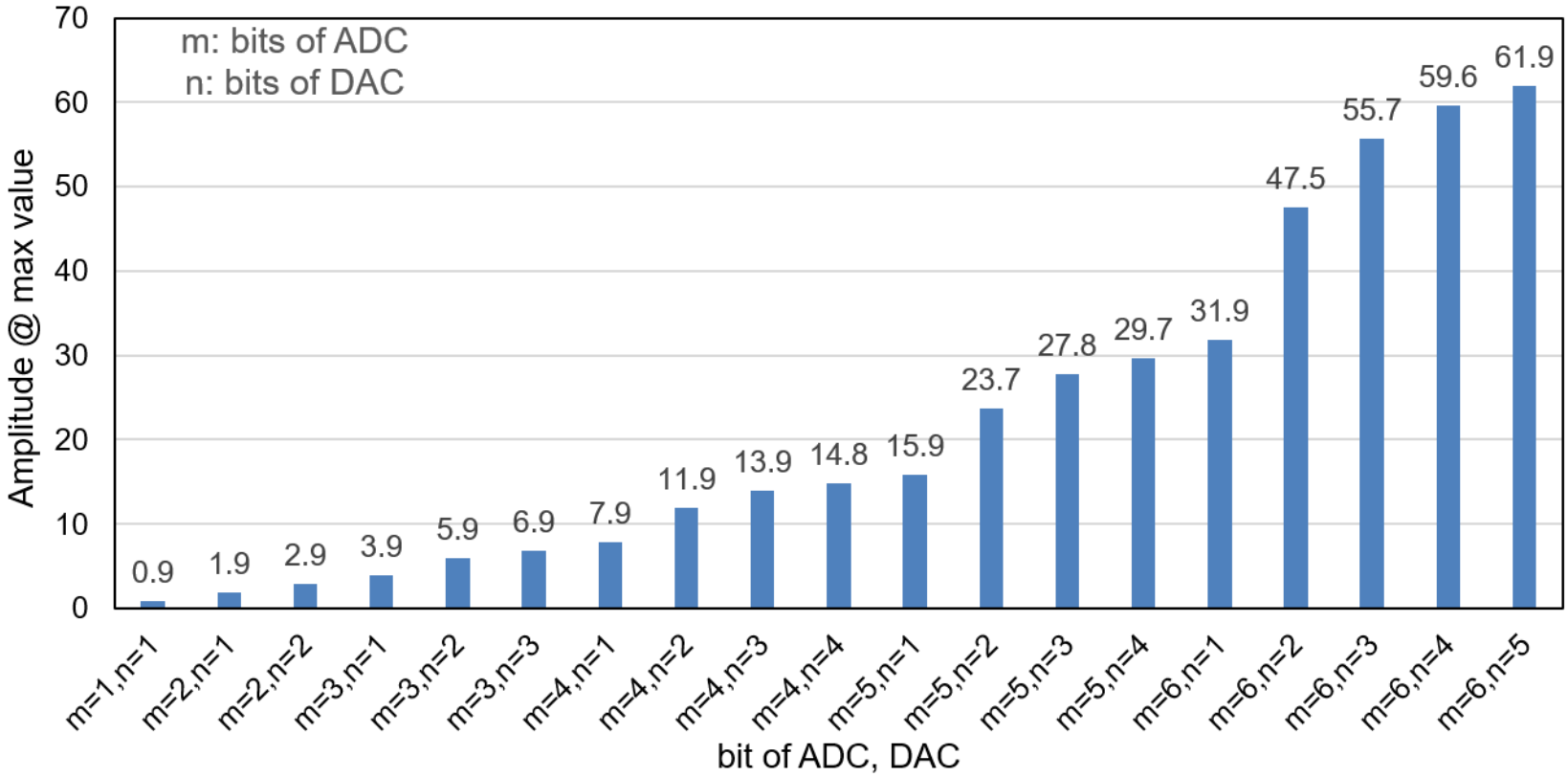
Simulation parameters

contents	Value
Input signal	Sine Wave
Input frequency	1
Sampling frequency	2^{20}
Data points	2^{20}



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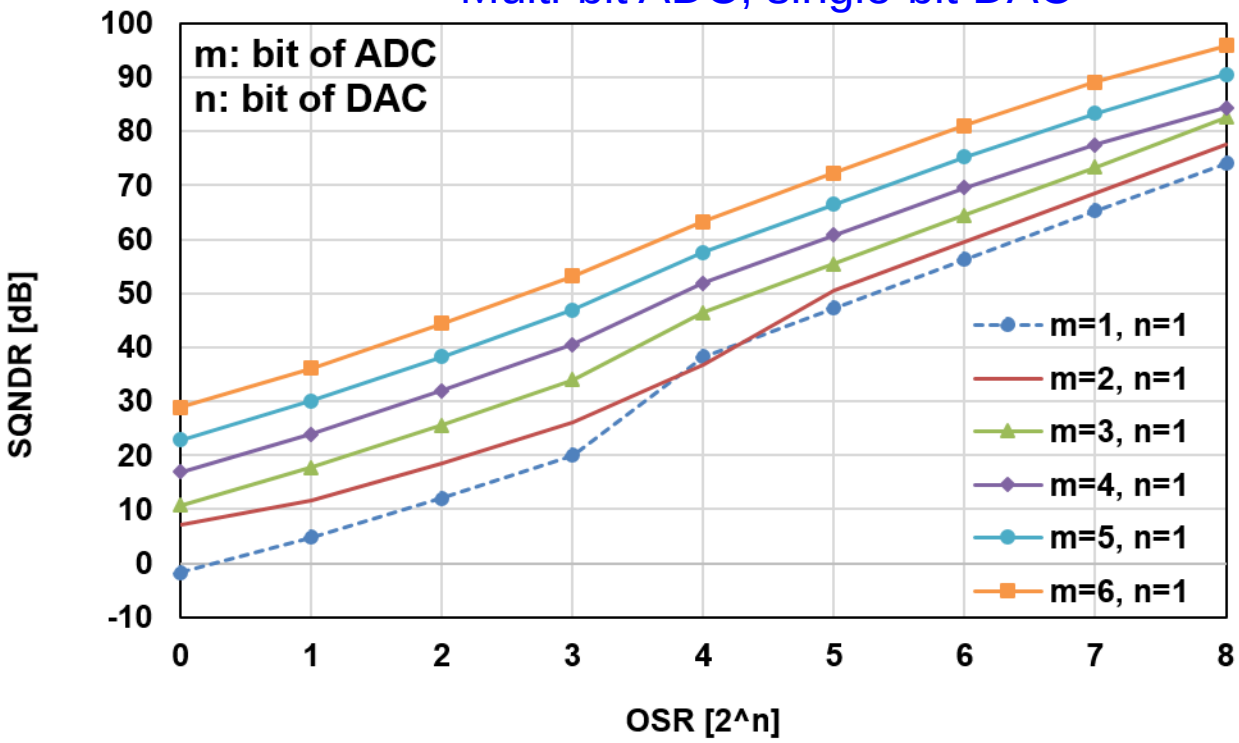
OSR-SQNDR

Multi-bit ADC, single-bit DAC



- Oversampling Ratio(OSR):

$$OSR = \frac{f_s}{2 \cdot B}$$

B: Input signal bandwidth
f_s: Sampling frequency

- Signal to [Quantization Noise + Distortion] Ratio(SQNDR):

$$SQNDR = 10\,log[\frac{Signal\ power}{\Sigma(Noise + distortion)\ power}]$$

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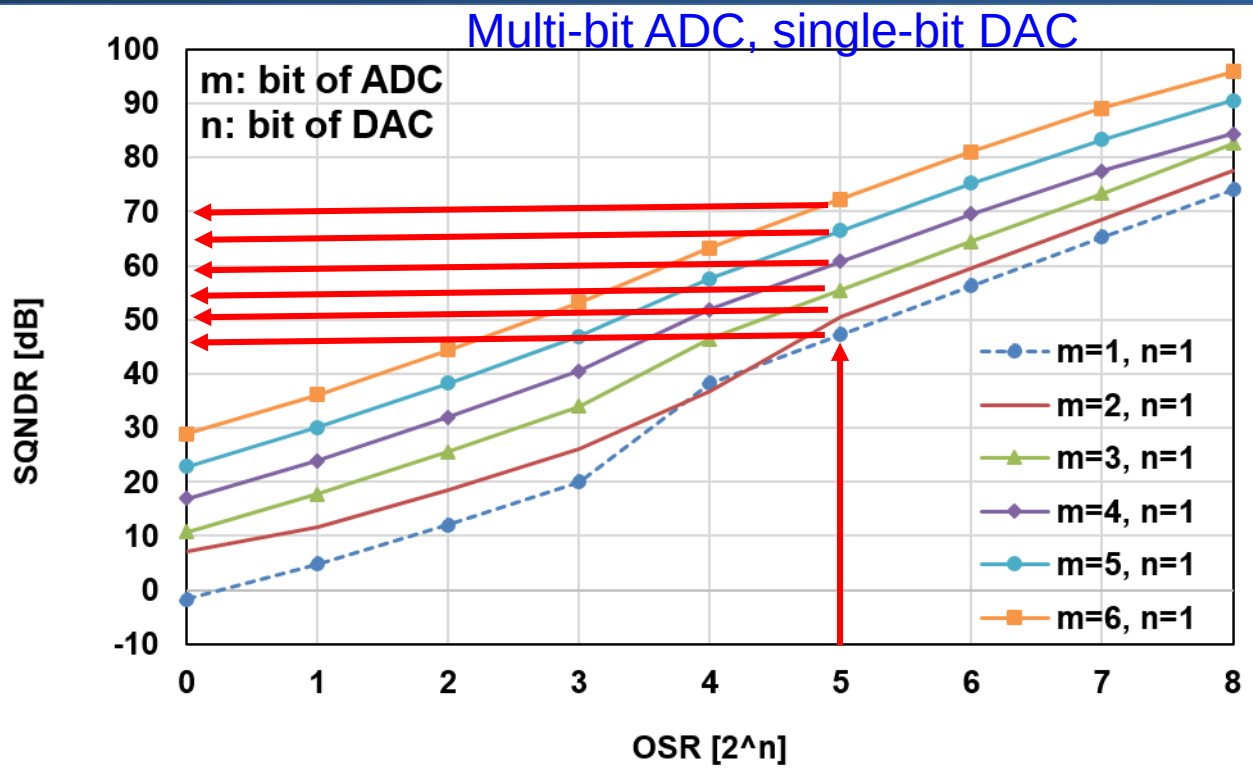
$SQNDR\ @\ OSR = 2^5$?



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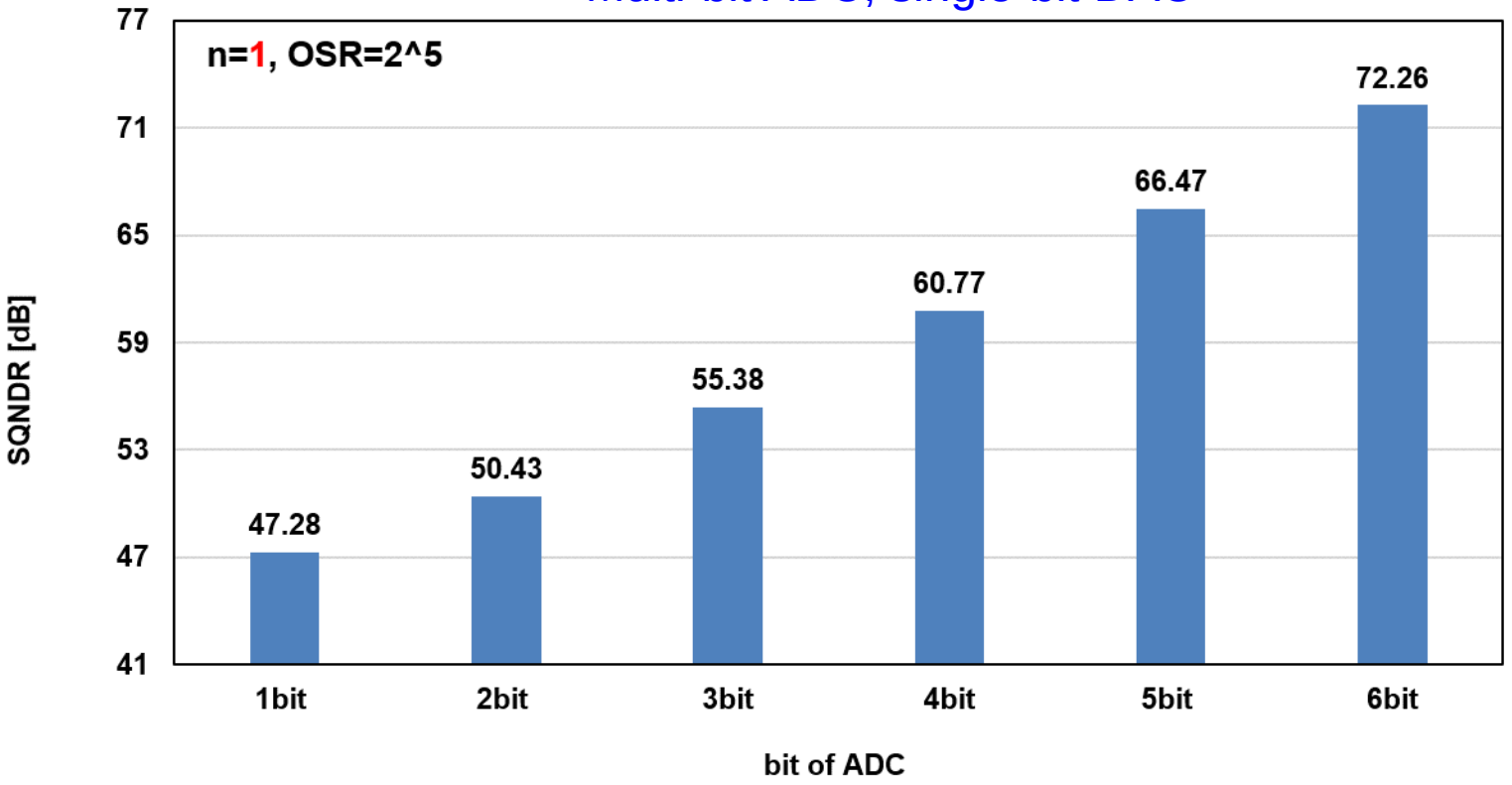
$SQNDR\ @\ OSR = 2^5$

Multi-bit ADC, single-bit DAC



For $m > 1$, every 1 bit of ADC increases

➡ $SQNDR \approx +6\ [dB]$

m: bits of ADC
n: bit of DAC

$$SQNDR = 6.02m + 1.76\ [dB]$$

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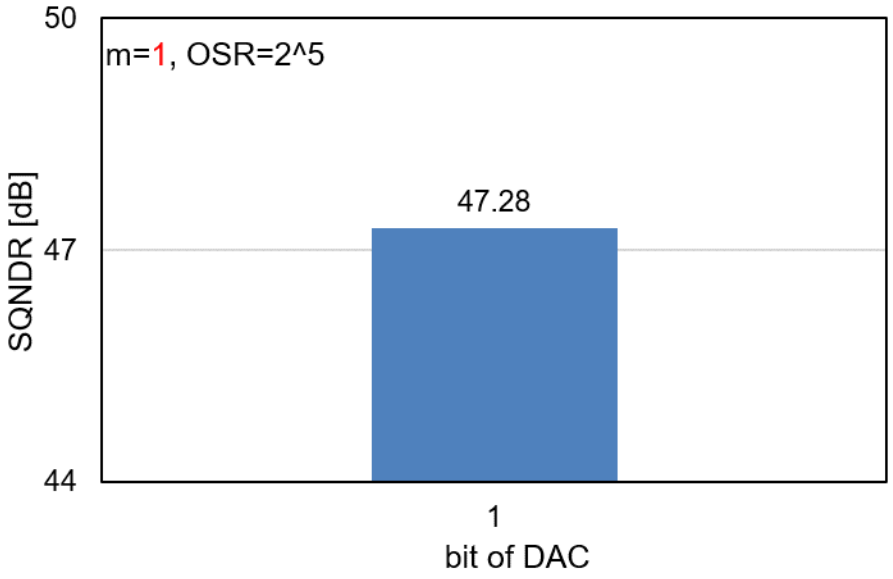
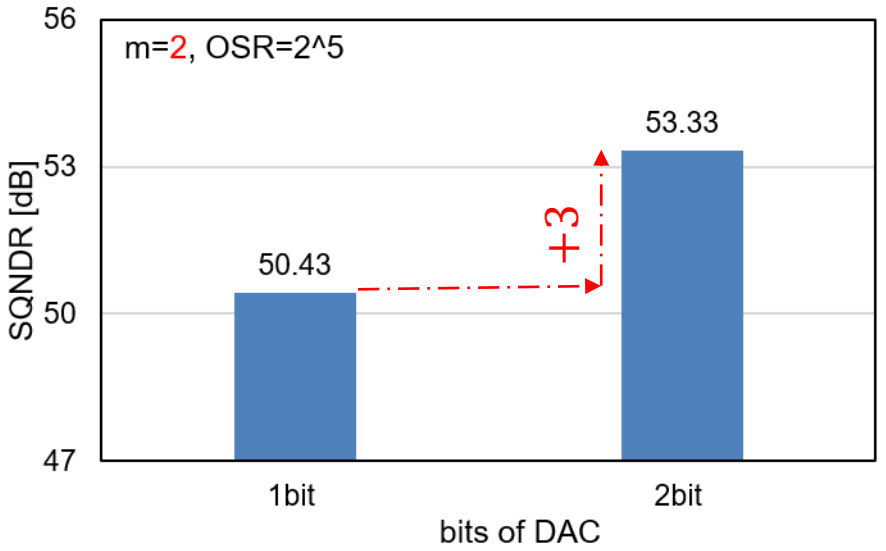
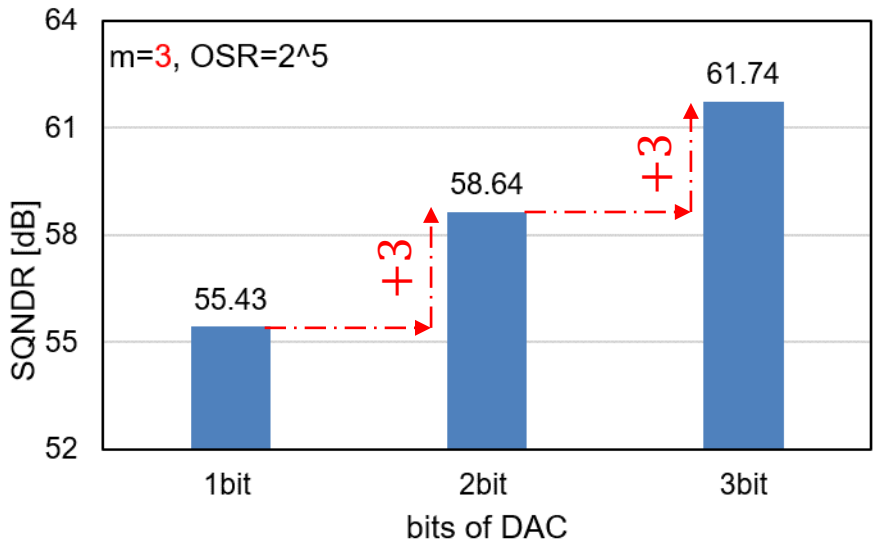
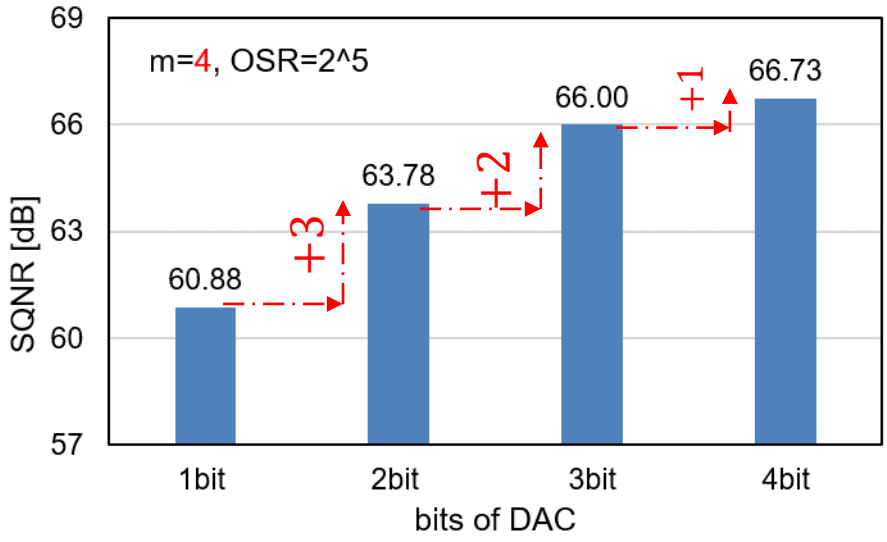
$SQNDR\ @\ OSR = 2^5$

Multi−bit ADC, multi−bit DAC



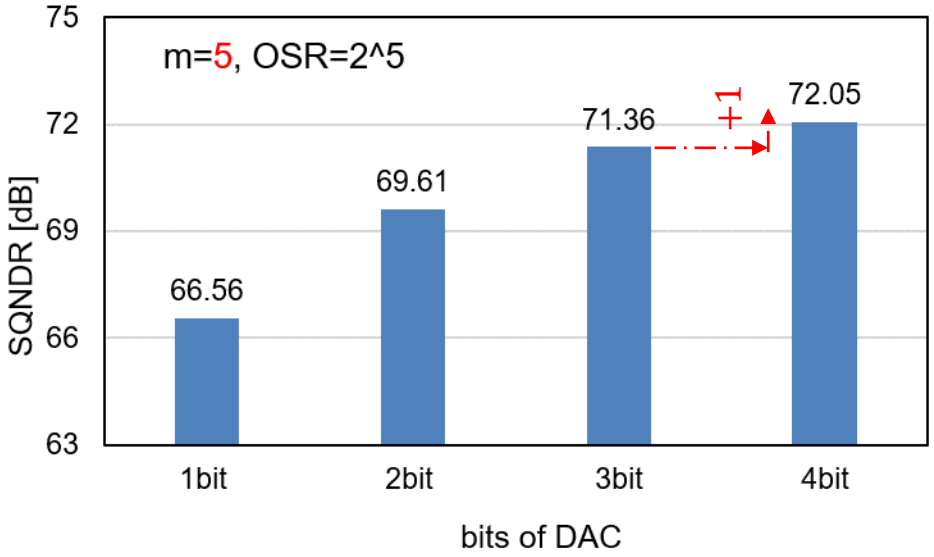


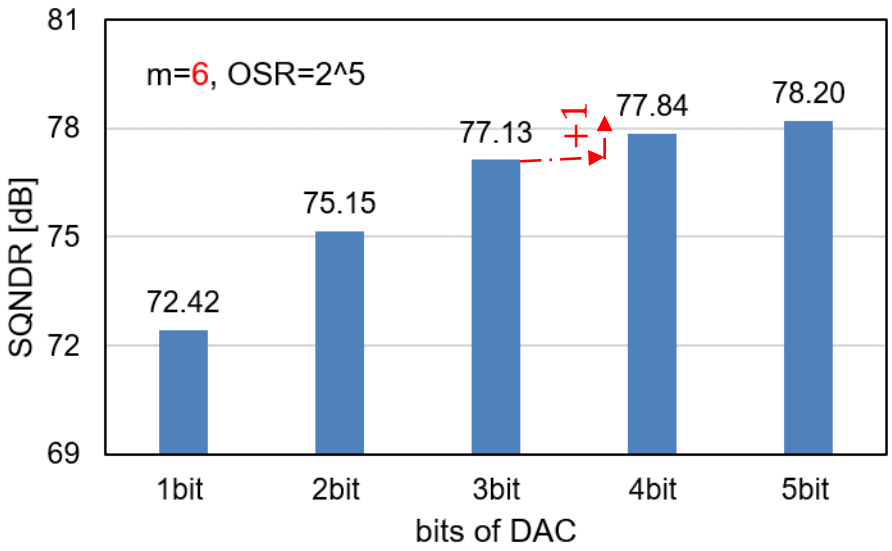




$SQNDR\ @\ OSR = 2^5$

Multi-bit ADC, multi-bit DAC





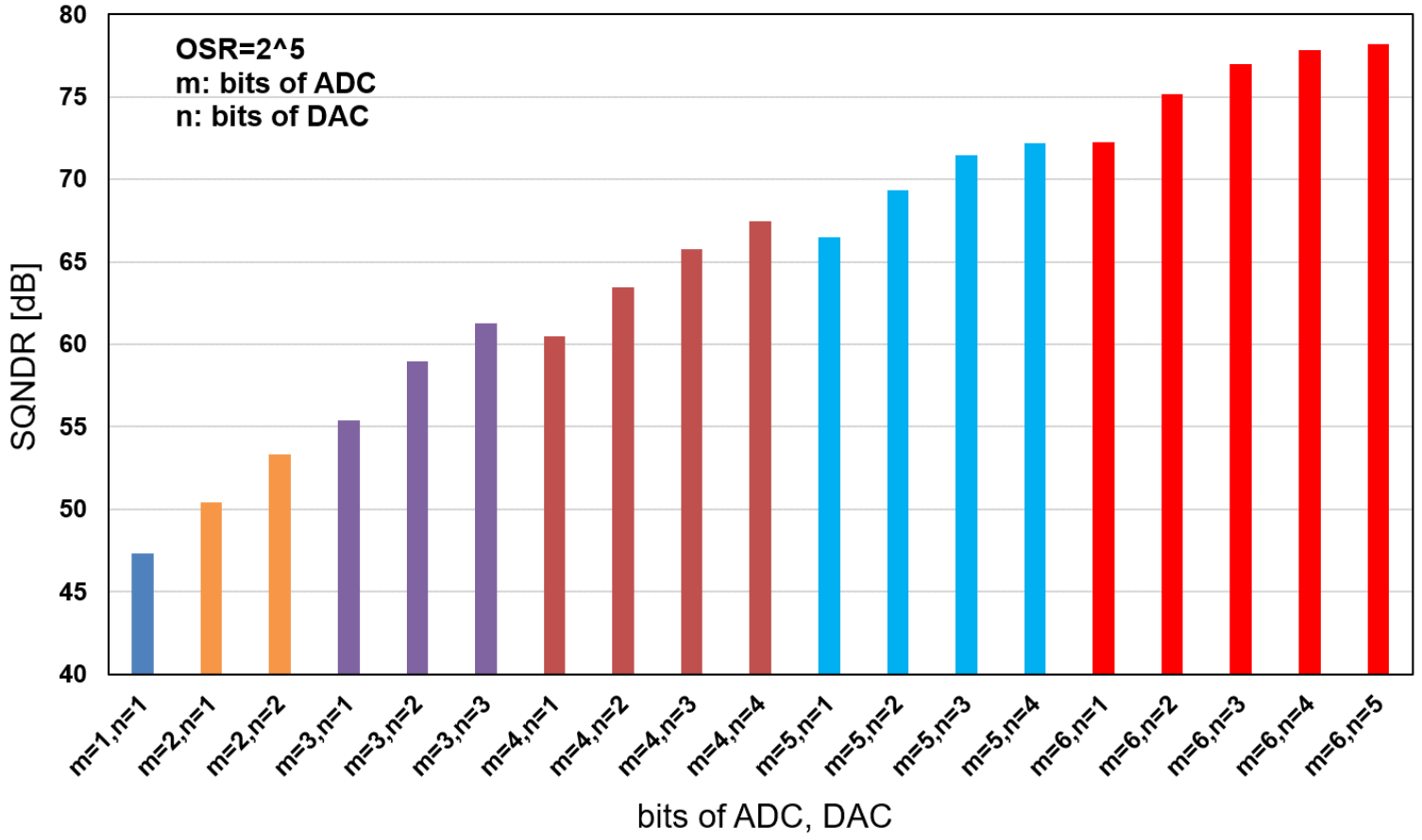
- For $n = 1{\sim}3$, every 1 bit of DAC increases:
  - ➡ $SQNDR \approx +3\ [dB]$
- For $n > 3$, every 1 bit of DAC increases:
  - ➡ $SQNDR < +3\ [dB]$

m: bits of ADC
n: bit of DAC

➡ 3-bit DAC may suffice in 6-bit ADC usage case

Summarized simulation results

$SQNDR\ @\ OSR = 2^5$ using various (m, n)



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Conclusion

- ADC: for every 1-bit increases
  - $m > 2, SQNDR \approx +6[dB]$
- DAC: for every 1-bit increases
  - $n = 1\sim3, SQNDR \approx +3[dB]$
  - $n > 3, SQNDR < +3[dB]$
  - $n = 3$ is suitable for the 6-bit ADC

➢Future works:

Study on generalized Leslie-Singh 2nd order ΔΣ AD Modulator

Thank you very much

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Q&A

Q : Have you considered with the imperfection of the multi-bit DAC, for example nonlinearity and so on ?

A : No, I am not considering the DAC nonlinearity. My research focuses on the ideal DAC case.