# Revival of Asynchronous SAR ADC based on Hopfield Network

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# Contents

- Research Objective and Background

- Binary asynchronous SAR ADC

- Non-binary asynchronous SAR ADC

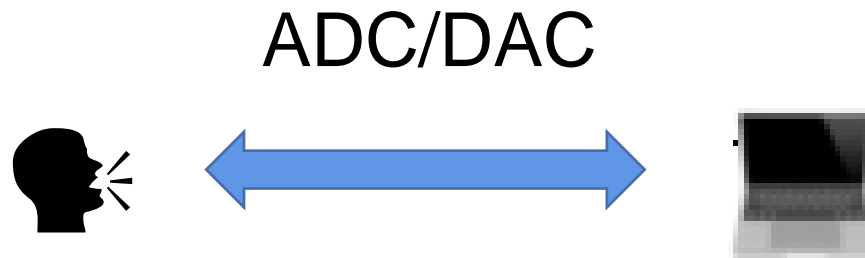- Hopfield network and DAC

- Conclusion

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- <u>Research Objective and Background</u>

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# Value of ADC DAC Research

- Analog signals are everywhere

- Digital signals are useful for computer processing

ADC/DAC

Analog-digital interface circuits are important.

# Hopfield neural net ADC

- Traditional Hopfield neural network ADC.



- Elements of "interest" are used

  as ADC design with realistic competitiveness.

Prof. John Joseph Hopfield
California Institute of Tech.
Princeton University

- Local minima problem

  - Sometimes wrong output



- Revisit because of

  - Very fast SAR ADC

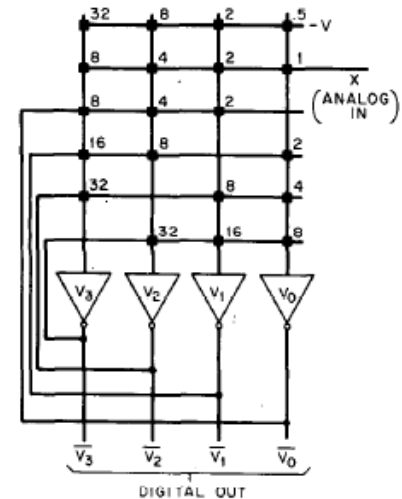  - Non-binary SAR ADC as well as binary

  - Simple design

Fig. 2. The 4-bit A/D converter computational network. The analog input voltage is $x$, while the complement of the digital word $V_3 V_2 V_1 V_0$ which is computed to be the binary value of $x$ is read out as the 0 or 1 values of the amplifier output voltages.

# Research Objective

Improvement of Hopfield neural network ADC

- Discard feedback from lower bits

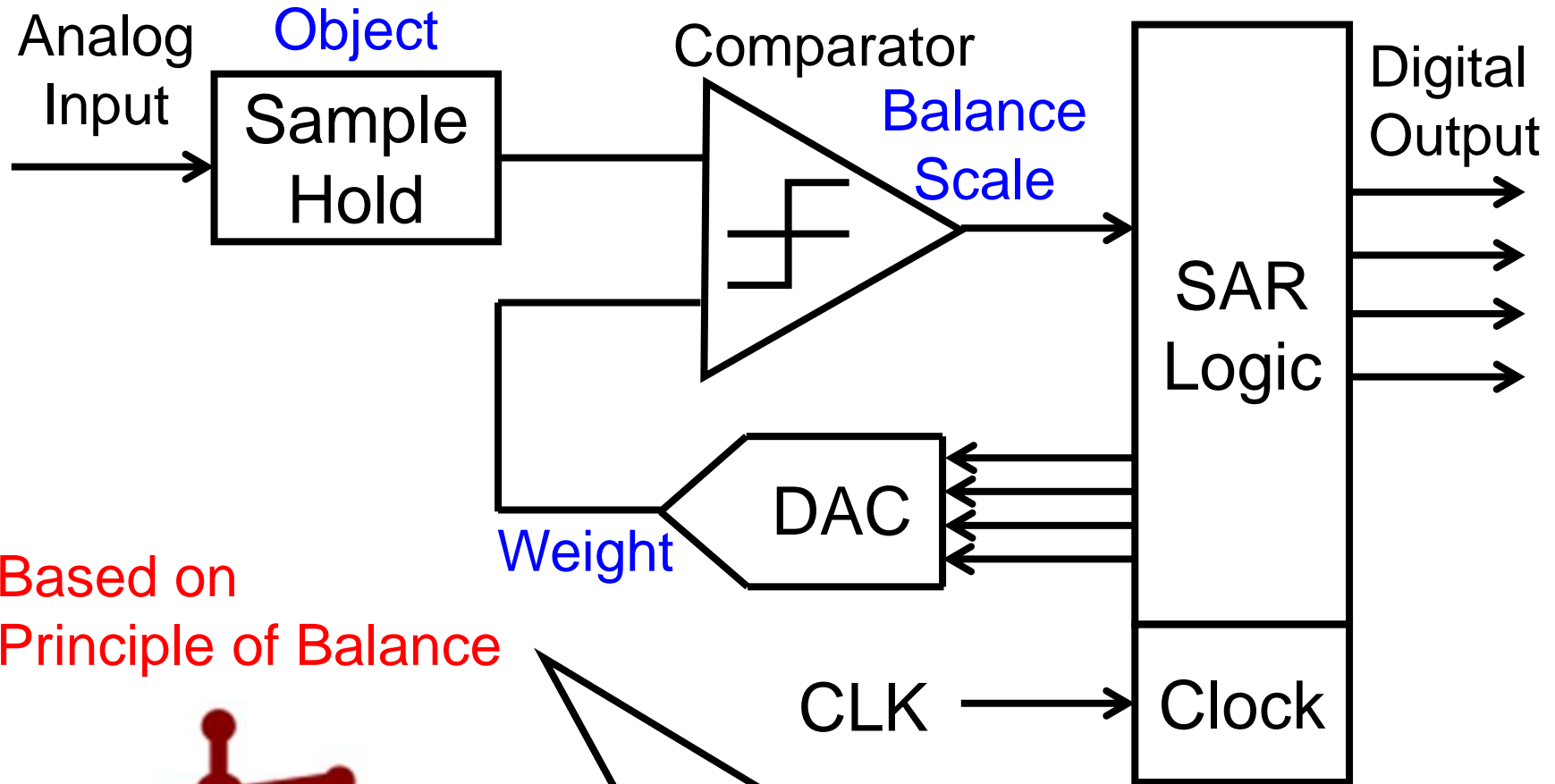- All feed-forward configuration

- No local minima

    - Always correct output

- Realization of asynchronous SAR ADC

    - Very fast

    - No high frequency clock required

    - Small hardware

- Proposal of Non-binary asynchronous SAR ADC

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# Binary Weighted SAR ADC

Analog Input

Object

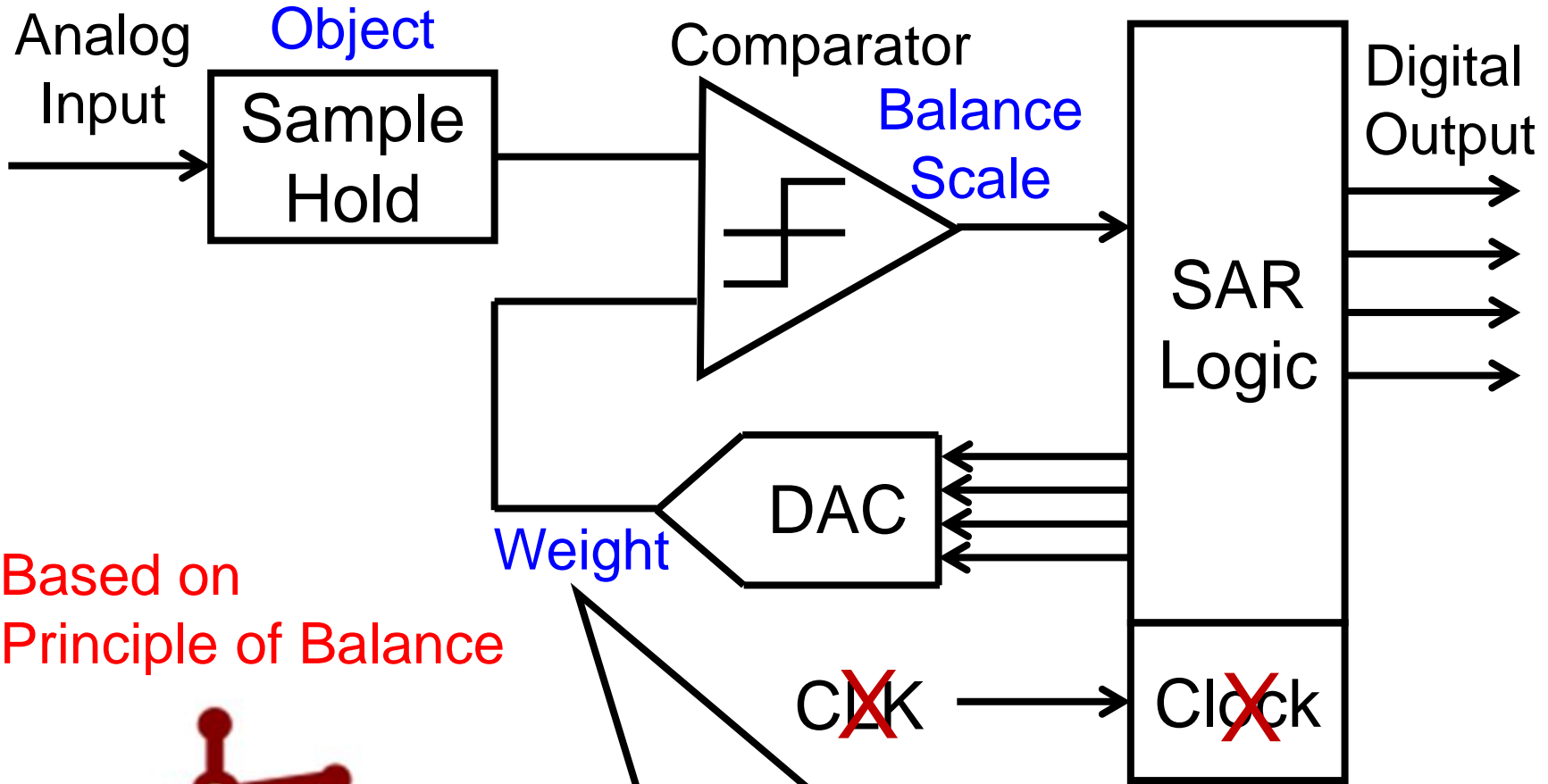Sample Hold

Comparator

Balance Scale

SAR Logic

Digital Output

DAC

Weight

CLK

Clock

Based on Principle of Balance

Synchronous

Binary weight (1, 2, 4, 8, 16, 32, 64…)

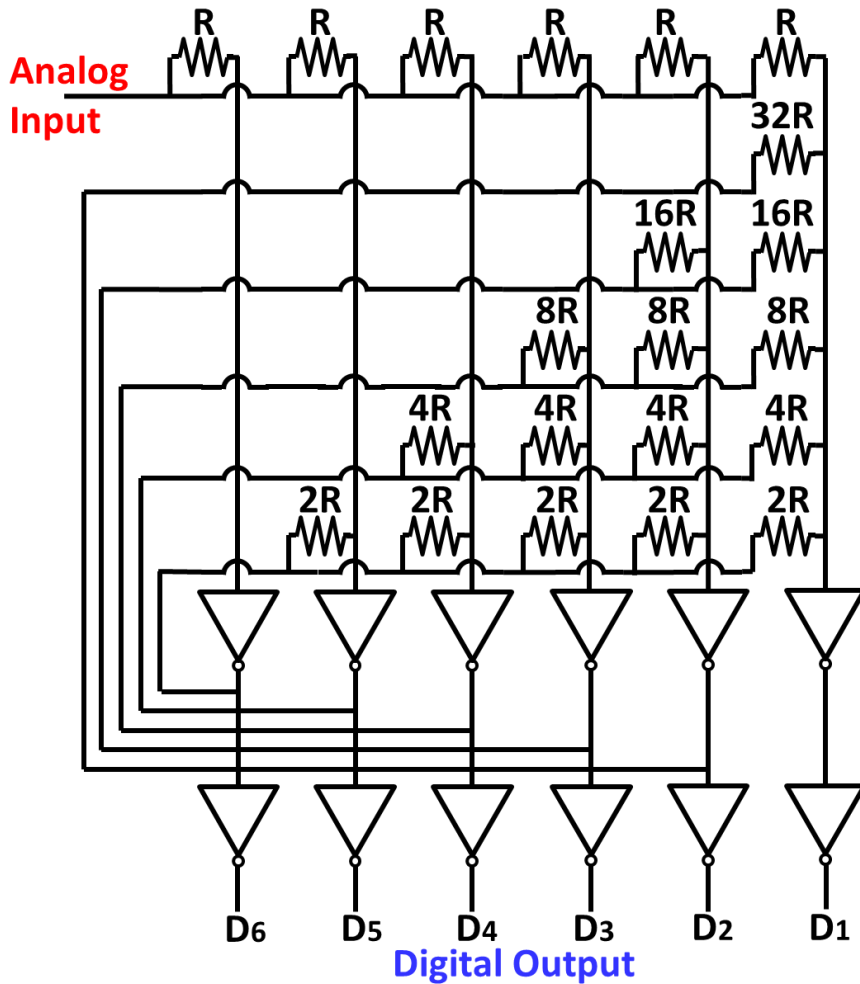# **Asynchronous Binary Weighted SAR ADC**

# Investigated Network

6-bit SAR ADC case



**Improvement of Hopfield neural network ADC**

**- Discard feedback from lower bits**

**- All feed-forward configuration**

**- No local minima**

**Asynchronous SAR ADC**

**- Very fast**

**- No high frequency clock**

**- Small hardware**

Analog Input

Digital Output

$D_6$ $D_5$ $D_4$ $D_3$ $D_2$ $D_1$

# Correspondence Table

## 10-bit binary weighted SAR ADC

| Step | 1st | 2nd | 3rd | 4th | 5th | 6th | 7th | 8th | 9th | 10th | output |
|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|--------|
| Weight | 516 | 256 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | |

Decimal digital output :

Data = $(1/R)\ D_{10} + (1/R_9)\ D_9 + (1/R_8)D_8 + (1/R_7)D_7 + (1/R_6)D_6$

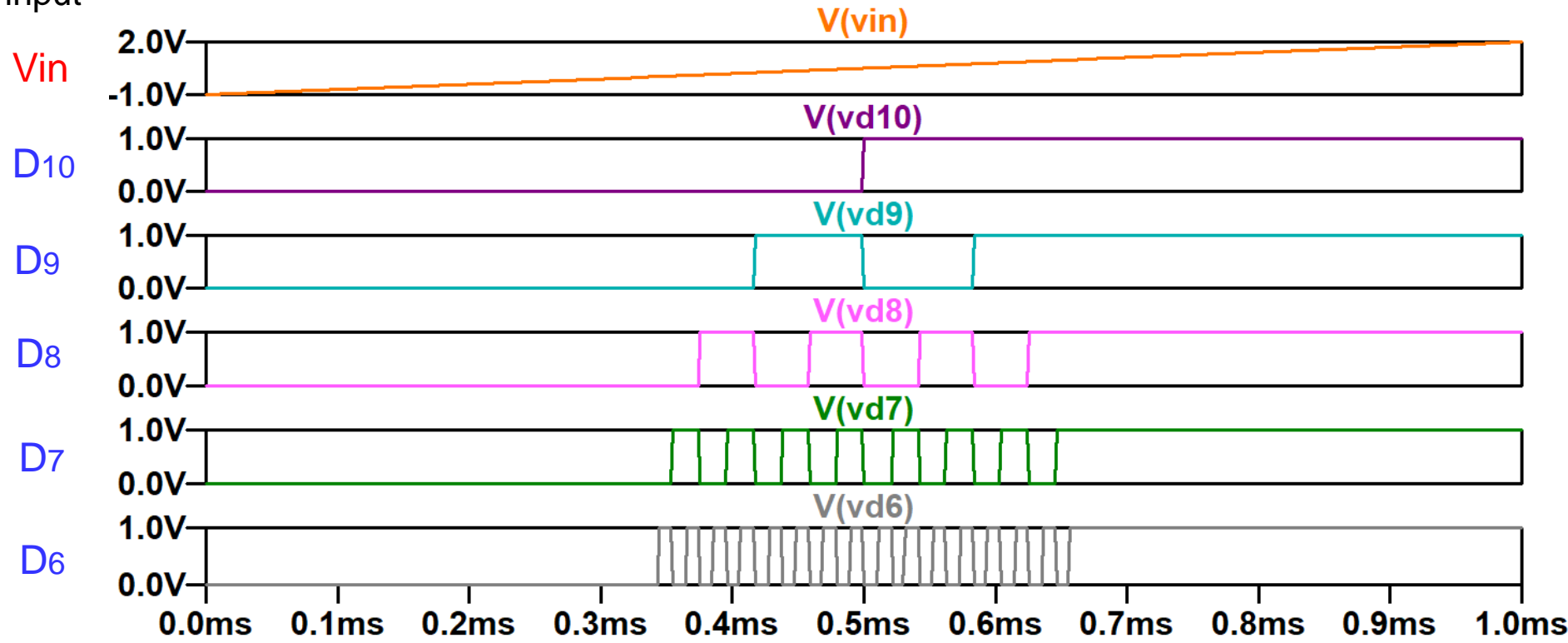$\qquad + (1/R_5)D_5 + (1/R_4)D_4 + (1/R_3)D_3 + (1/R_2)D_2 + (1/R_1)D_1$

Here
$1/R = 512, \ 1/R_9 = 256, \ 1/R_8 = 128, \ 1/R_7 = 64, \ 1/R_6 = 32$
$1/R_5 = 16, \ \ 1/R_4 = 8, \ \ \ \ 1/R_3 = 4, \ \ \ \ 1/R_2 = 2, \ \ 1/R_1 = 1$
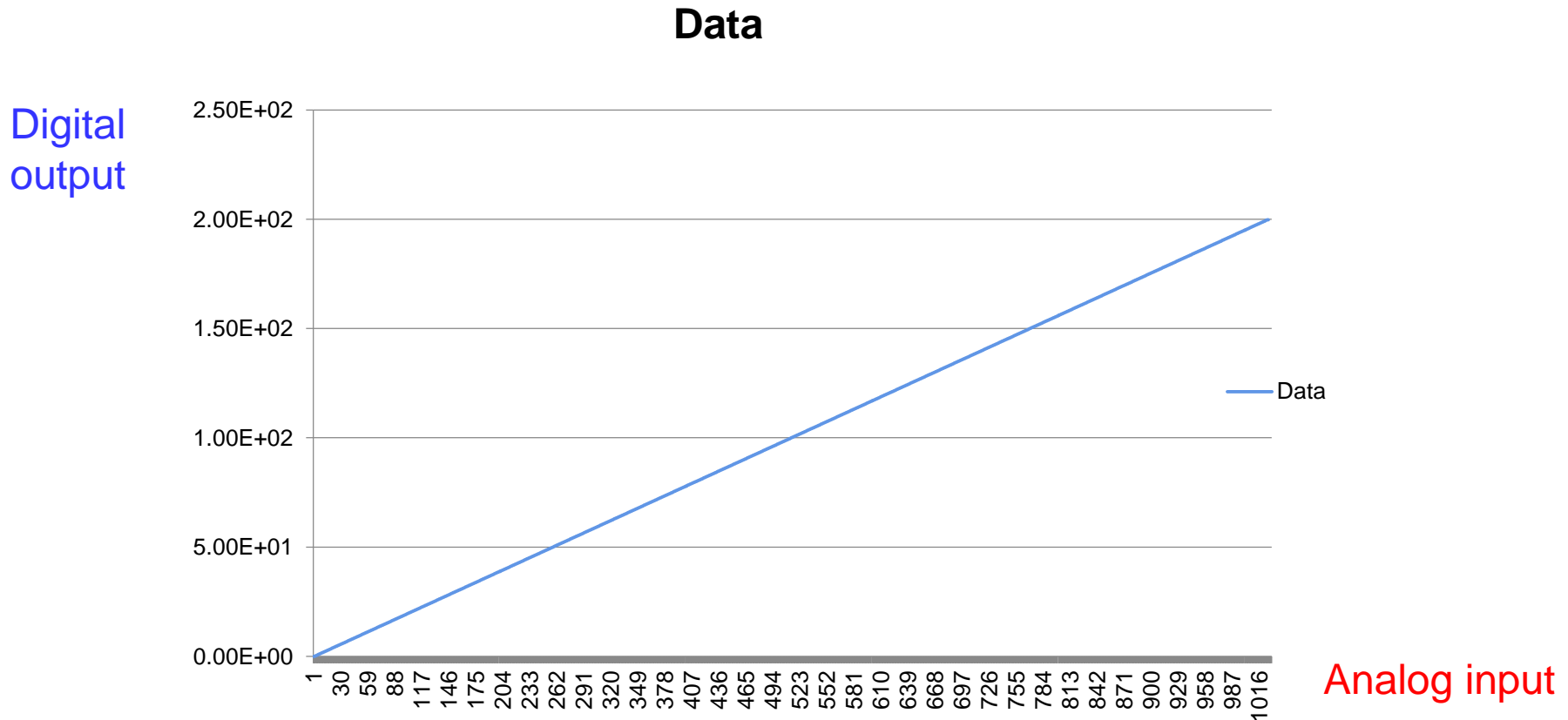
Binary weighted

# SPICE Simulation Result

## 10-bit asynchronous binary-weighted SAR ADC
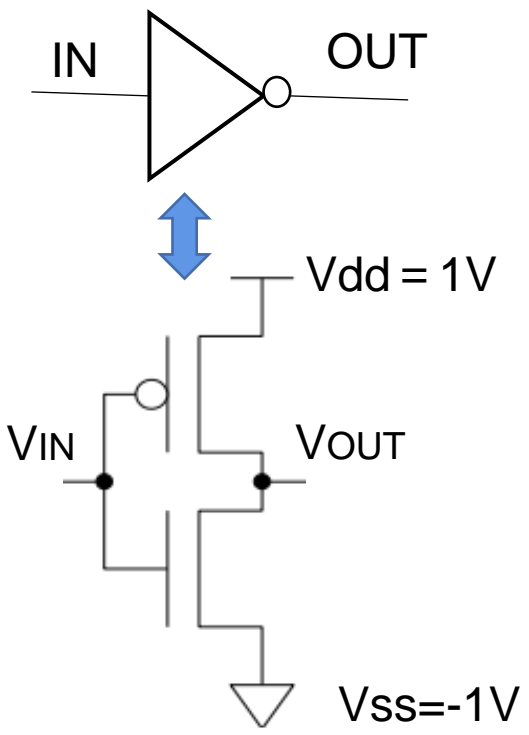## with improved Hopfield network

# Decimal Data Calculation

$$\text{Data} = (1/R)\, D_{10} + (1/R_9)\, D_9 + (1/R_8)D_8 + (1/R_7)D_7 + (1/R_6)D_6$$
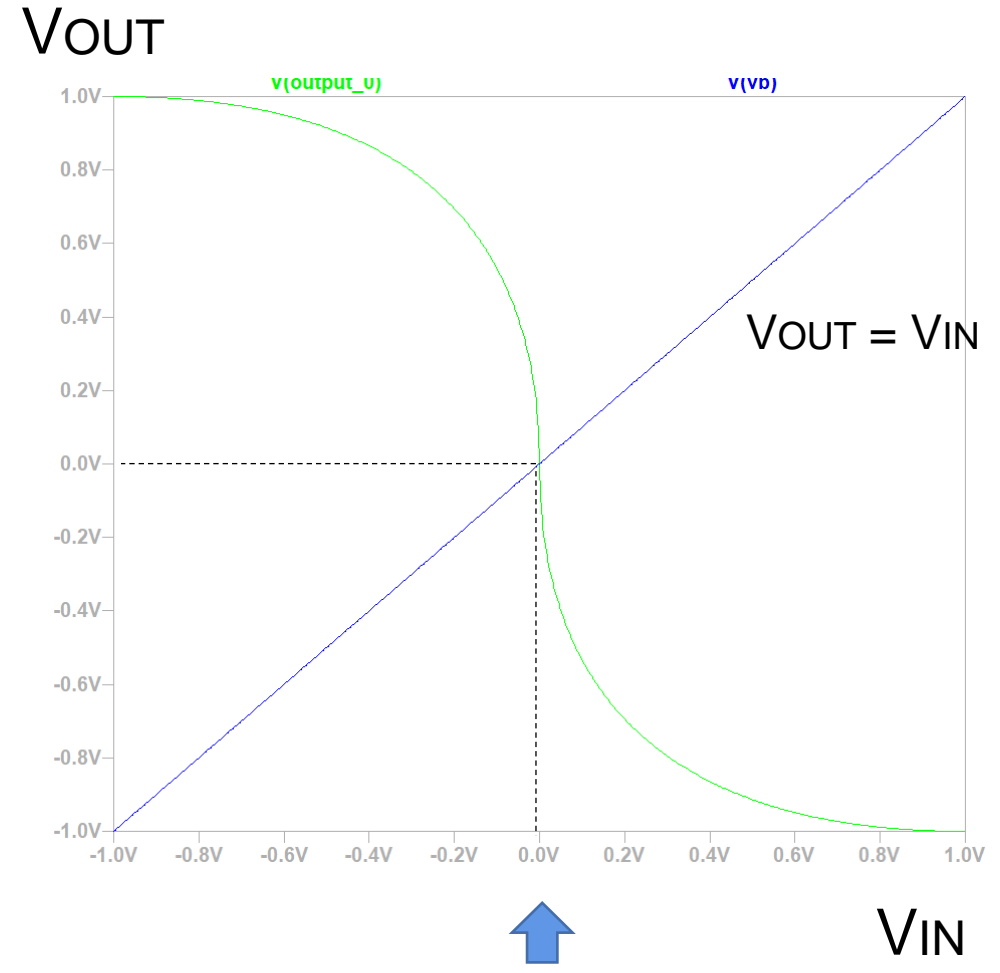$$+ (1/R_5)D_5 + (1/R_4)D_4 + (1/R_3)D_3 + (1/R_2)D_2 + (1/R_1)D_1$$

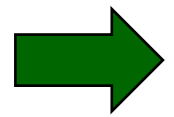**Data**

Digital output

Analog input



- Operation has been confirmed.
- Amazingly simple design can realize a 10-bit SAR ADC

# CMOS inverter



CMOS inverter threshold voltage

⇒ Affected by PVT variation

⇒ ADC nonlinearity

# Application

Asynchronous SAR ADC with Hopfield network
Advantage: High speed, small chip area
Disadvantage: ADC nonlinearity
  due to resistors mismatch, inverter threshold voltage variation

Proposed killer application
  Usage inside multi-bit $\Delta\Sigma$ ADC

  Currently, 3-bit flash ADC is used.

  More than 6-bit Hopfield asynchronous SAR ADC can be used.
  Its nonlinearity is noise-shaped inside the modulator.



Extended Leslie-Singh
Architecture

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# Fibonacci Number

## Definition (n=0,1,2,3…)

$$F_0 = 0$$
$$F_1 = 1$$
$$F_{n+2} = F_n + F_{n+1}$$

**Example of numbers(Fibonacci number)**
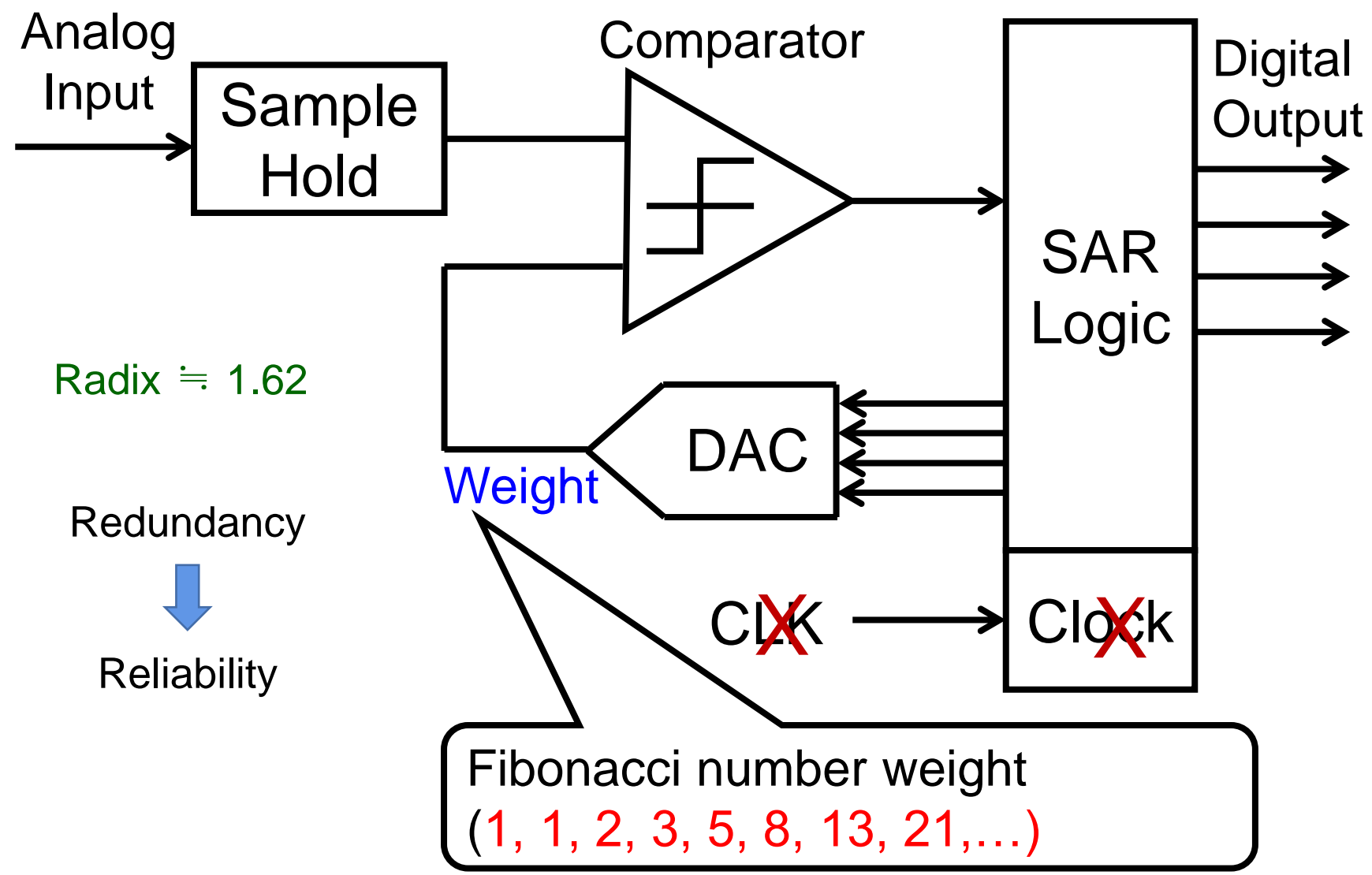
0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89…

**Leonardo Fibonacci (around 1170-1250)**

## Property
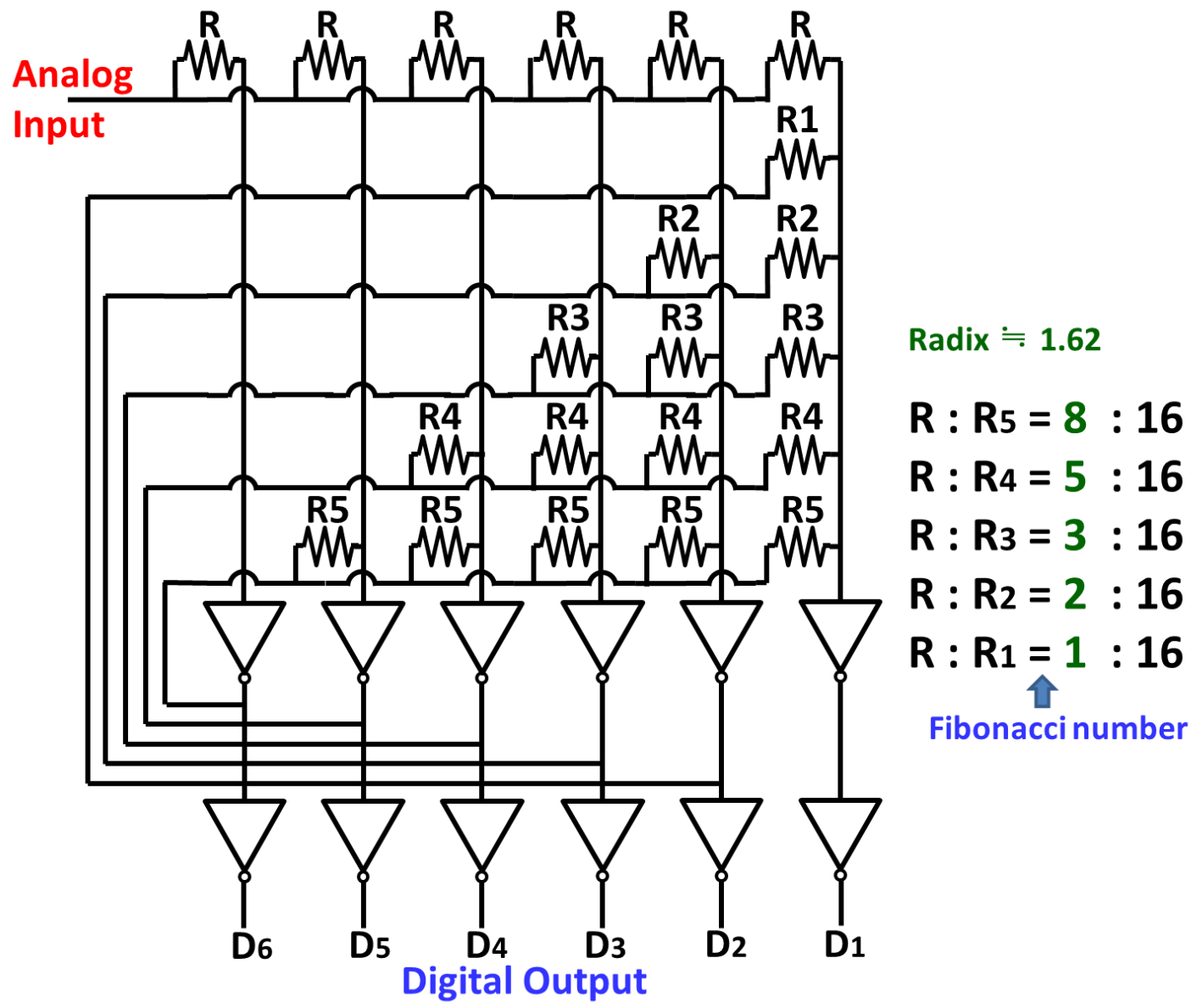
**The closest terms ratio converges to *"Golden Ratio"* !**

$$\lim_{n \to \infty} \frac{F_n}{F_{n-1}} = 1.618033988749895 = \varphi$$

# Fibonacci number weighted SAR ADC

Analog Input

Sample Hold

Comparator

SAR Logic

Digital Output

Radix ≒ 1.62

Redundancy

⬇

Reliability

Weight

DAC

CLK

Clock

Fibonacci number weight
(1, 1, 2, 3, 5, 8, 13, 21,…)

[1] Y. Kobayashi, H. Kobayashi, et. al.,"SAR ADC Design
   Using Golden Ratio Weight Algorithm," ISCIT (Oct. 2015)

# Fibonacci number weighted SAR ADC



Radix ≒ 1.62

R : $R_5$ = **8** : 16

R : $R_4$ = **5** : 16

R : $R_3$ = **3** : 16

R : $R_2$ = **2** : 16

R : $R_1$ = **1** : 16

Fibonacci number

Analog Input

Digital Output

# Correspondence Table

## 10-bit Fibonacci weighted SAR ADC

| Step | 1st | 2nd | 3rd | 4th | 5th | 6th | 7th | 8th | 9th | 10th | output |
|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|--------|
| Weight | 89 | 55 | 34 | 21 | 13 | 8 | 5 | 3 | 2 | 1 | |

Decimal digital output :

$$Data = (1/R) D_{10} + (1/R_9) D_9 + (1/R_8)D_8 + (1/R_7)D_7 + (1/R_6)D_6$$

$$+ (1/R_5)D_5 + (1/R_4)D_4 + (1/R_3)D_3 + (1/R_2)D_2 + (1/R_1)D_1$$

Here

$1/R = 89$,  $1/R_9 = 55$, $1/R_8 = 34$, $1/R_7 = 21$, $1/R_6 = 13$  Fibonacci number
$1/R_5 = 8$,  $1/R_4 = 5$,  $1/R_3 = 3$,  $1/R_2 = 2$,  $1/R_1 = 1$  weighted
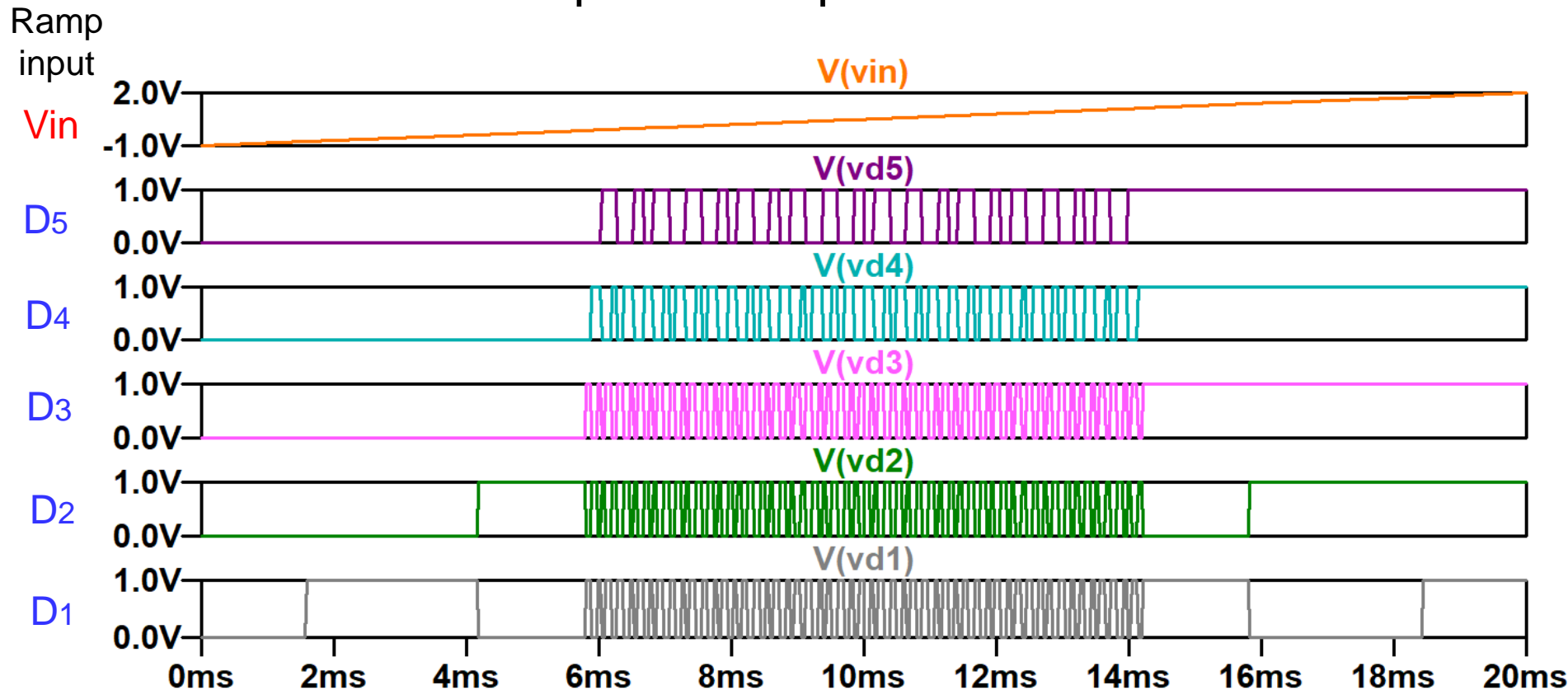
# SPICE Simulation Result

## 10-bit asynchronous Fibonacci number weighted SAR ADC with improved Hopfield network
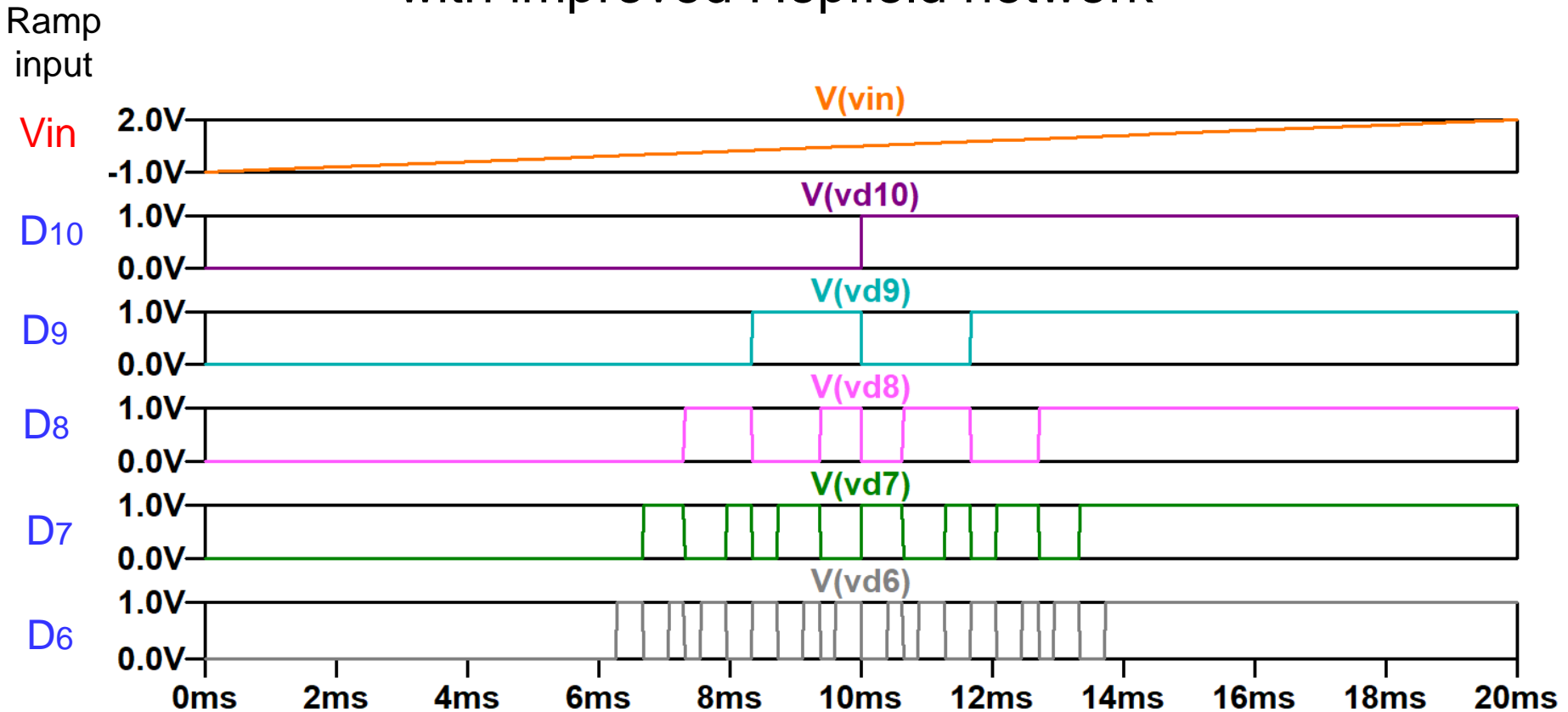


Higher 5 bits

# SPICE Simulation Result

10-bit asynchronous Fibonacci number weighted SAR ADC
with improved Hopfield network



Ramp input

Vin

D5

D4

D3

D2

D1

Lower 5 bits

# Decimal Data Calculation

$$\text{Data} = (1/R)\, D_{10} + (1/R_9)\, D_9 + (1/R_8)D_8 + (1/R_7)D_7 + (1/R_6)D_6$$
$$+ (1/R_5)D_5 + (1/R_4)D_4 + (1/R_3)D_3 + (1/R_2)D_2 + (1/R_1)D_1$$
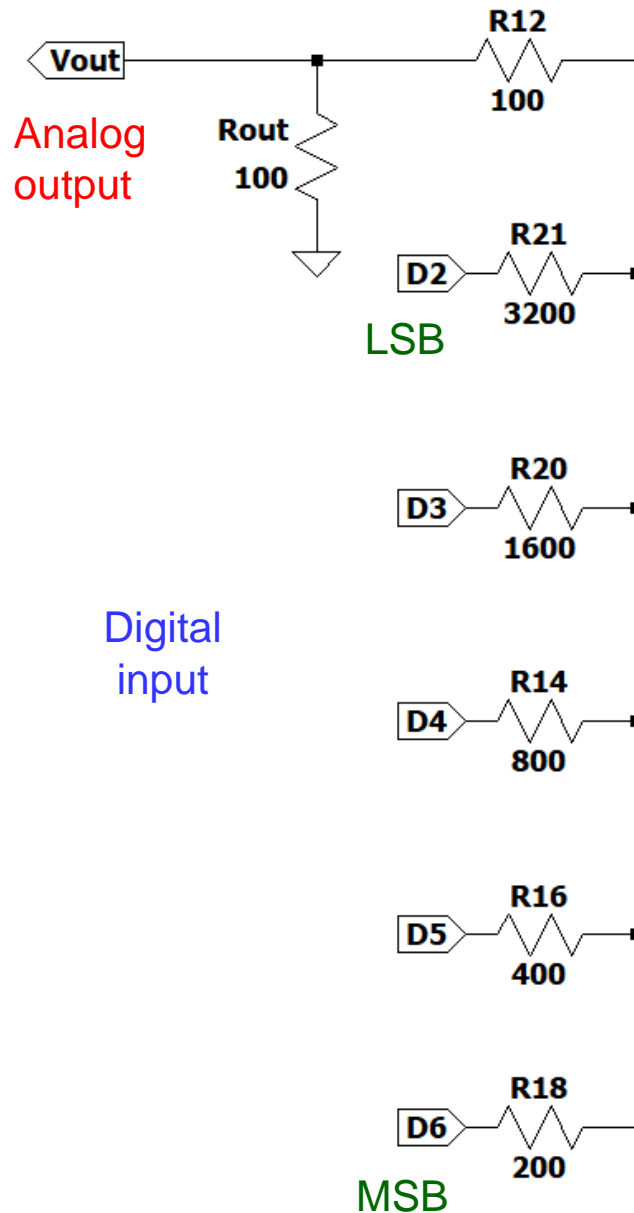
**Data**

Digital
Output

Analog Input
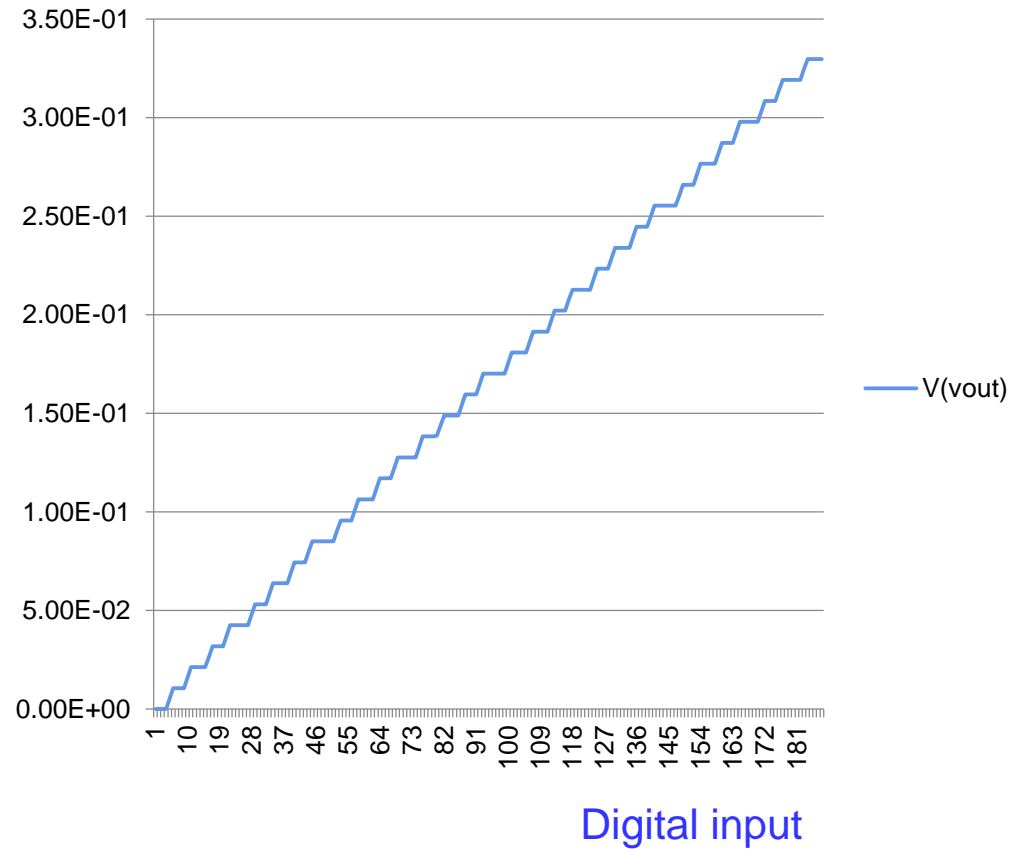
● Operation has been confirmed.

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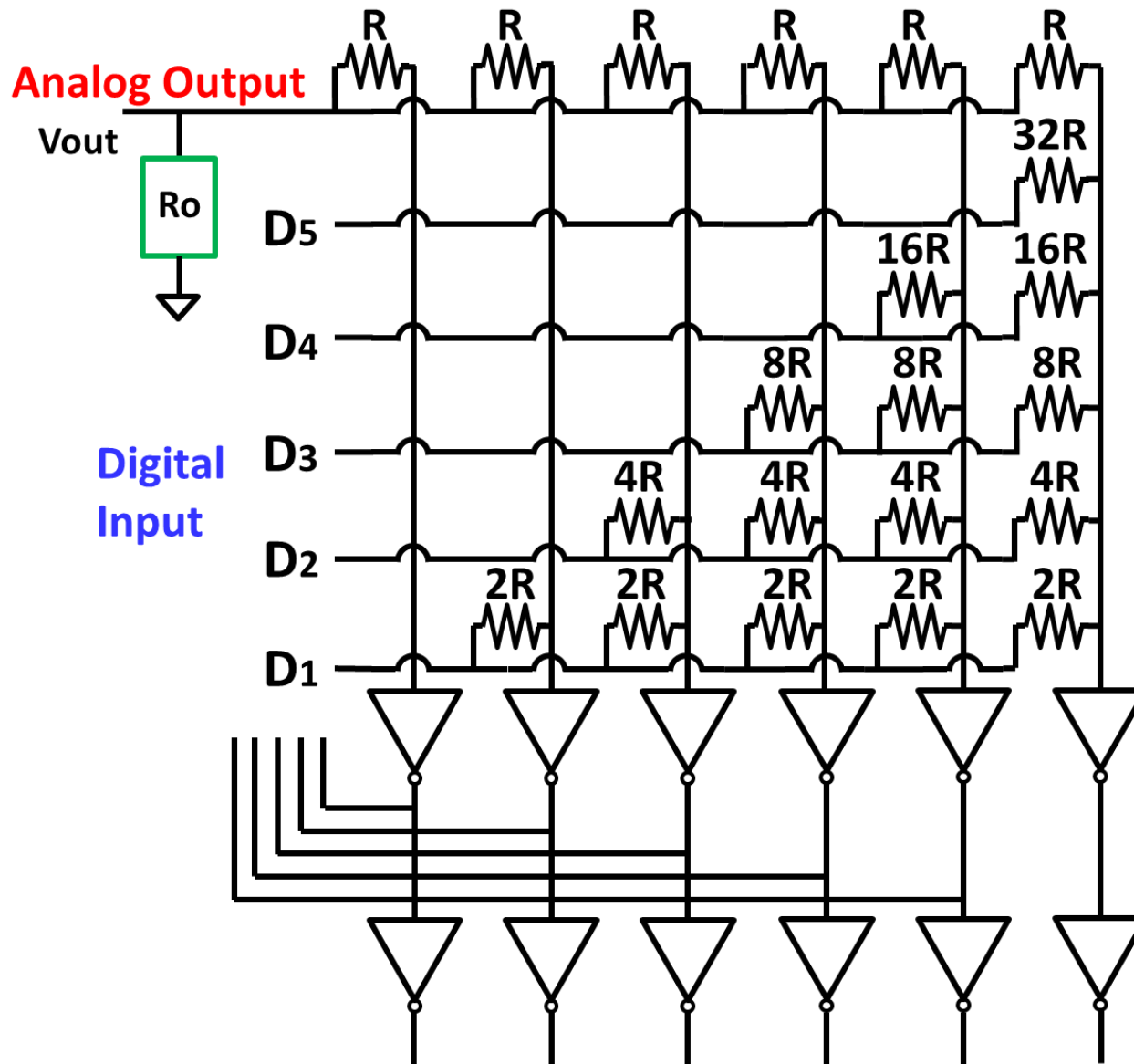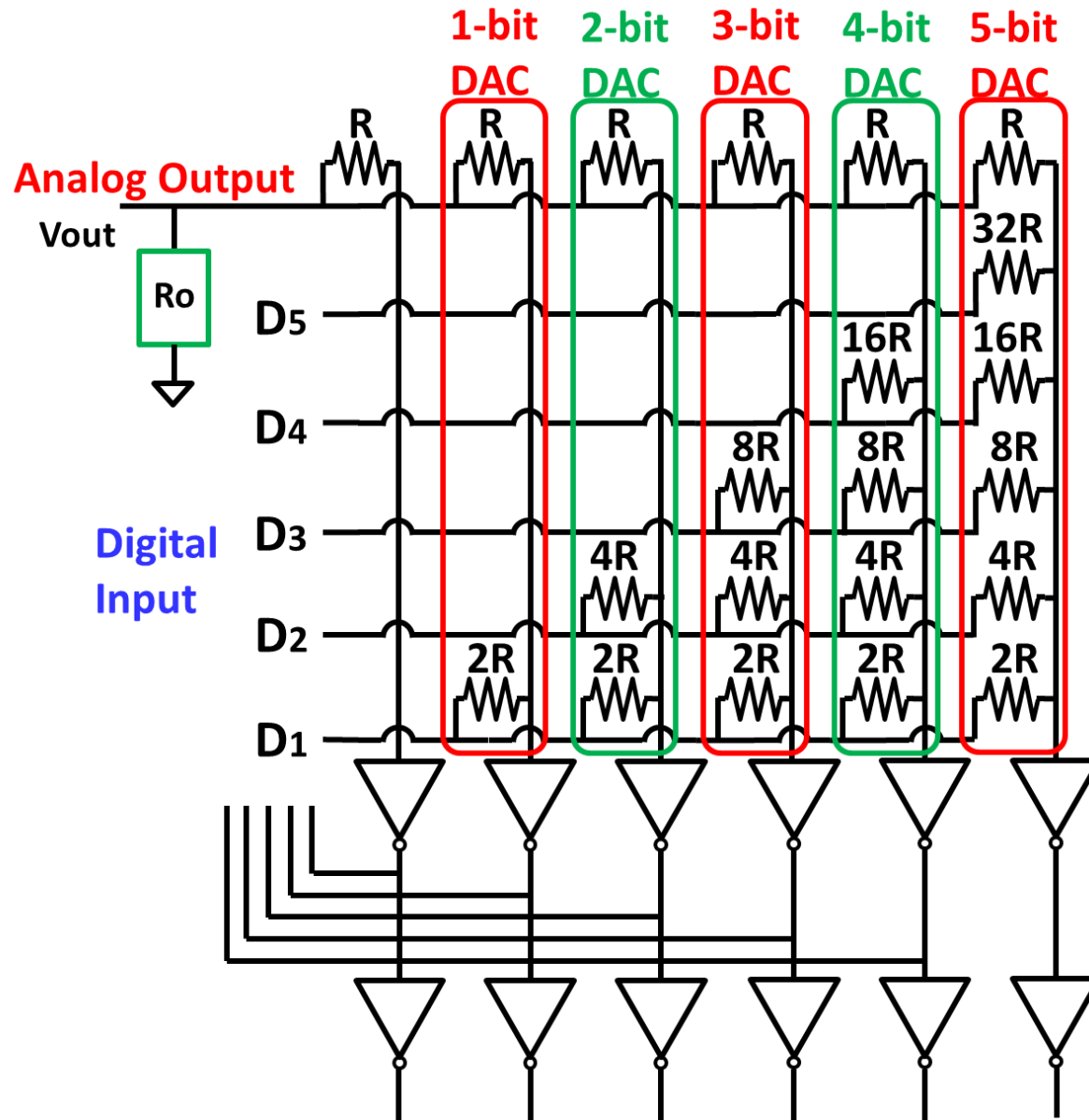
●Conclusion

# DAC inside Hopfield network

# DAC array inside network

# DAC array inside network

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# Conclusion

- Improved Hopfield network ADC

- Asynchronous SAR ADC

  - Very fast

  - Simple design

  - Non-binary as well as binary configurations

  - Competitive to state-of-the-art SAR ADC

  - Verified by SPICE simulation

- Large resistors with good matching and small chip area

    $\Rightarrow$ Technology development is expected

Thank you for listening

ご清聴ありがとうございました