Segmented DAC Linearity Improvement Algorithm Using Unit Cell Sorting with Digital Method

Yi Liu , Anna Kuwana , Xiongyan Li ,
Atsushi Motozawa , Haruo Kobayashi

Division of Electronics and Informatics,
Gunma University
Renesas Electronics Corp

OUTLINE

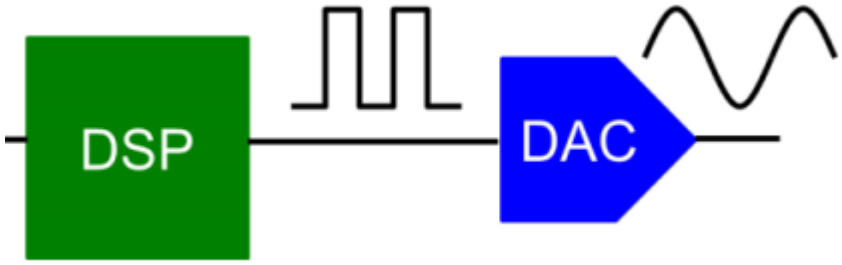
- Research Background and Objective
- Segmented Current-Steering DAC
- Problem Formulation
- Unit Current Cell Sorting Algorithm
- Simulation Results
- DAC Architecture with Sorting Algorithm
- Conclusion

OUTLINE

- Research Background and Objective
- Segmented Current-Steering DAC
- Problem Formulation
- Unit Current Cell Sorting Algorithm
- Simulation Results
- DAC Architecture with Sorting Algorithm
- Conclusion

Research Background

Digital-to-Analog Converter (DAC)



- Key component in modern transmitter circuits.
- High linearity is required.

Research Objective

Nano-CMOS implementation of DAC

- Device mismatch is large
- DAC linearity deteriorates
- Digital circuit can be implemented with small chip area

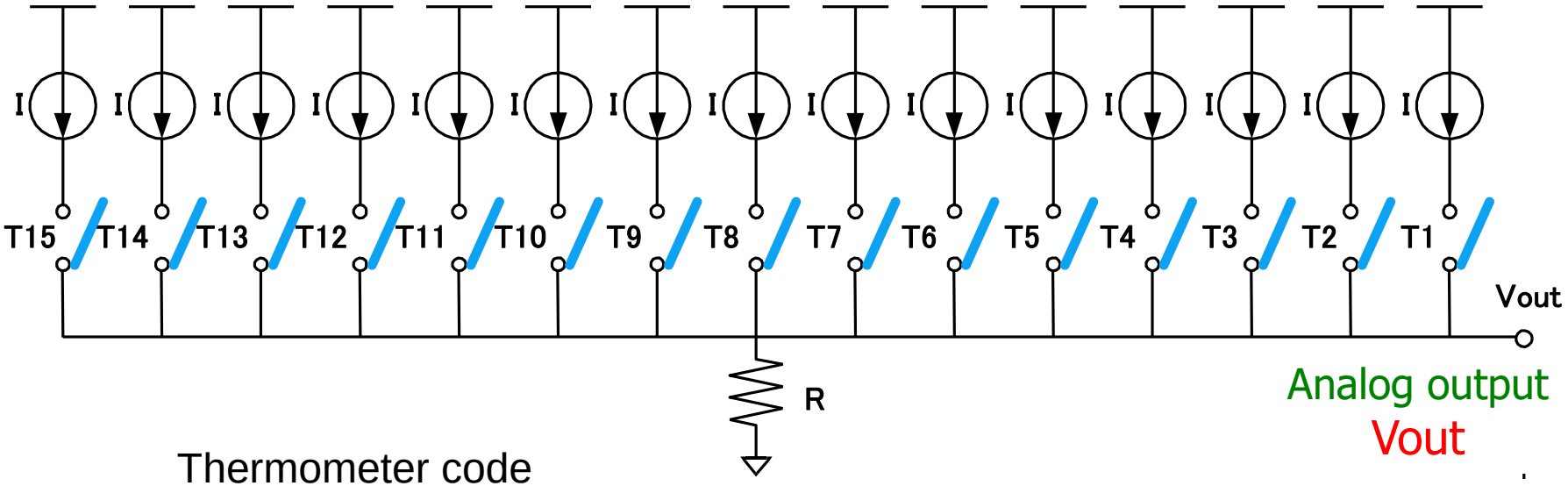
Development of digital calibration method for DAC non-linearity

Digitally-assisted analog technology

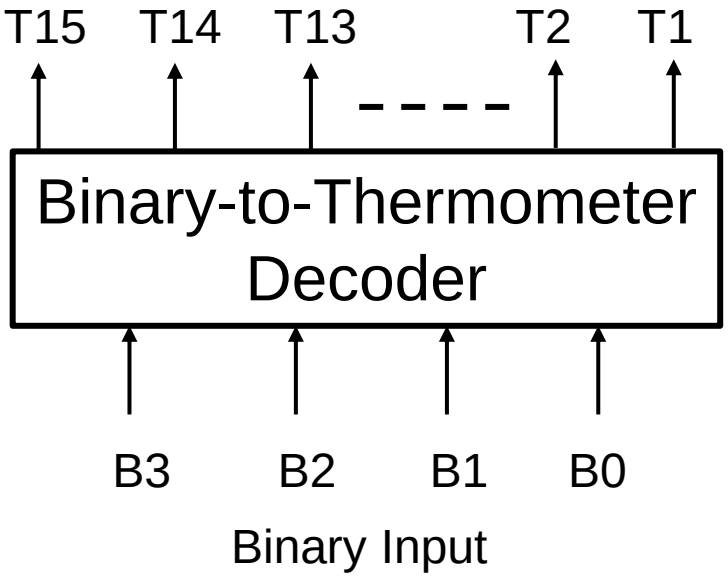
OUTLINE

- Research Background and Objective
- Segmented Current-Steering DAC
- Problem Formulation
- Unit Current Cell Sorting Algorithm
- Simulation Results
- DAC Architecture with Sorting Algorithm
- Conclusion

Segmented DAC Configuration: 4-bit case



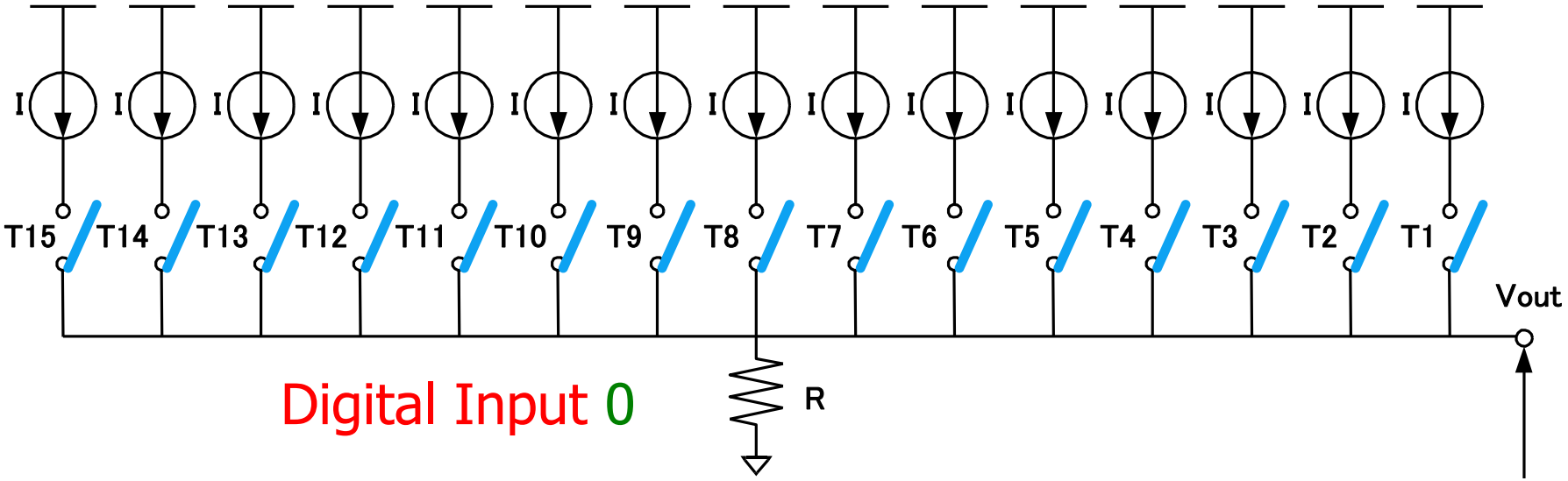
Thermometer code



Features

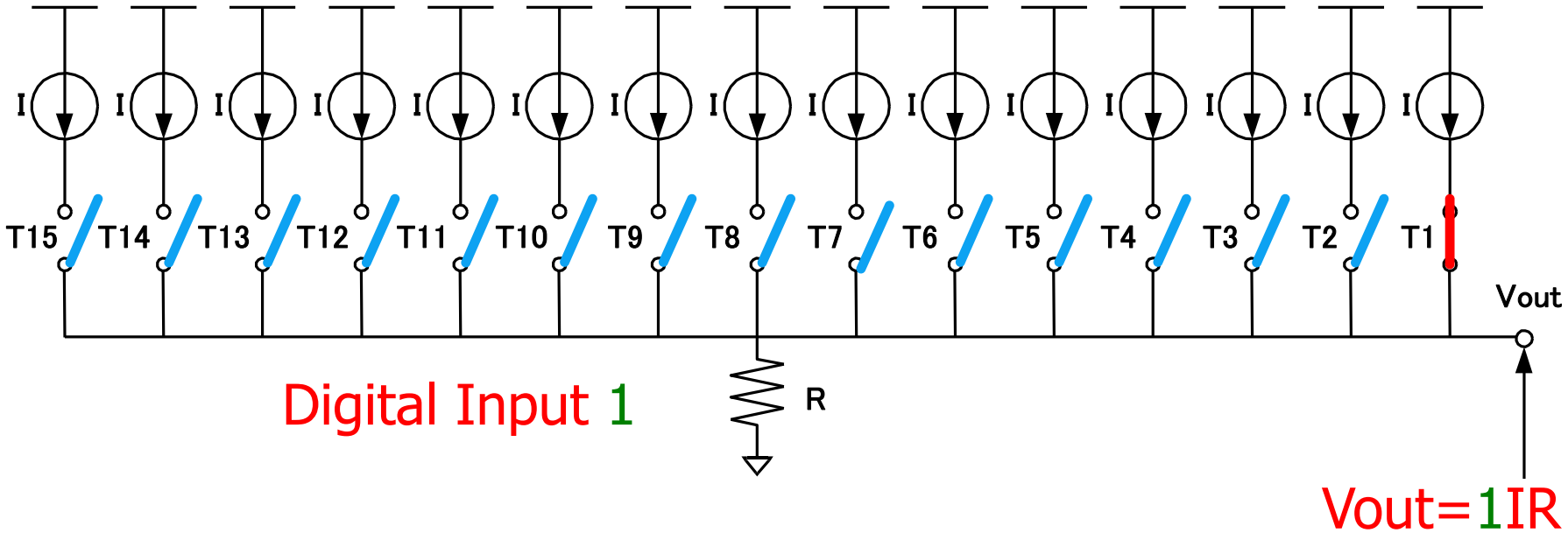
- Monotonicity guaranteed
- Small glitch
- Small DNL
- Decoder required

Segmented DAC Operation: Digital Input = 0

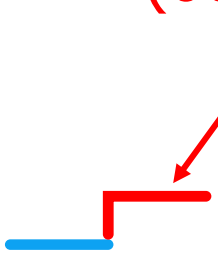


(000000000000000)

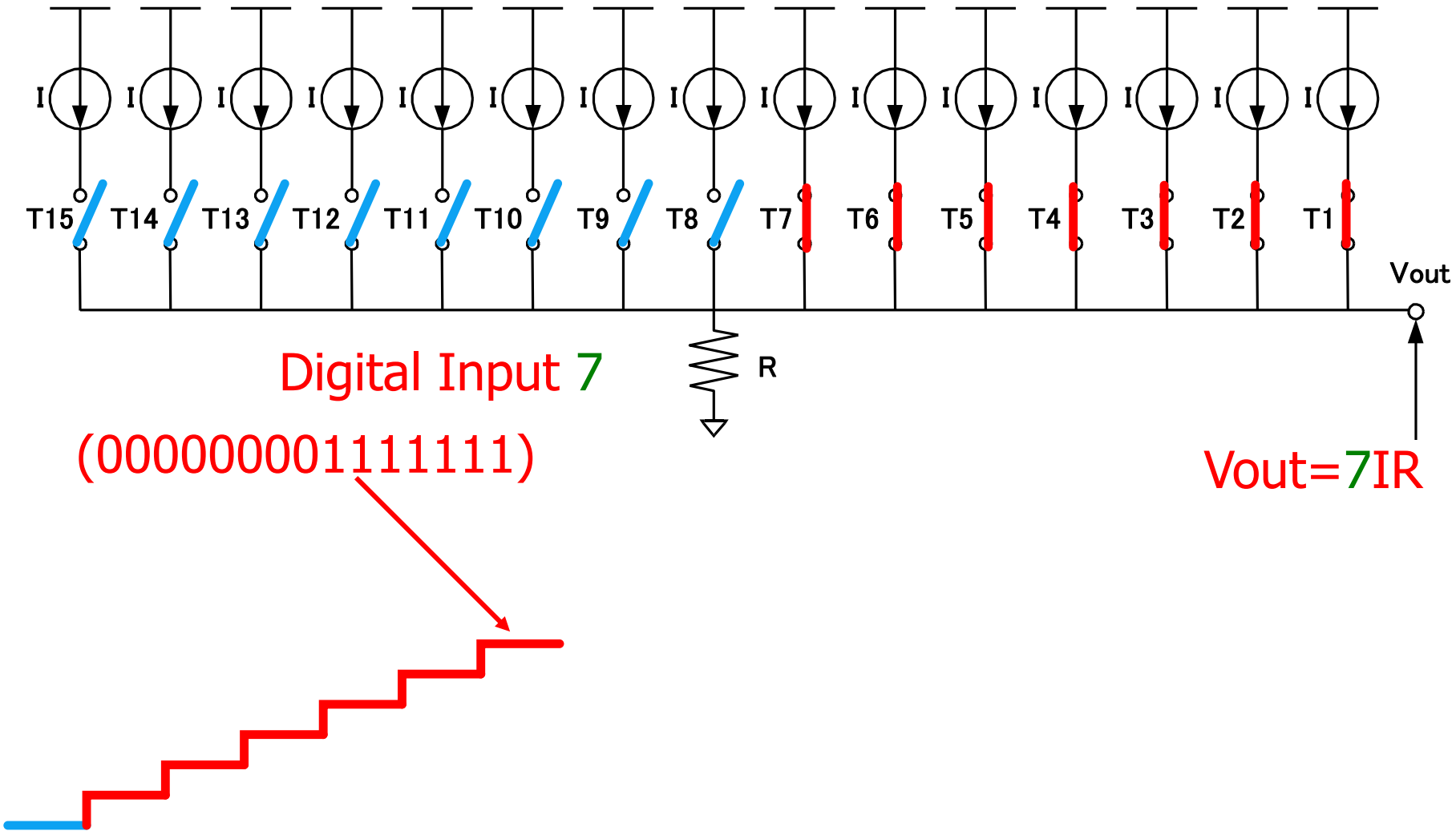
Segmented DAC Operation: Digital Input = 1



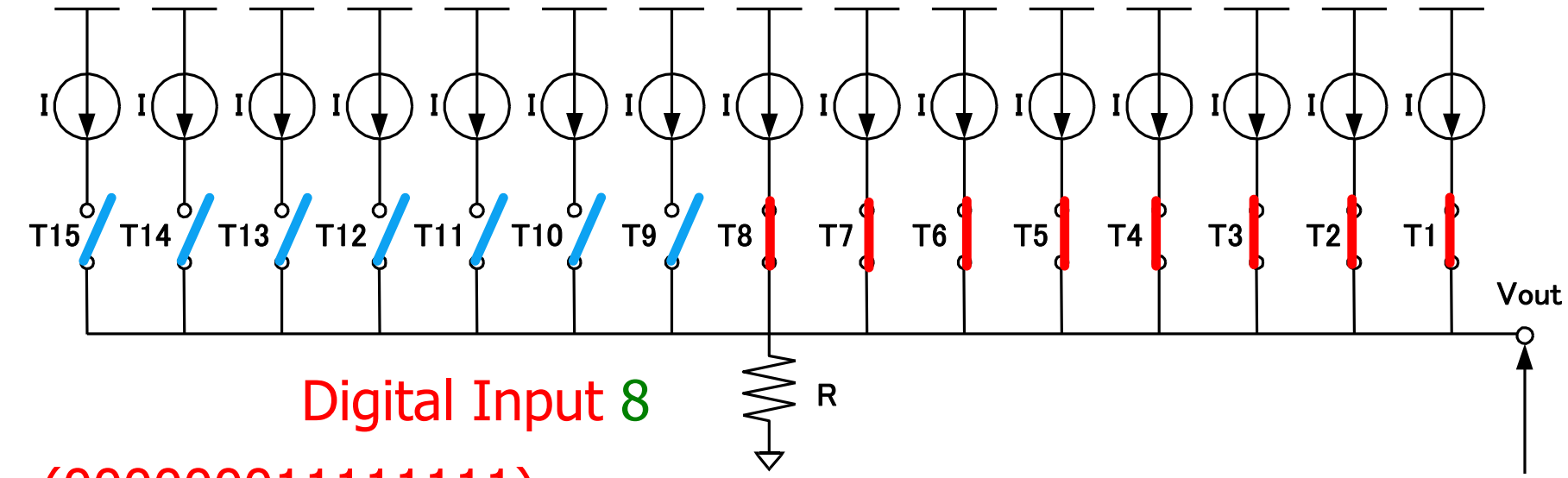
(000000000000001)

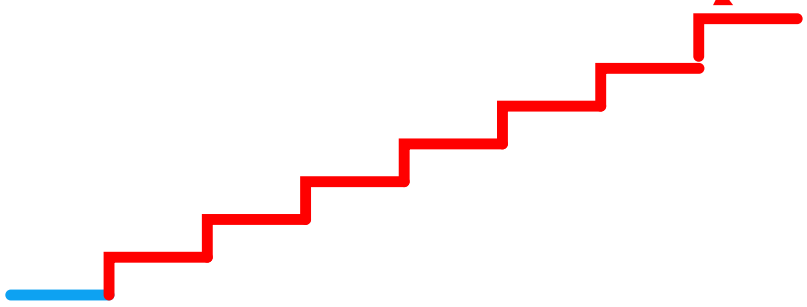


Segmented DAC Operation: Digital Input = 7

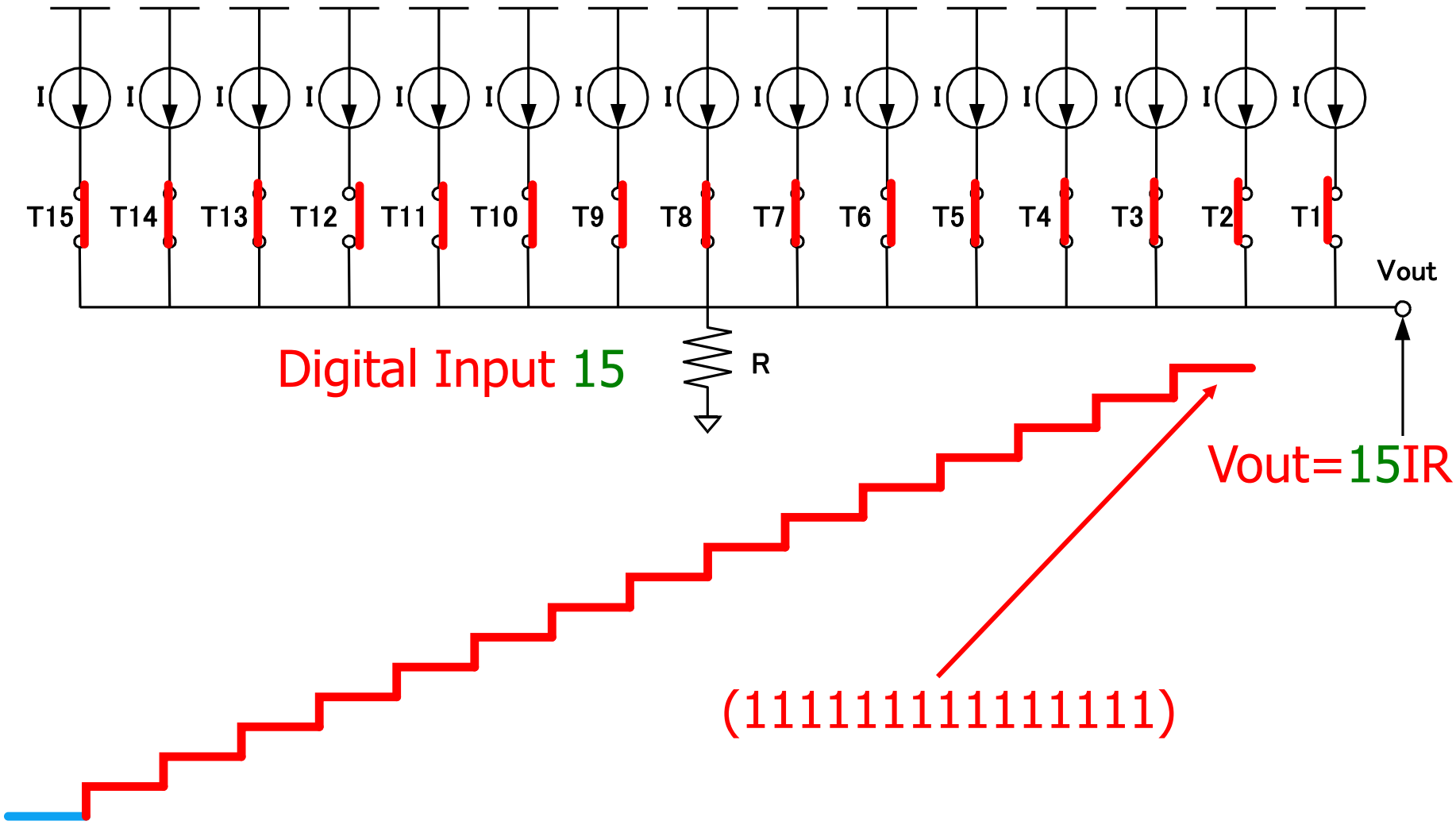


Segmented DAC Operation: Digital Input = 8





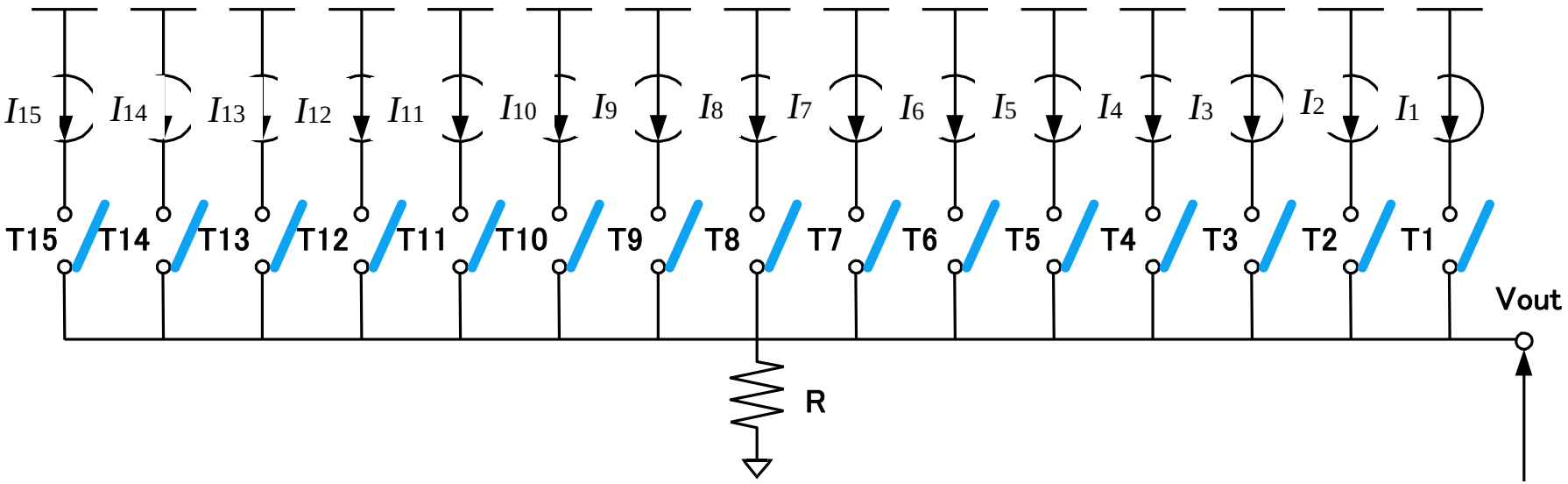
Segmented DAC Operation: Digital Input = 15



OUTLINE

- Research Background and Objective
- Segmented Current-Steering DAC
- Problem Formulation
- Unit Current Cell Sorting Algorithm
- Simulation Results
- DAC Architecture with Sorting Algorithm
- Conclusion

Problem of Actual Segmented DAC



Ideal DAC :

$$I_1 = I_2 = I_3 = \ldots = I_N.$$

Actual DAC : Mismatches among current sources

$$I_1 = I + \Delta I_1,\ I_2 = I + \Delta I_2,\ I_3 = I + \Delta I_3, \ldots,\ I_N = I + \Delta I_N.$$

I : Average current

Problem Formulation

Current sources with mismatches

$$I_1 = I + \Delta I_1,\ I_2 = I + \Delta I_2,\ I_3 = I + \Delta I_3, \ldots,\ I_N = I + \Delta I_N.$$

Definition of average current

$$I = \frac{1}{N}\left[I_1 + I_2 + I_3 + \ldots + I_N\right].$$

$$\Delta I_1 + \Delta I_2 + \Delta I_3 + \ldots + \Delta I_N = 0.$$

For digital input = k

$$V_{OUT} = R\ (I_{n1} + I_{n2} + \ldots + I_{nk}) = R\,(\mathrm{k}\,I + \underbrace{\Delta I_{n1} + \Delta I_{n2} + \ldots + \Delta I_{nk}}_{\text{Integral Non-Linearity (INL)}})$$

Choose k current sources

$$|\Delta I_{n1} + \Delta I_{n2} + \ldots + \Delta I_{nk}| \Rightarrow \text{Very Small}$$

OUTLINE

- Research Background and Objective
- Segmented Current-Steering DAC
- Problem Formulation
- Unit Current Cell Sorting Algorithm
- Simulation Results
- DAC Architecture with Sorting Algorithm
- Conclusion

Switching Sequence Post-Adjustment (SSPA)

Features

- Calibration method after fabrication process
- Change the switching sequence of unit current cells
- DAC integral linearity is improved.

Disadvantage

- Current comparator usage

[1] T. Chen, G. Gielen (KU Leuven), “A 14-bit 200-MHz Current-Steering DAC with Switching Sequence Post-Adjustment Calibration”, IEEE ASSCC (Nov. 2006)

Our research here

- No need for current comparator
- Deep analysis of SSPA

Unit Current Cell Sorting Algorithm

1) Measure values of unit current cells with VCO instead of comparator
   Store them in memory from the lowest to the highest order.

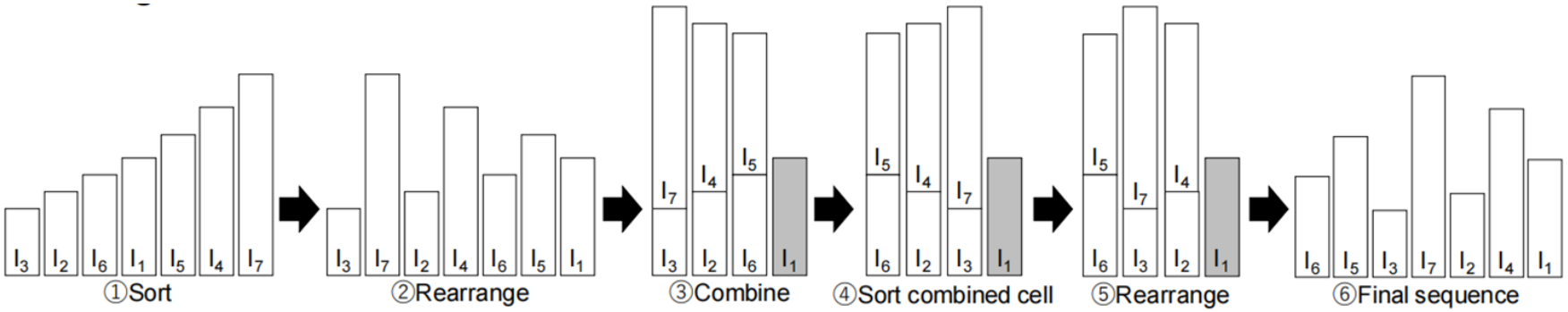
2) Rearrange them
   by arranging small unit current cells between two large cells,

3) Sum two neighboring unit current cells

4) Measure summed unit current cells again measured
   and sort as 2).

5) Rearranged as 3).

6) Final sequence is obtained.

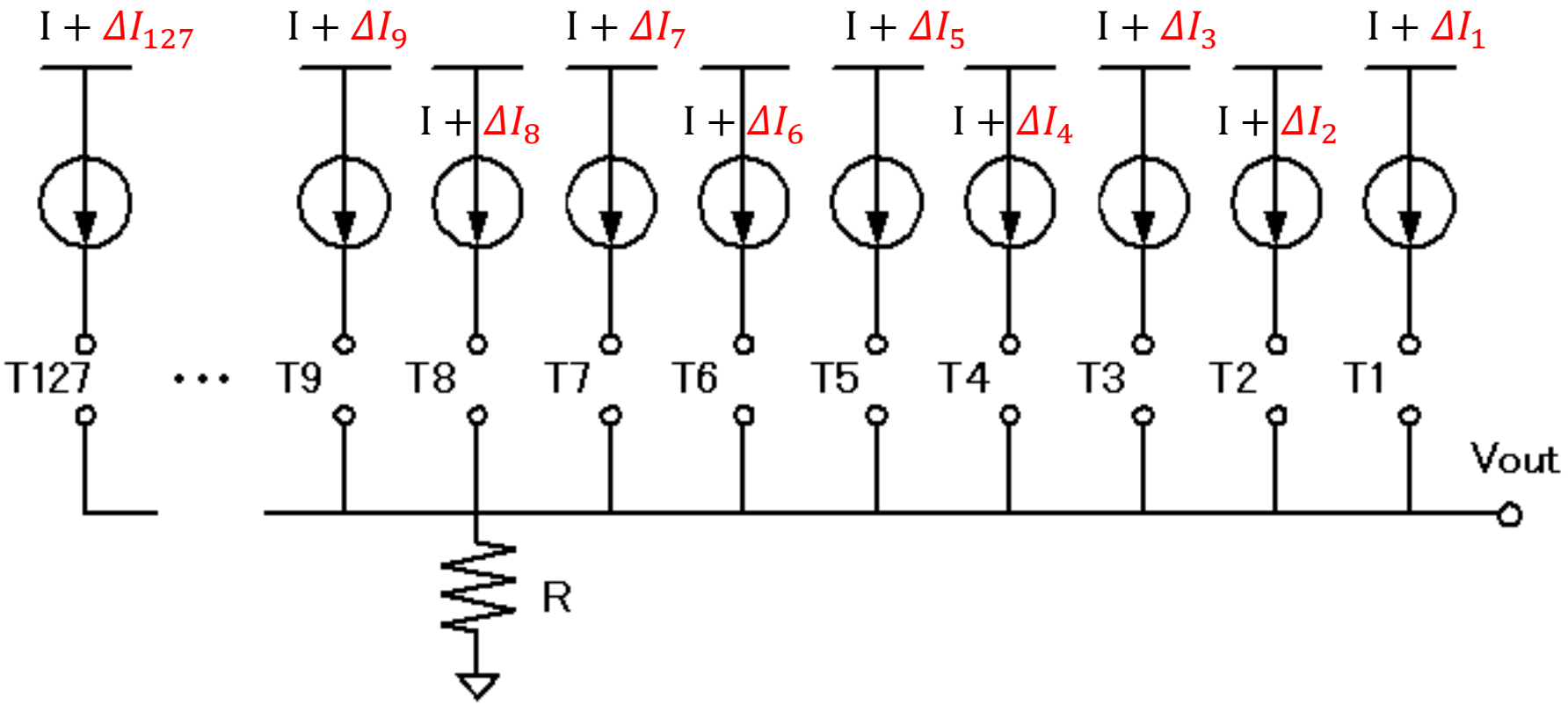


OUTLINE

- Research Background and Objective
- Switching Sequence Post Adjustment
- Problem Formulation
- Unit Current Cell Sorting Algorithm
- Simulation Results
- DAC Architecture with Sorting Algorithm
- Conclusion

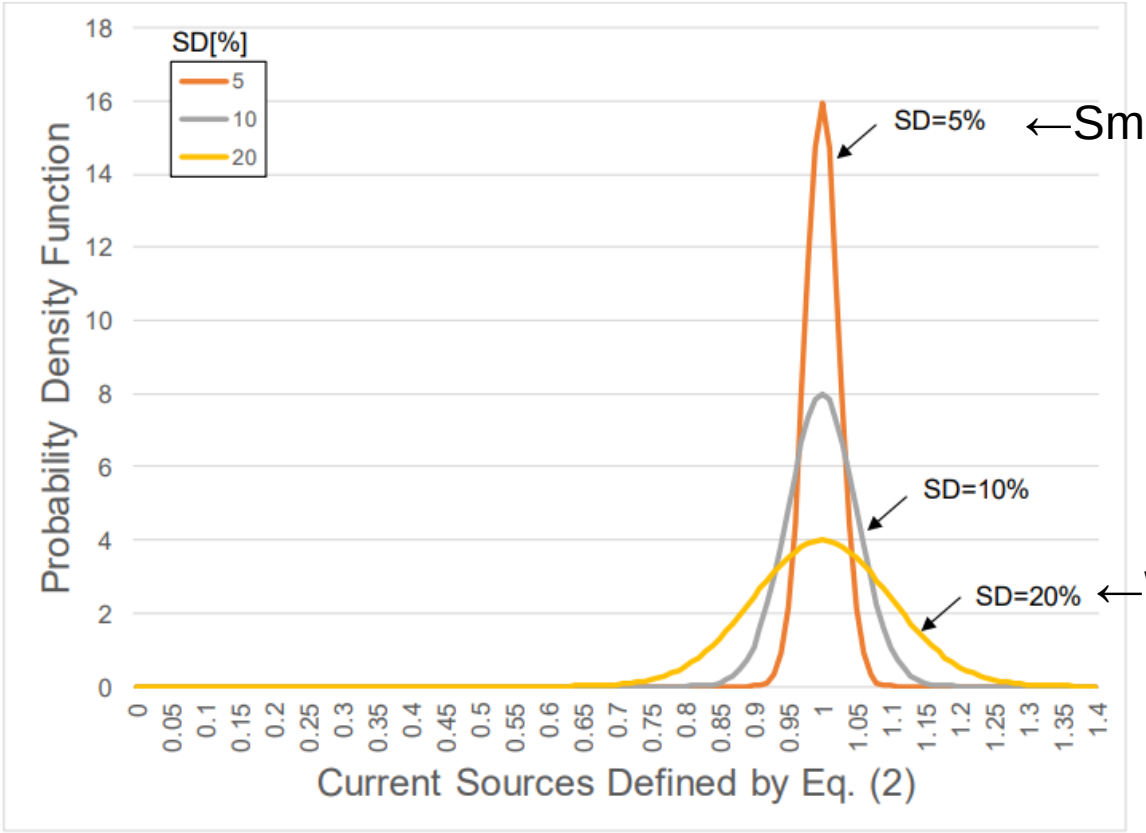
Simulation Conditions

Assuming a 7-bit DAC, 127 current sources are used.
The current sources have mismatches. (ΔI_i)



Mismatch variation as a parameter

Mismatches vary within the range of SD [%].
The simulation was performed by varying the degree of mismatches from 1% to 20% as parameter SD.



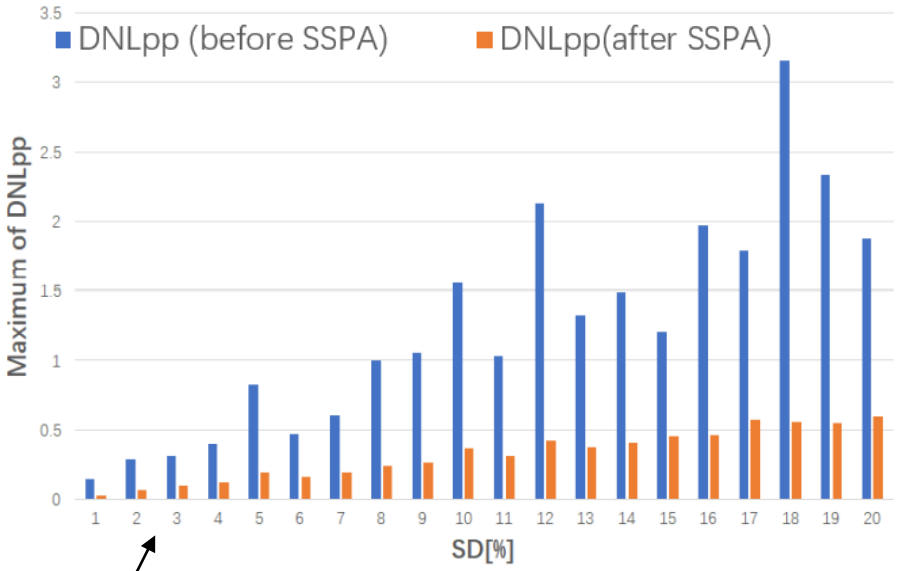
$\leftarrow \mathrm{I} + \Delta I_i$

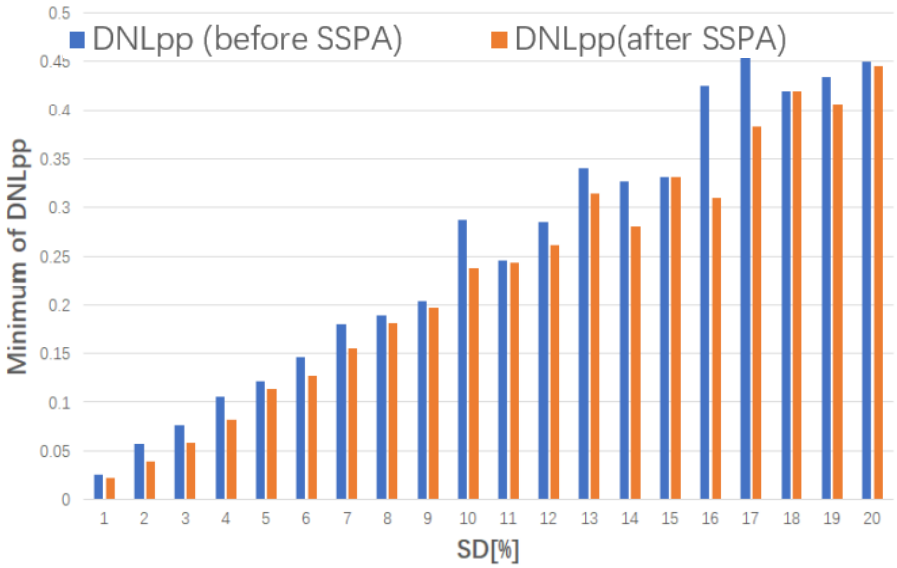
Example of the current sources mismatches

Maximum and minimum value of DNLpp

DNLpp=maximum(DNL_{k1})-minimum(DNL_{k2})

DNLpp before SSPA and after SSPA are analyzed.





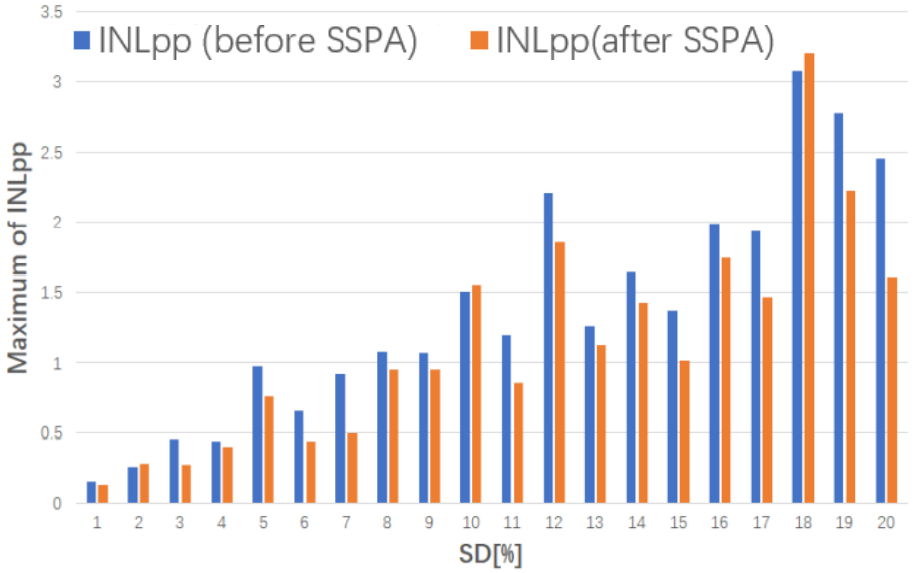
Maximum and minimum value of DNLpp during 10 times of simulation

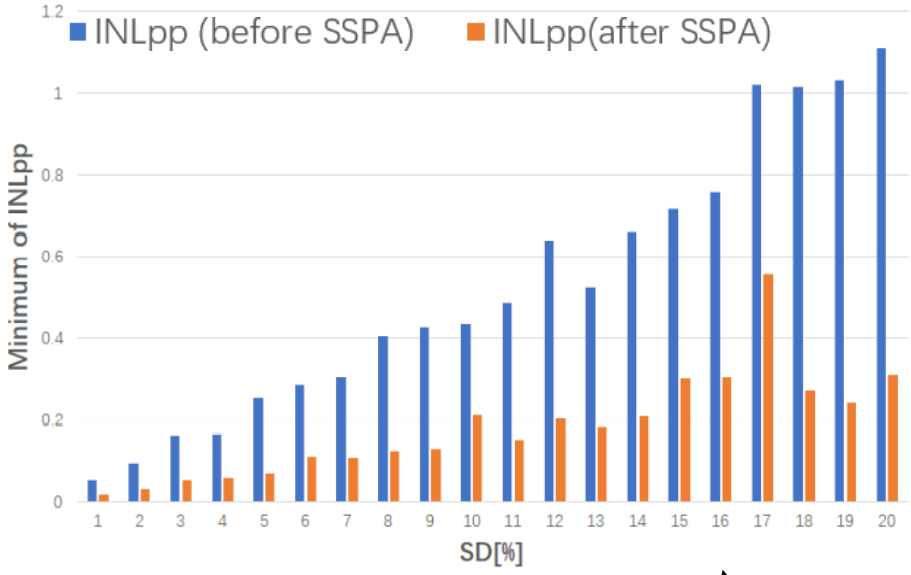
SSPA is greatly reduced the maximum value of DNLpp.

Maximum and minimum value of INLpp

INLpp=maximum(INL_{k3})-minimum(INL_{k4})

INLpp before SSPA and after SSPA are analyzed.



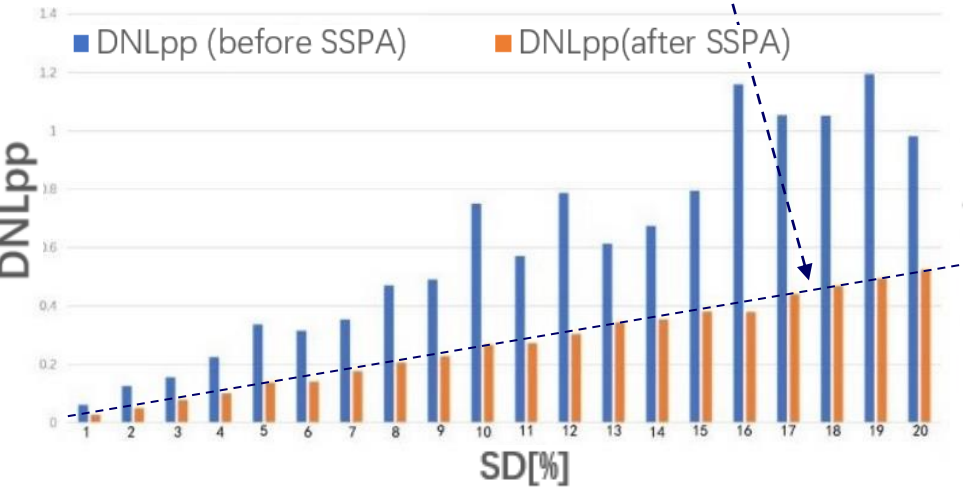


Maximum and minimum value of INLpp during 10 times of simulation

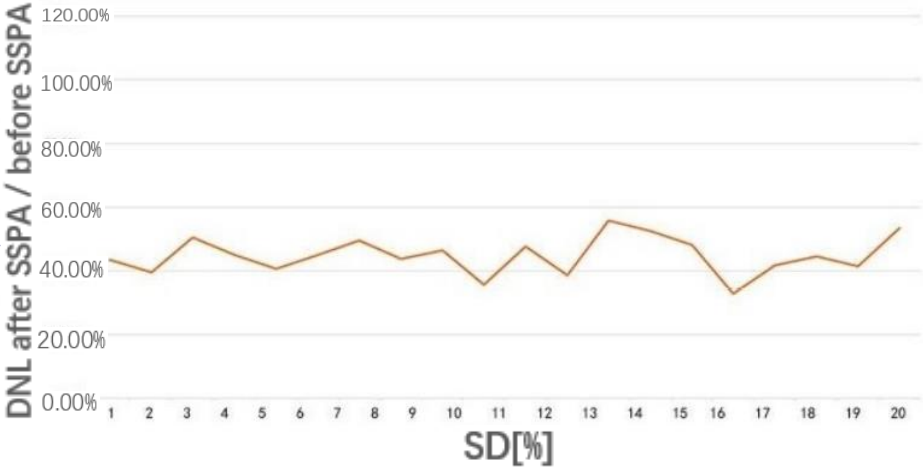
SSPA is greatly reduced the minimum value of INLpp.

Average value of DNLpp before SSPA and after SSPA

- Average value of DNLpp is also reduced by SSPA.
- DNLpp tended to increase as the SD increased.
- DNLpp were reduced by about 40% by SSPA.
- The larger the SD is, the larger absolute value of DNLpp reduction is.
- After SSPA, DNLpp increases in proportion to SD.
  (DNLpp = 0.025 × SD).



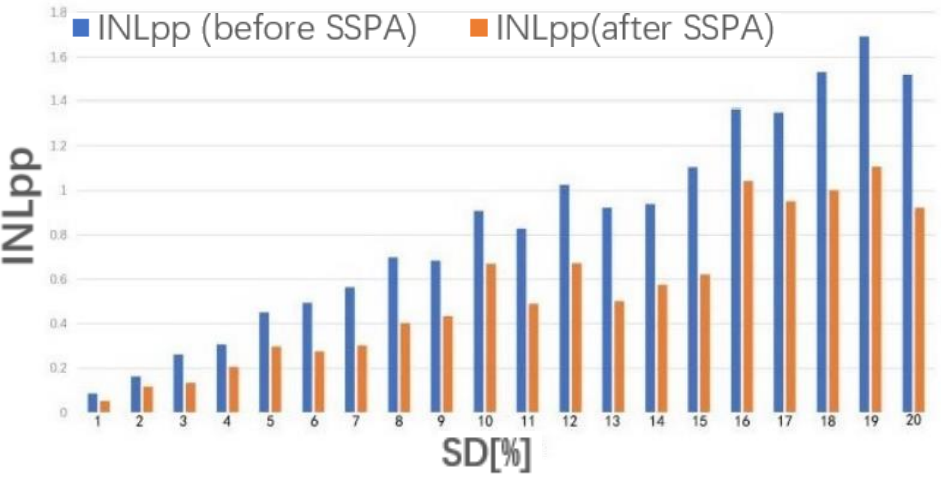
DNLpp before SSPA and after SSPA



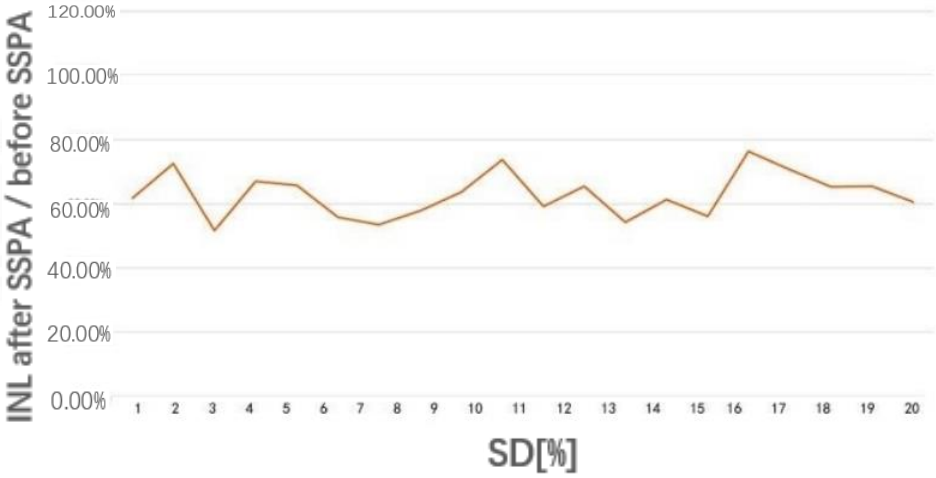
Reduction ratio by SSPA

Average value of INLpp before SSPA and after SSPA

- Average value of INLpp is also reduced by SSPA.
- INLpp tended to increase as the SD increased.
- INLpp were reduced by about 60% by SSPA.
- The larger the SD is, the larger absolute value of INLpp reduction is.
- SSPA is significantly reduced the minimum value of INLpp.
  It reduced the average value of INLpp.



INLpp before SSPA and after SSPA

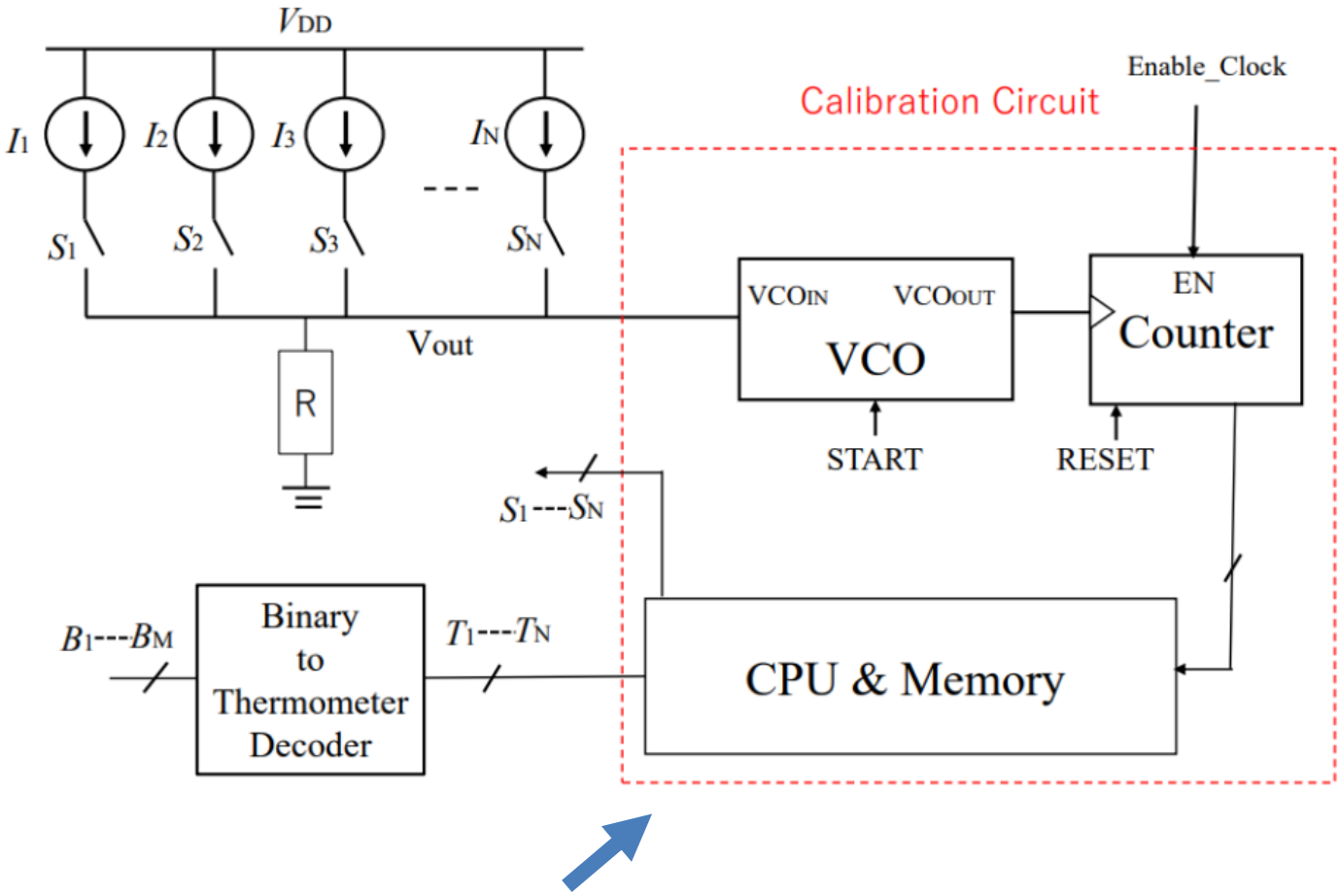


Reduction ratio by SSPA

OUTLINE

- Research Background and Objective
- Segmented Current-Steering DAC
- Problem Formulation
- Unit Current Cell Sorting Algorithm
- Simulation Results
- DAC Architecture with Sorting Algorithm
- Conclusion

DAC Architecture with Calibration using Sorting Algorithm

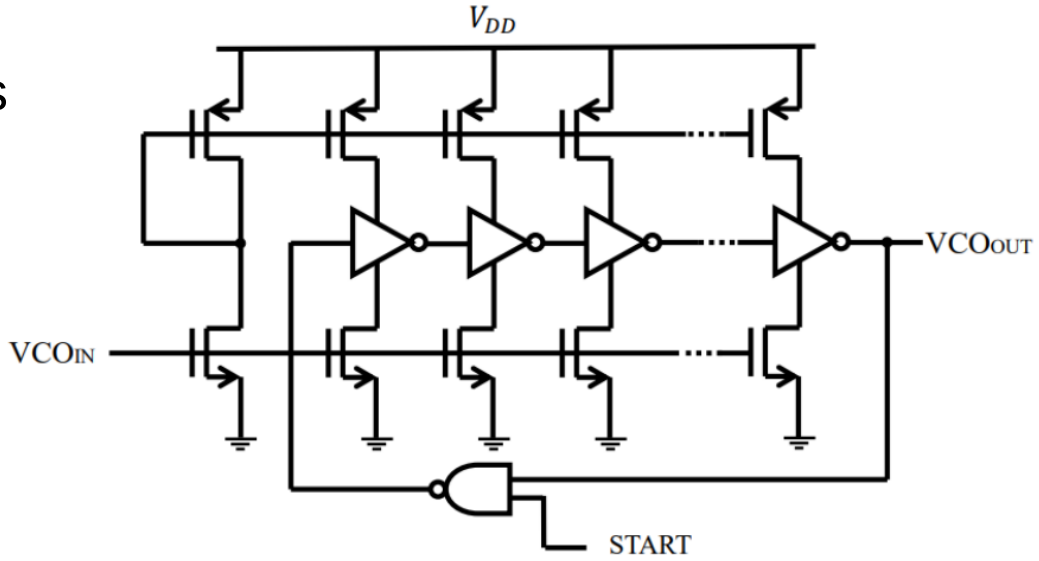


- Implementation with only digital circuit

  No need for a current comparator

VCO with Current-Controlled Inverters and START Circuit

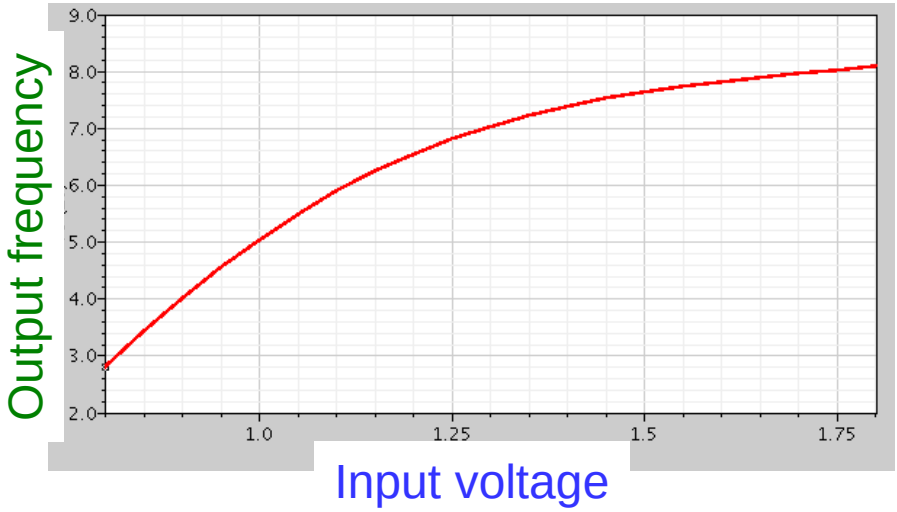
Ring oscillators



Input voltage

Output frequency

SPICE simulation results



Nonlinear, but monotonic characteristics

OUTLINE

- Research Background and Objective
- Segmented Current-Steering DAC
- Problem Formulation
- Unit Current Cell Sorting Algorithm
- Simulation Results
- DAC Architecture with Sorting Algorithm
- Conclusion

Conclusion

- Investigated the segmented current-steering DAC linearity improvement algorithm using unit current cell sorting algorithm (SSPA).

- Simulation results show:

  - SSPA can reduce DNL by about 40%
    INL by about 60%.

  - The larger mismatches among current sources, the larger absolute values of DNL and INL can be reduced.

- Proposed a digital implementation method of the SSPA.

Thank you for listening

Kobayashi Laboratory

群馬大学 GUNMA UNIVERSITY