Analysis of Switching Characteristics of Dual RESURF 40 V N-LDMOS Transistor with Grounded Field Plate

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OUTLINE

- Research Background and Objective
- Device Structures and Features
- Simulation Results
    - Turn-on Process
    - Turn-off Process
- Discussion
- Conclusion
- Acknowledgements

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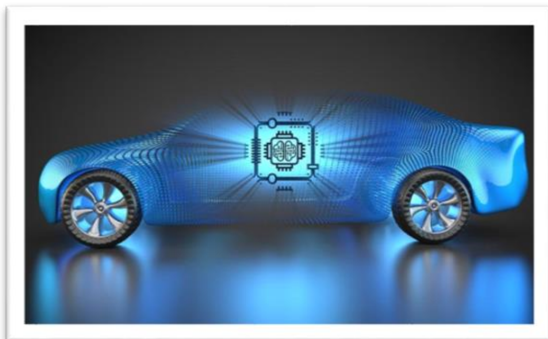
Research Background

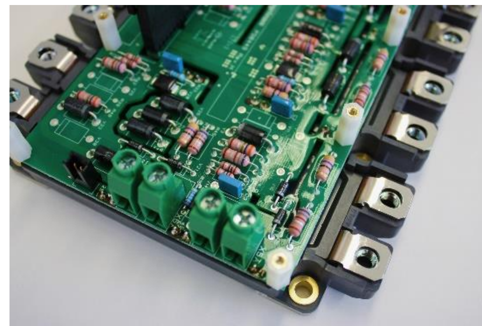
Switches of power converters for automotive applications

High-performance Lateral Double Diffused MOS (LDMOS) transistors

- Low cost: mature Si process can be used
- One-chip integration with other circuits

Attractive in industry

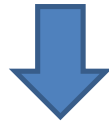




Research Objective

Our previously proposed:

0.18 μm CMOS compatible dual REduced SURface Field (RESURF)
40 V N-LDMOS transistor with grounded field plate



Our research here:

- Detailed analysis of switching loss with the proposed LDMOS
- Clarification of lower loss compared to the conventional LDMOS
- Verification with TCAD simulation

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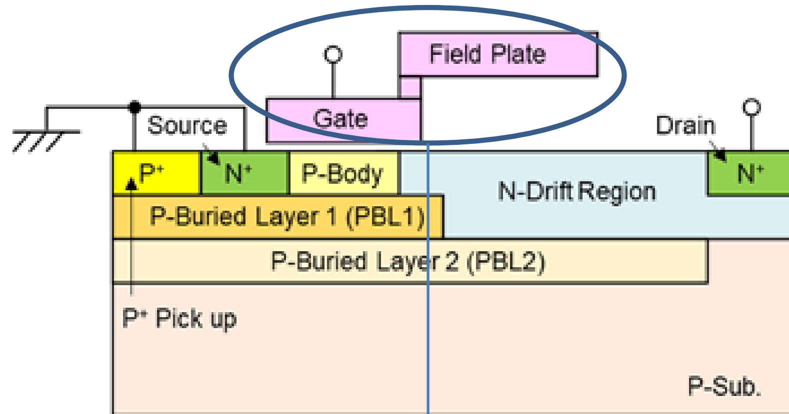
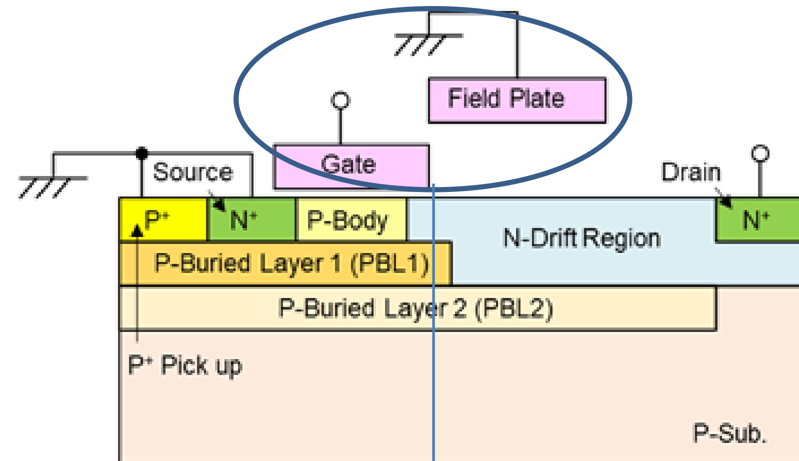
Device Structures and Features

Conventional device



(a) Conventional device

Proposed device [1, 2]



(b) Proposed device

Field plate ➡ connected to gate

Field plate ➡ connected to ground

[1] J. Matsuda, et. al., “A Low Switching Loss 40 V Dual RESURF LDMOS Transistor with Low Specific On-Resistance”, in *Proc. ICMEMIS*, Kiryu, 2017.

[2] J. Matsuda, et. al., “Low Switching Loss and Scalable 20-40 V LDMOS Transistors with Low Specific On-Resistance”, in *Proc. ICTSS*, Kiryu, 2018.

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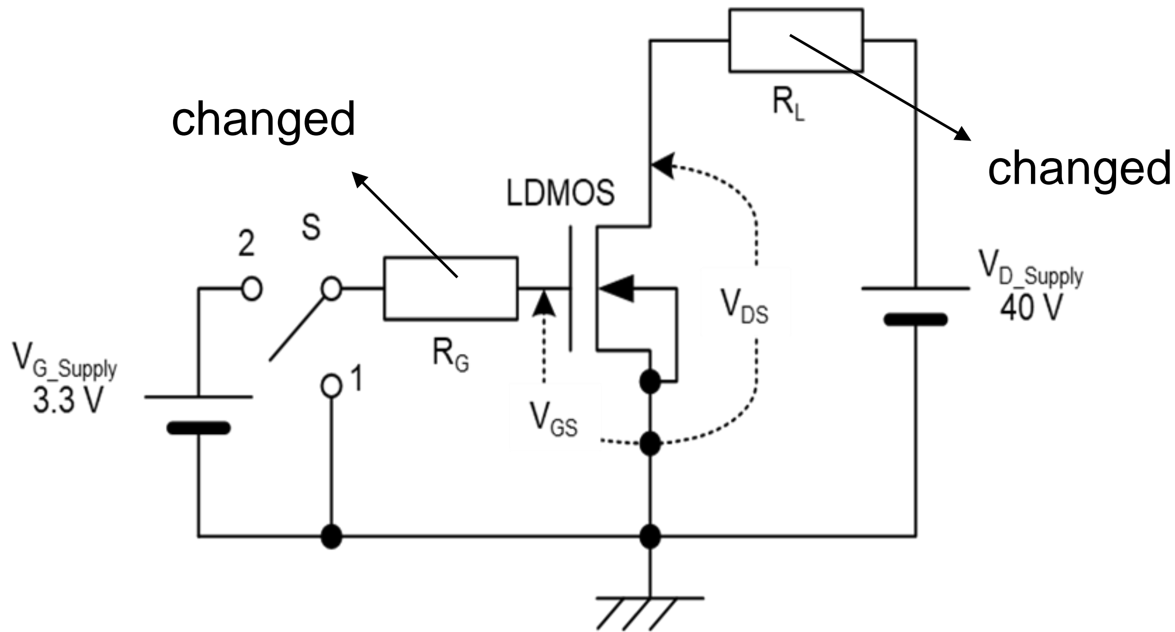
Simulation Circuit



Circuit for TCAD device simulation

R_L changes from 2.13 Ωmm^2 to 10.7 Ωmm^2,

R_G, from 1.07 Ωmm^2 to 5.33 Ωmm^2

for unit LDMOS layout area of 1 mm^2

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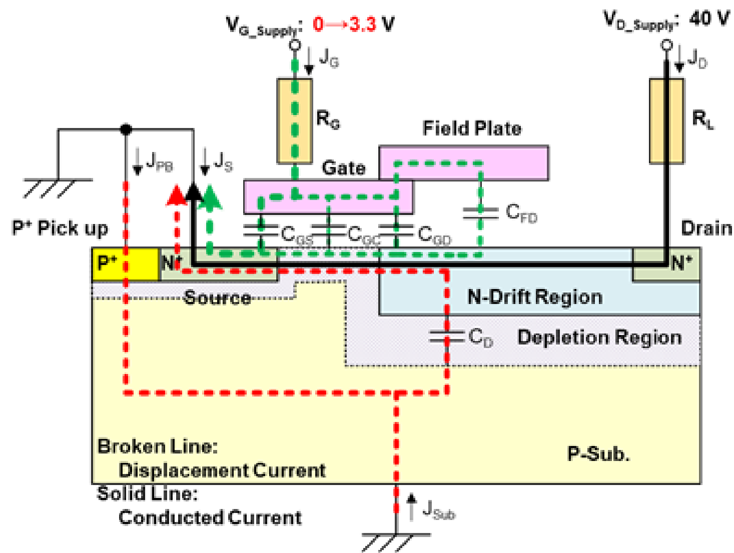
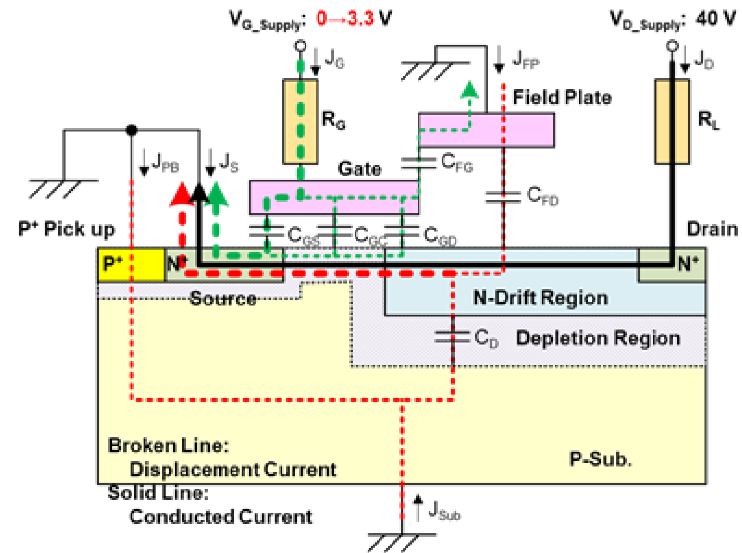
Turn-On Behaviors

Conventional device



(a) Conventional device

Proposed device



(b) Proposed device

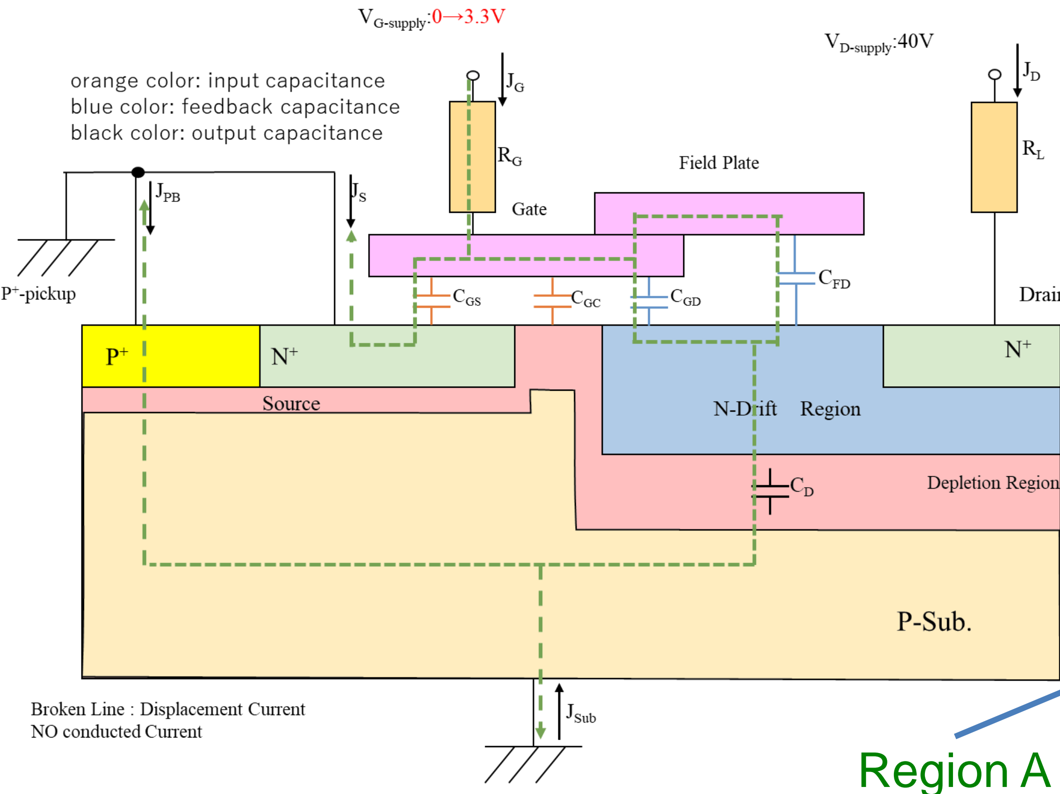
Current paths for turn-on process when $V_{GS} > V_T$.

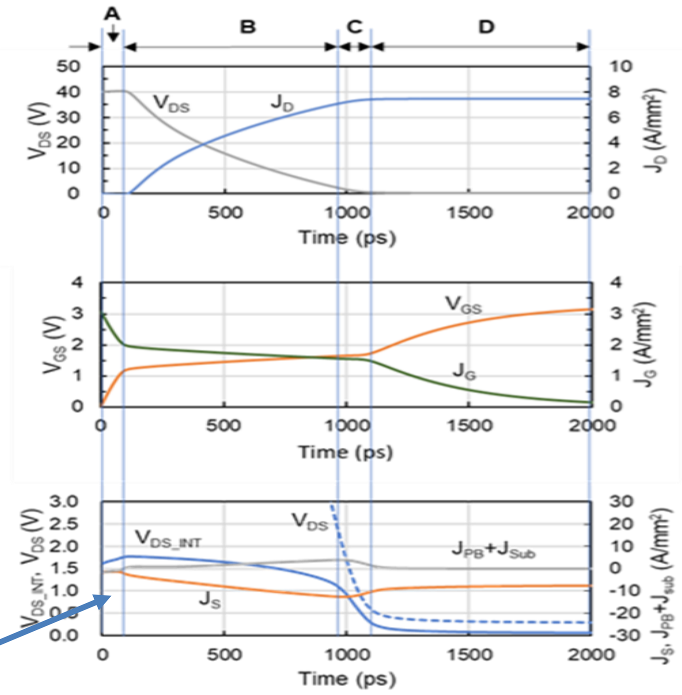
Parasitic capacitances in LDMOS transistors.

Capacitance	Conventional	Proposed
Input capacitance	$C_{GS}+C_{GC}$	$C_{GS}+C_{GC}+C_{FG}$
Feedback capacitance	$C_{GD}+C_{FD}$	C_{GD}
Output capacitance	C_D	C_D+C_{FD}

Turn-On Simulation Results (Region A)

Conventional device





(a) Conventional device

Region A

$V_{GS} < V_T$ ➡ in off-state,

Charging

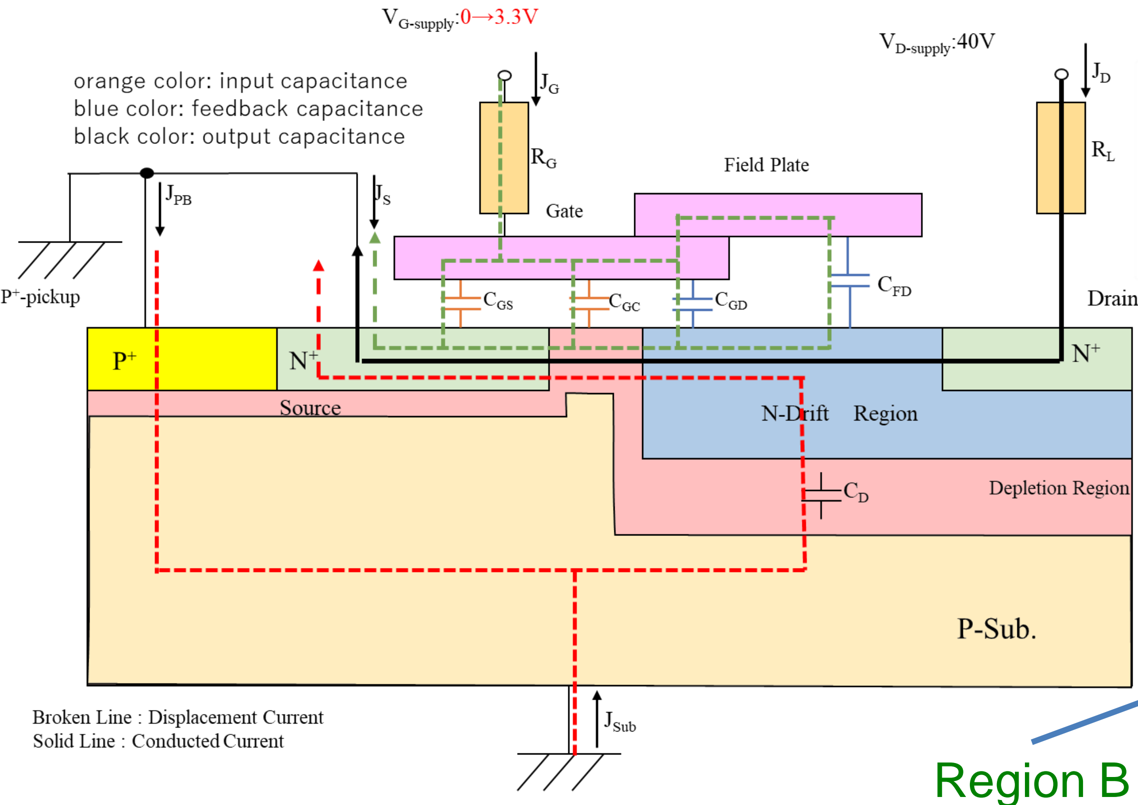
input capacitance(C_{GS}),

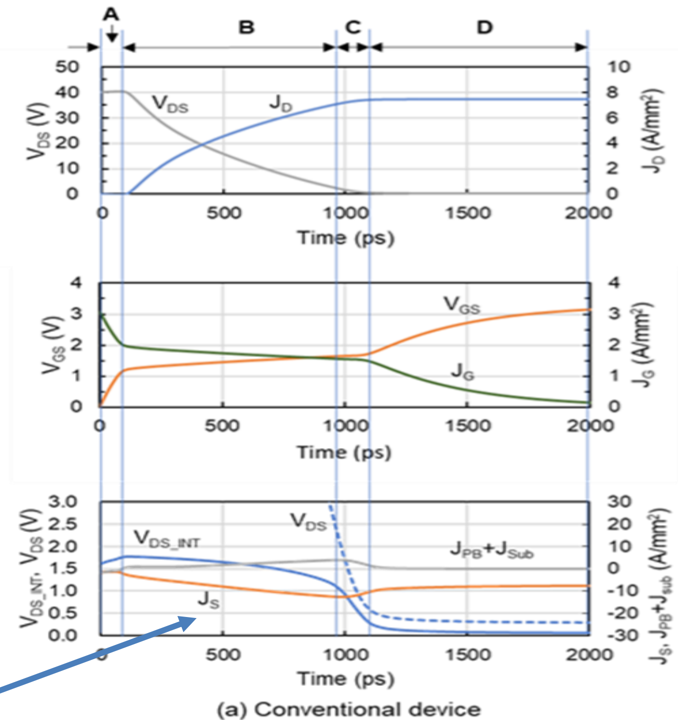
feedback capacitance(C_{GD}+C_{FD}),

output capacitance(C_D)

Turn-On Simulation Results (Region B)

Conventional device

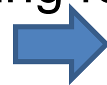




(a) Conventional device

Region B

Charging feedback capacitance (C_{GD}+C_{FD})



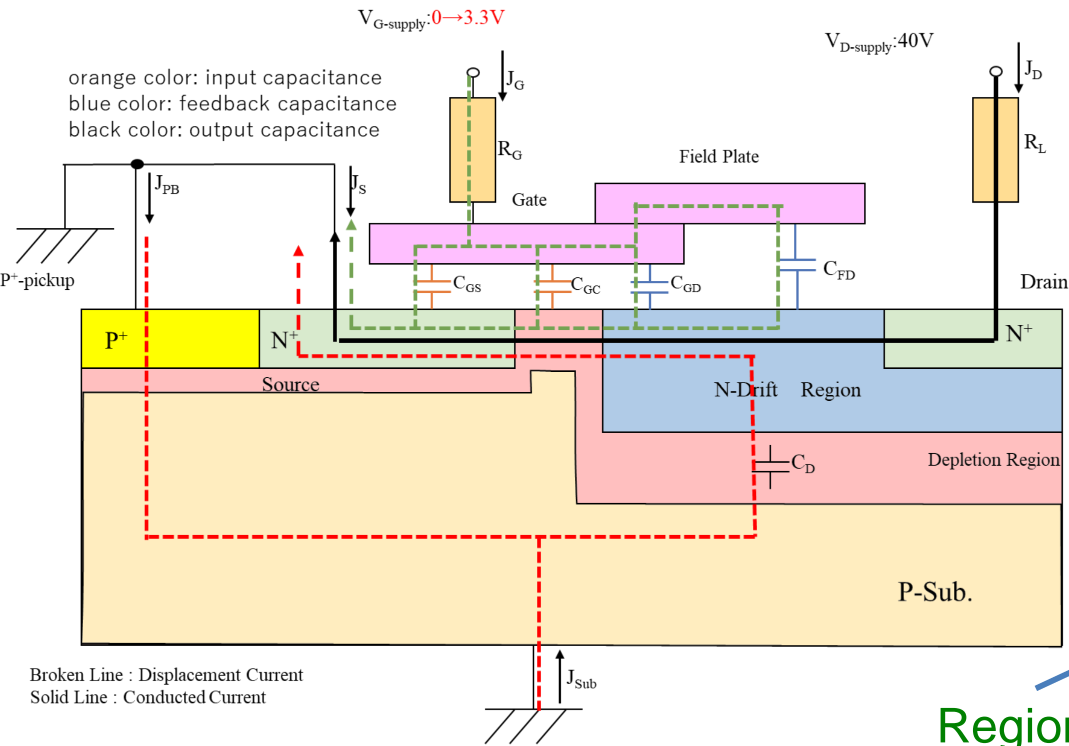
In gate plateau state

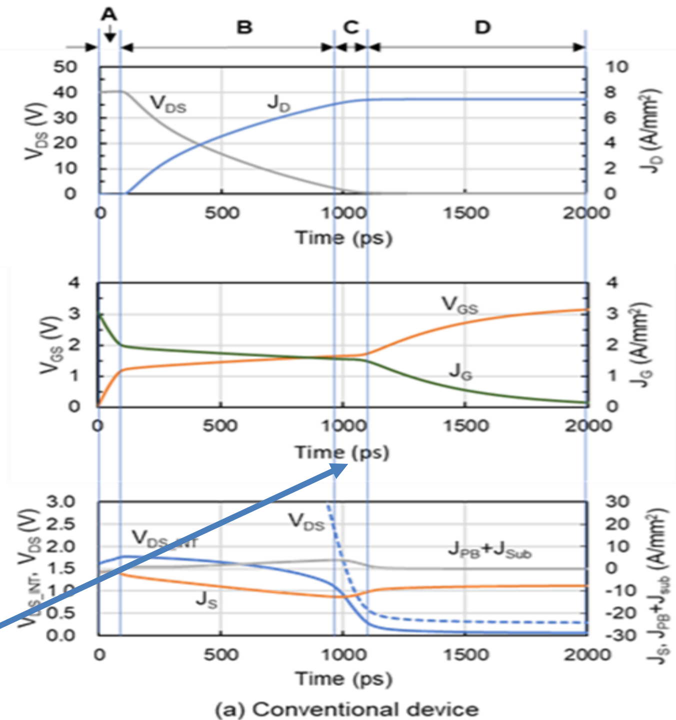
(**Long, intense Miller effect**)

Discharging C_D

Turn-On Simulation Results (Region C)

Conventional device





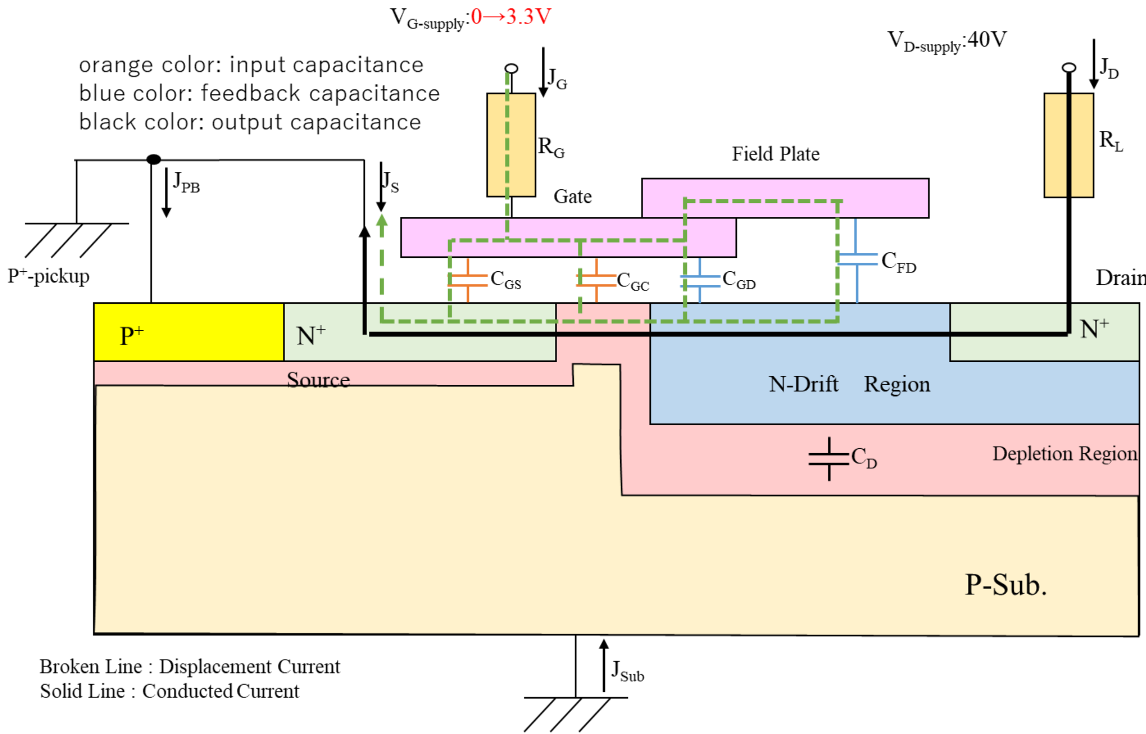
Region C

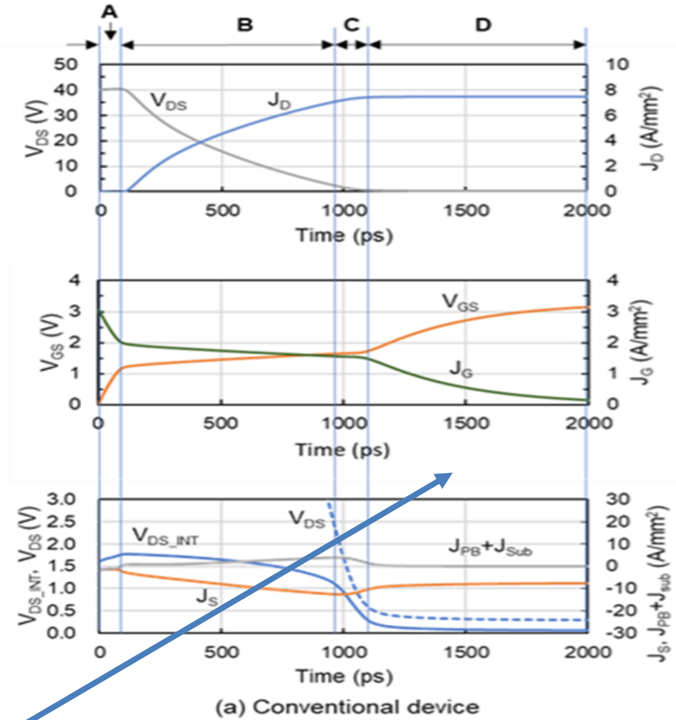
In gate plateau state
Disappearance of RESURF effect

Steep decrease in V_{DS_INT}

Turn-On Simulation Results (Region D)

Conventional device



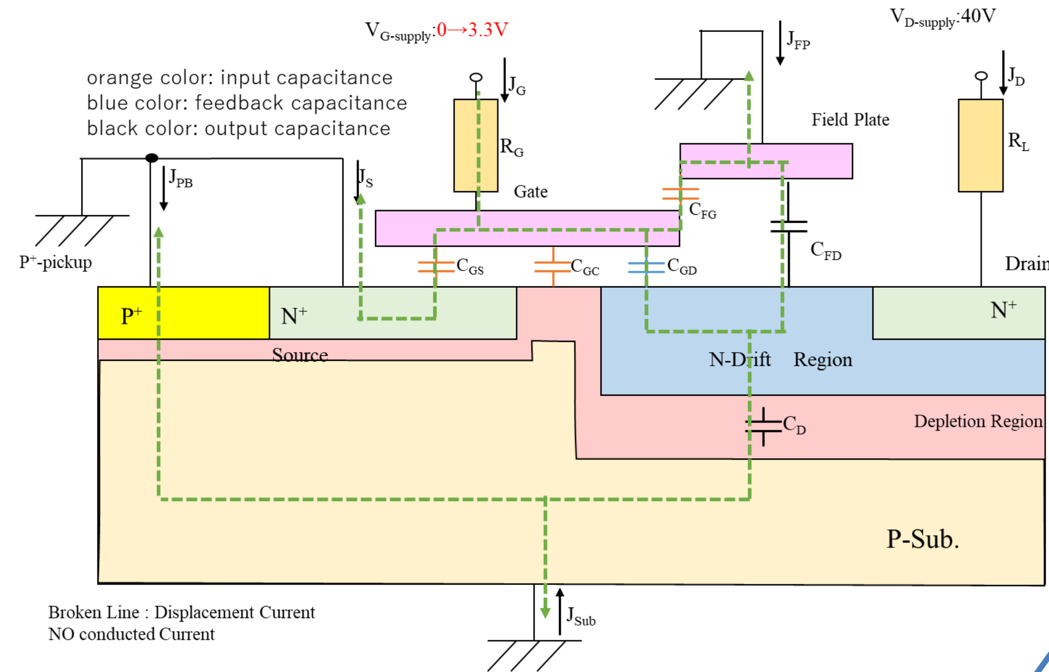


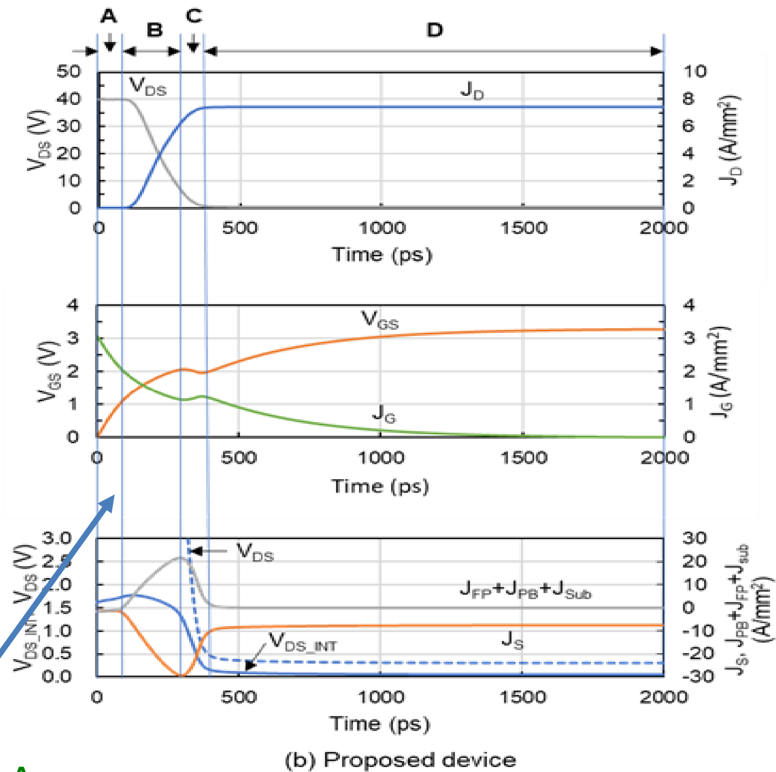
Region D

In on-state

Turn-On Simulation Results (Region A)

Proposed device





(b) Proposed device

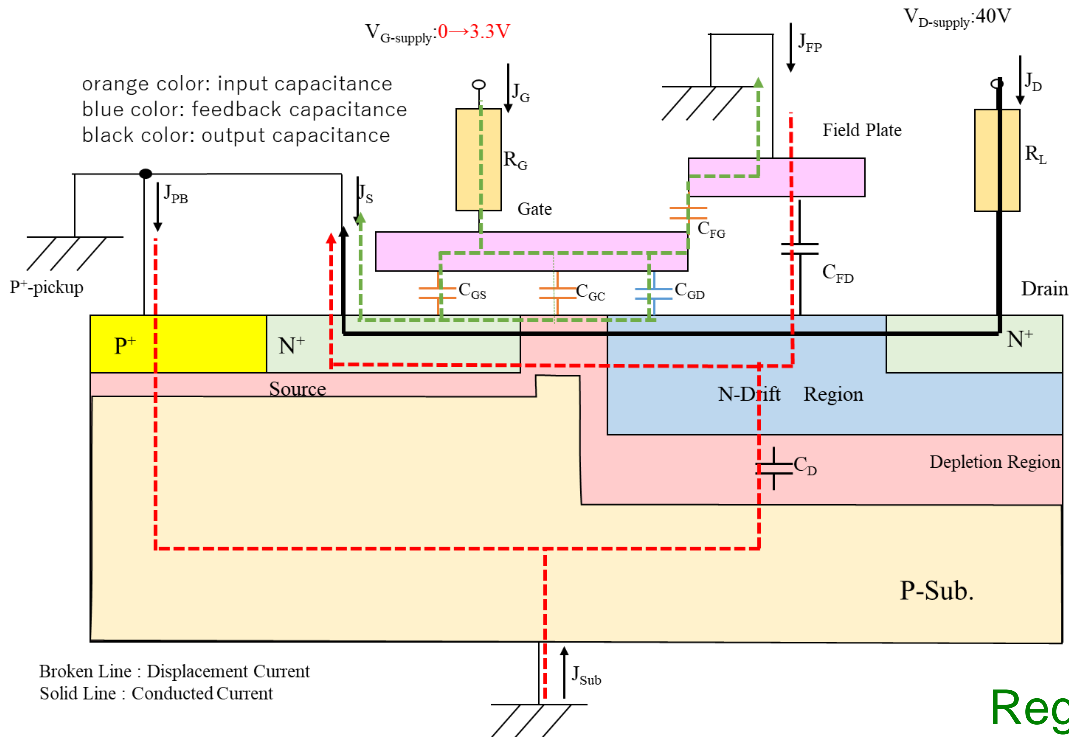
Region A

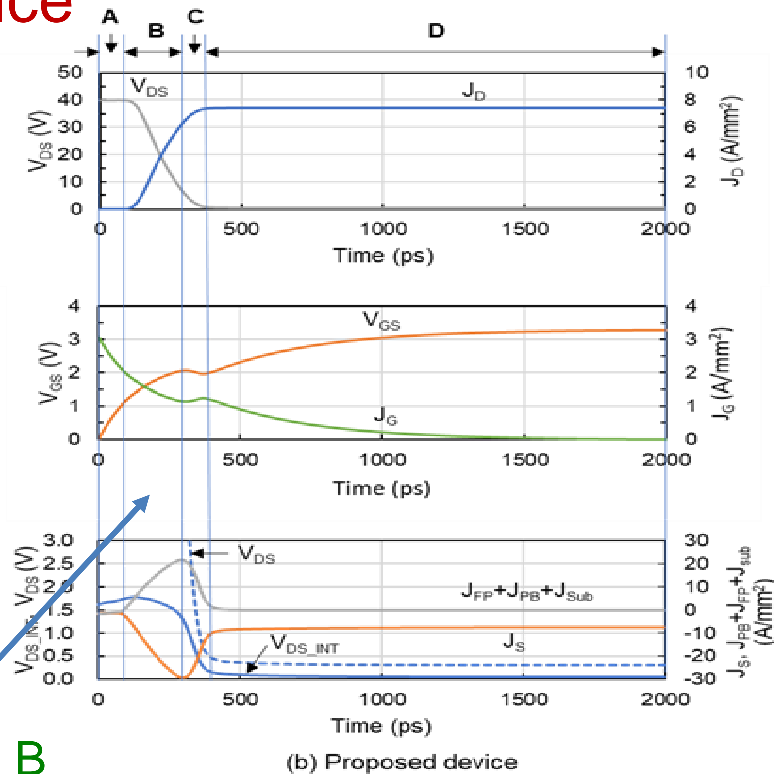
$V_{GS} < V_T$ ⇒ in off-state

Charging
- input capacitance($C_{GS}+C_{FG}$),
- feedback capacitance(C_{GD}),
- output capacitance(C_D+C_{FD})

Turn-On Simulation Results (Region B)

Proposed device





Region B

Discharging C_D+C_{FD}

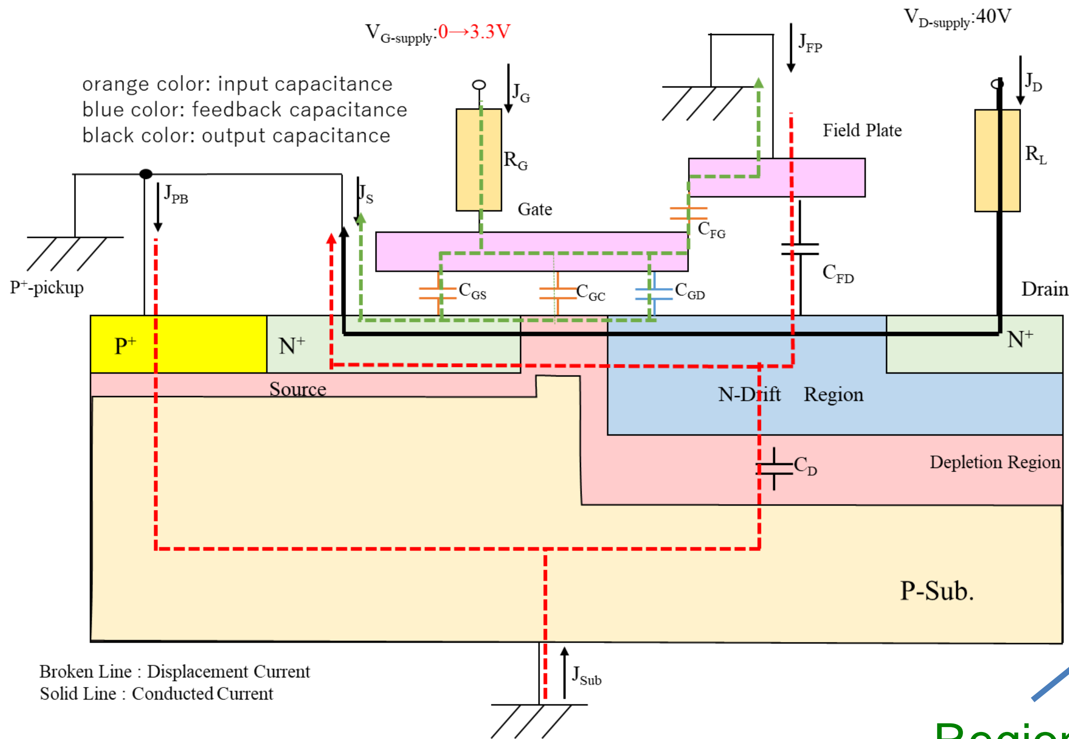
Increase in displacement current (J_{FP}+J_{PB}+J_{Sub})

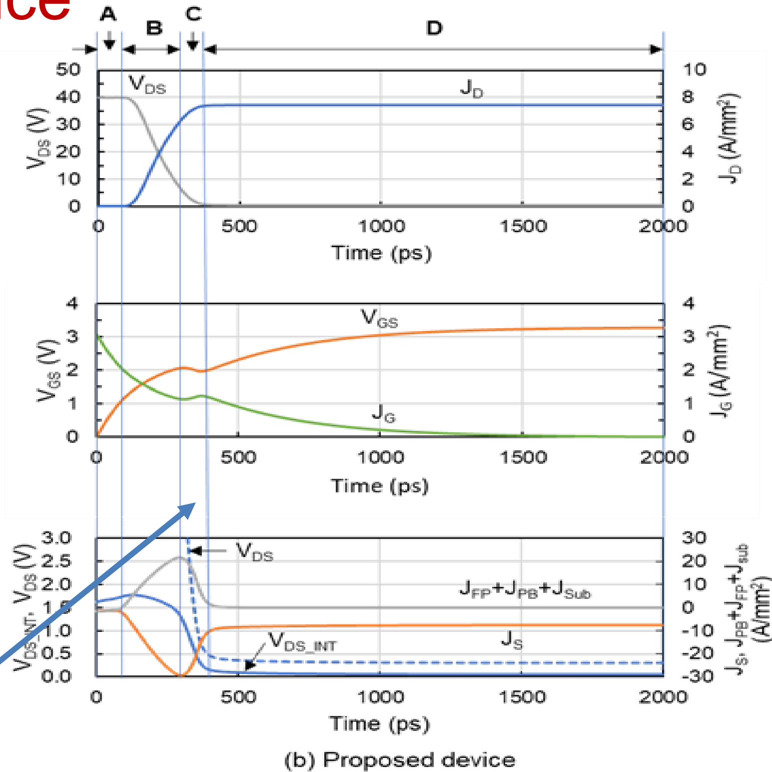
Gradual decrease in V_{DS_INT}

(**Weak Miller effect**) ☺

Turn-On Simulation Results (Region C)

Proposed device





Region C

In gate plateau state (convex-shape gate plateau state)

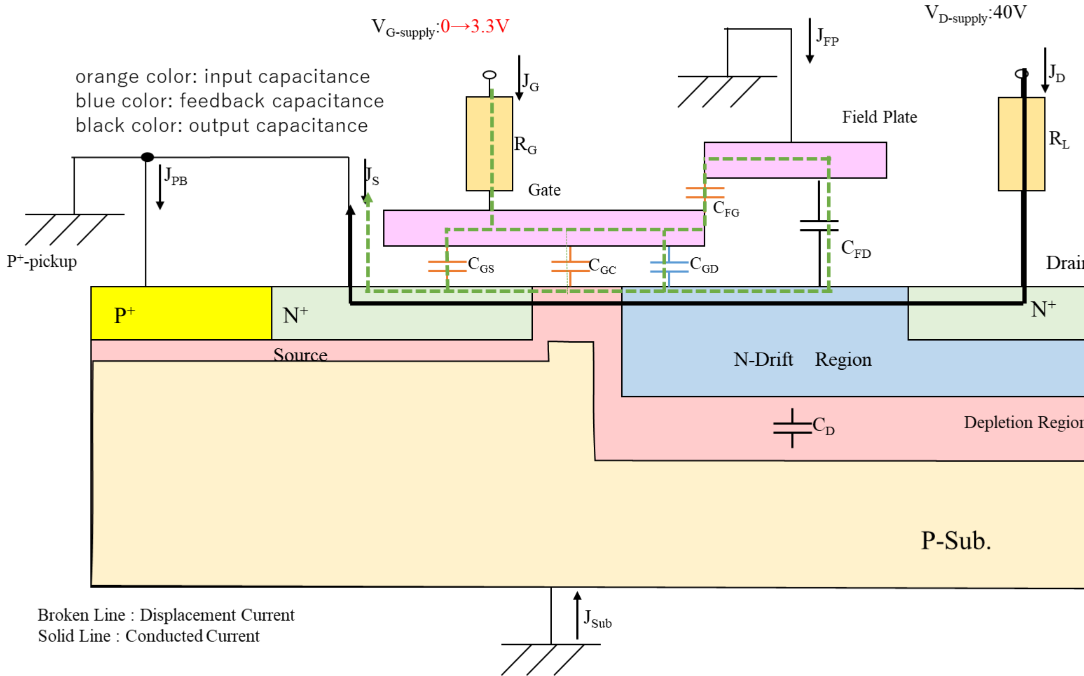
Disappearance of RESURF effect

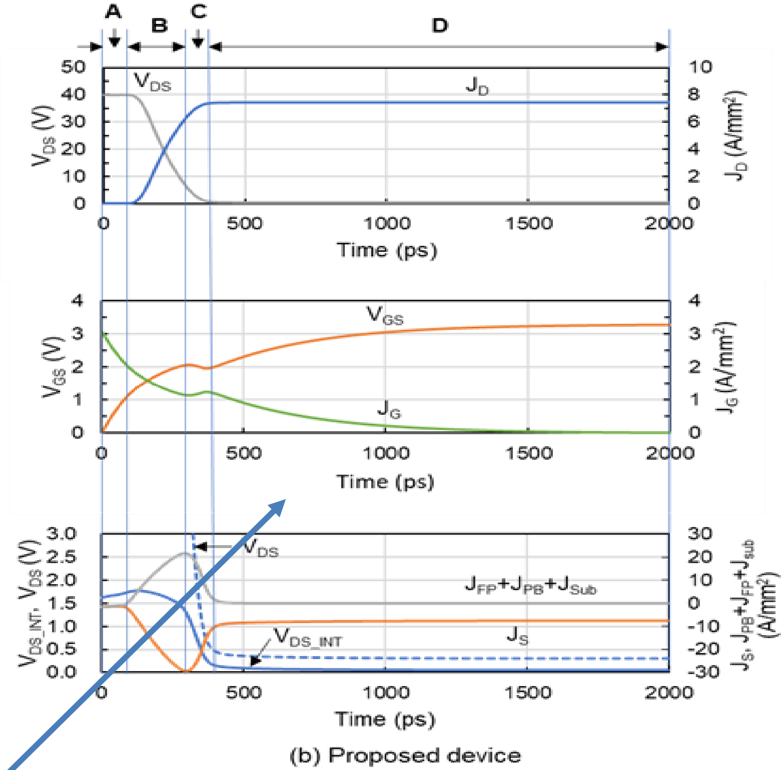
Steep decrease in V_{DS_INT}

(**Short, modest Miller effect**)

Turn-On Simulation Results (Region D)

Proposed device



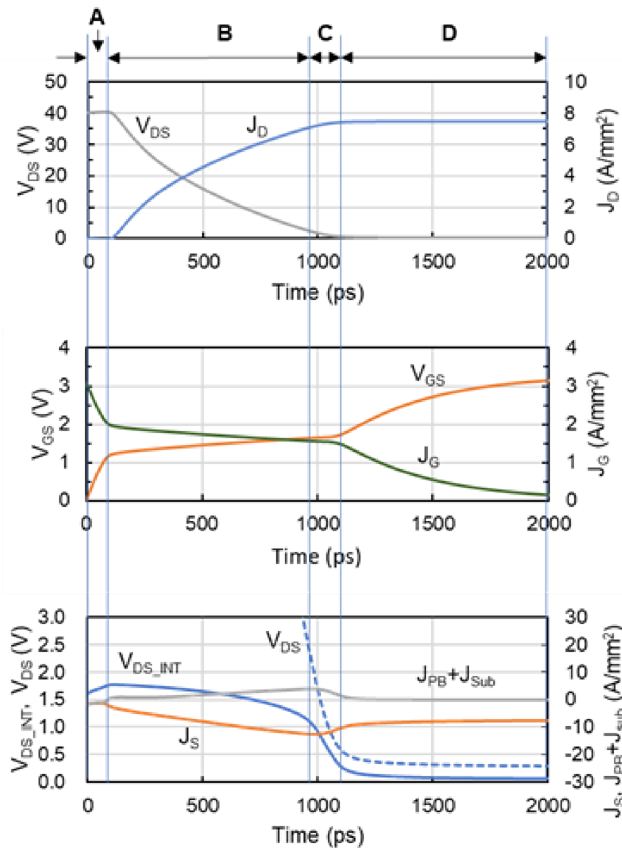


Region D

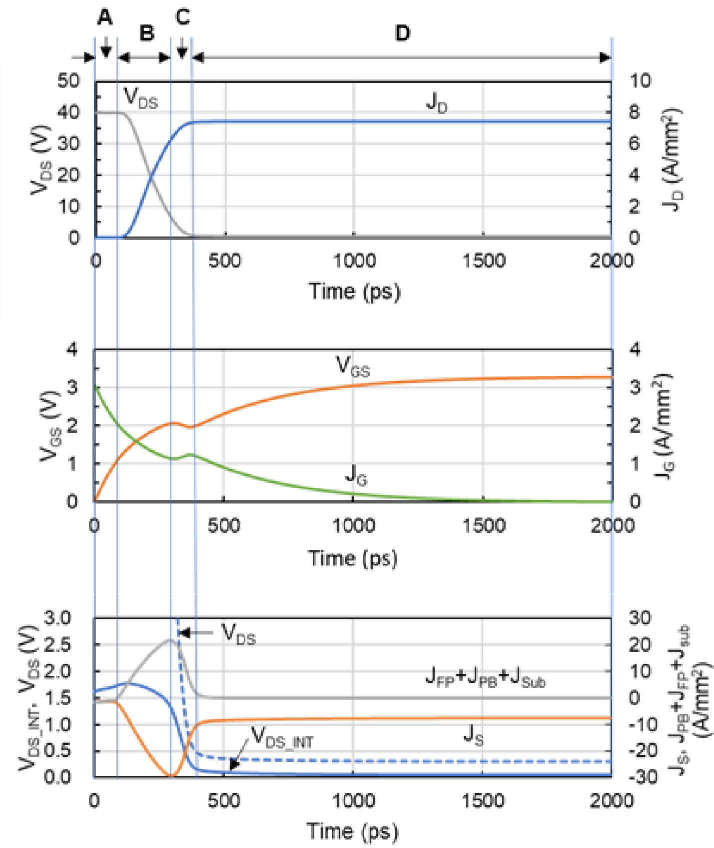
In on-state

Turn-On Simulation Results

Conventional device | Proposed device



(a) Conventional device



(b) Proposed device

Turn-on transient behaviors
for low R_G of 1.07 Ωmm² and middle R_L of 5.33 Ωmm²
with unit LDMOS layout area of 1 mm².

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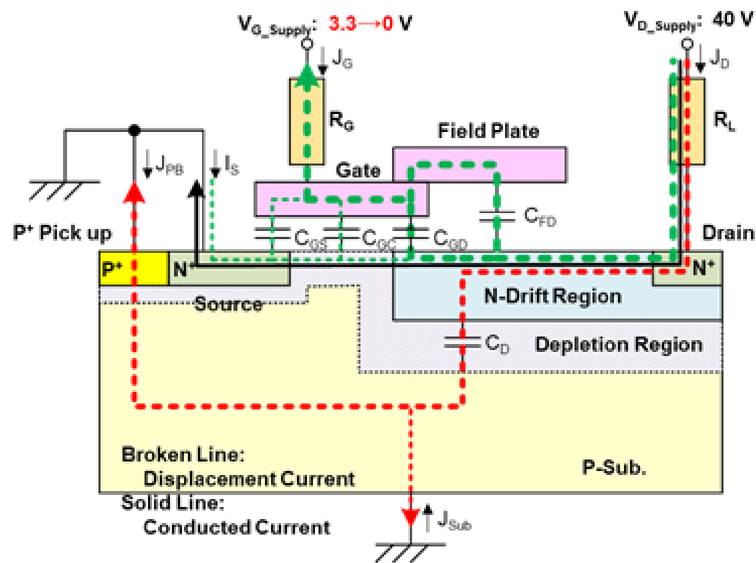
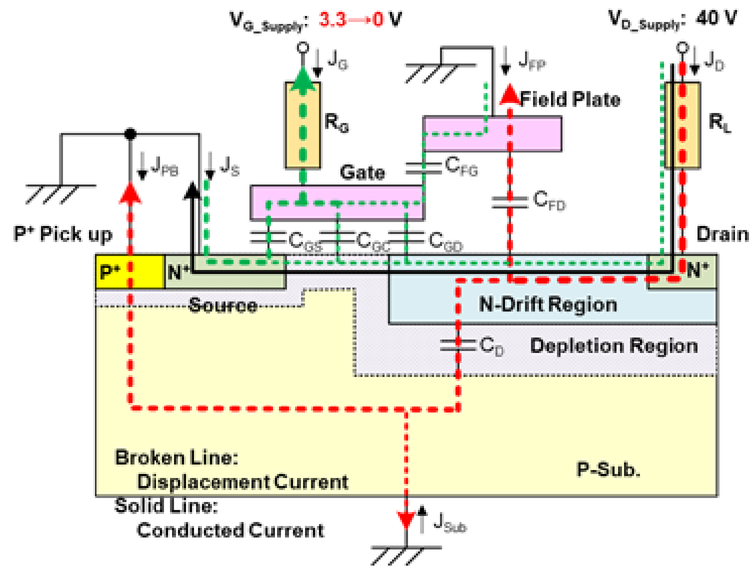
Turn-Off Behaviors

Conventional device

Proposed device



(a) Conventional device



(b) Proposed device

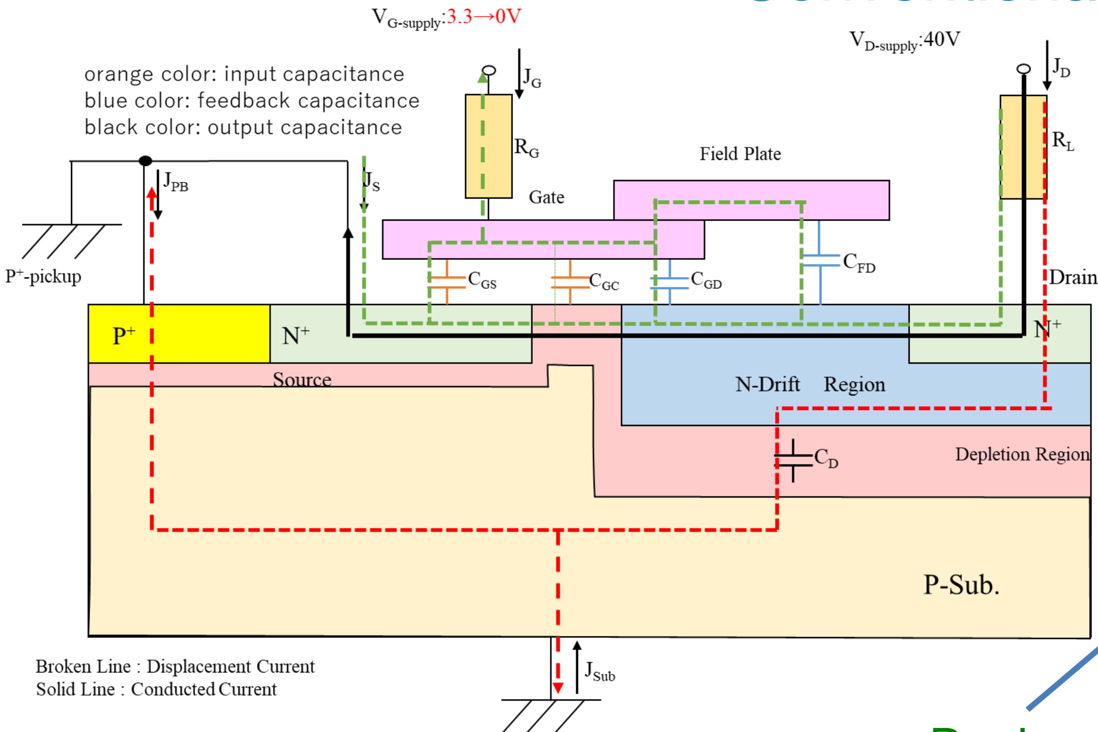
Current paths for turn-off process when $V_{GS} > V_T$.

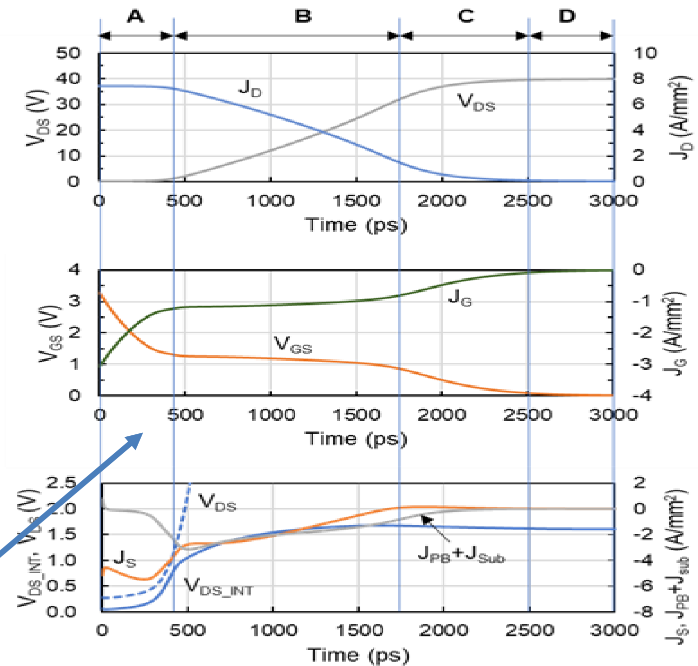
Parasitic capacitances in LDMOS transistors.

Capacitance	Conventional	Proposed
Input capacitance	$C_{GS}+C_{GC}$	$C_{GS}+C_{GC}+C_{FG}$
Feedback capacitance	$C_{GD}+C_{FD}$	C_{GD}
Output capacitance	C_D	C_D+C_{FD}

Turn-Off Simulation Results (Region A)

Conventional device





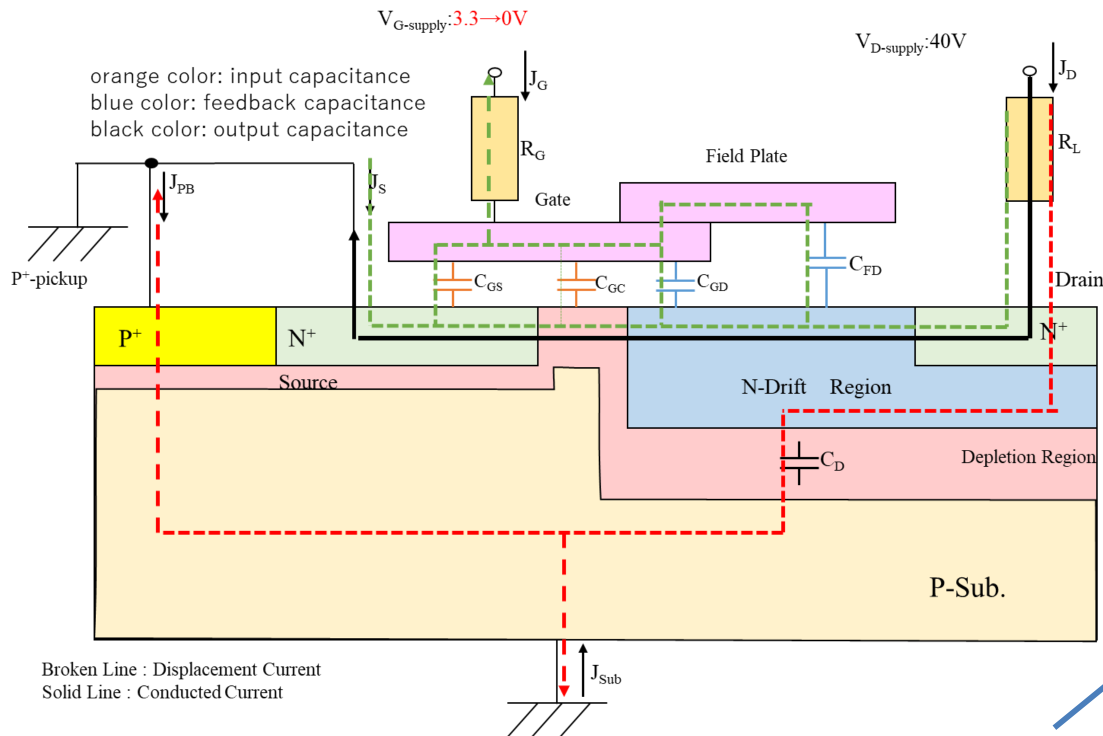
Region A

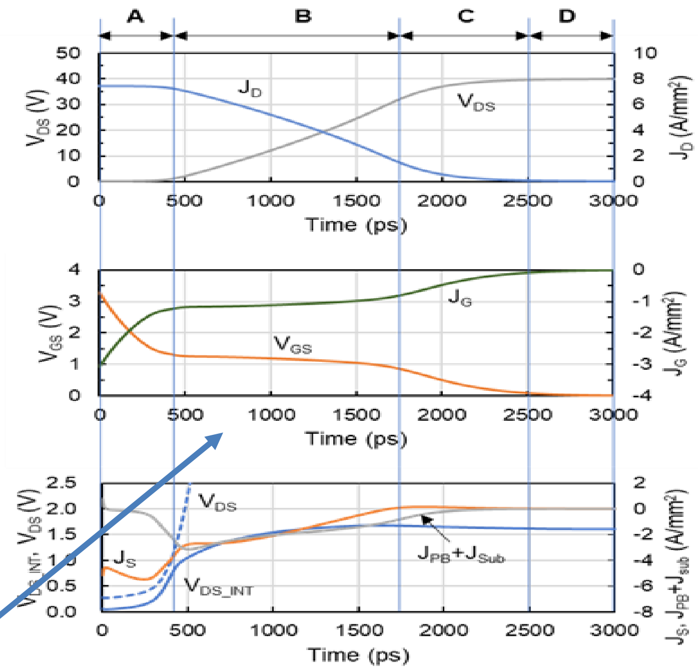
$V_{GS} > V_T$ ➡ in on-state

- Discharging
  input capacitance ($C_{GS}+C_{GC}$)
  feedback capacitance ($C_{GD}+C_{FD}$)
- Charging output capacitance (C_D)
- At end of Region A, RESURF effect occurs

Turn-Off Simulation Results (Region B)

Conventional device





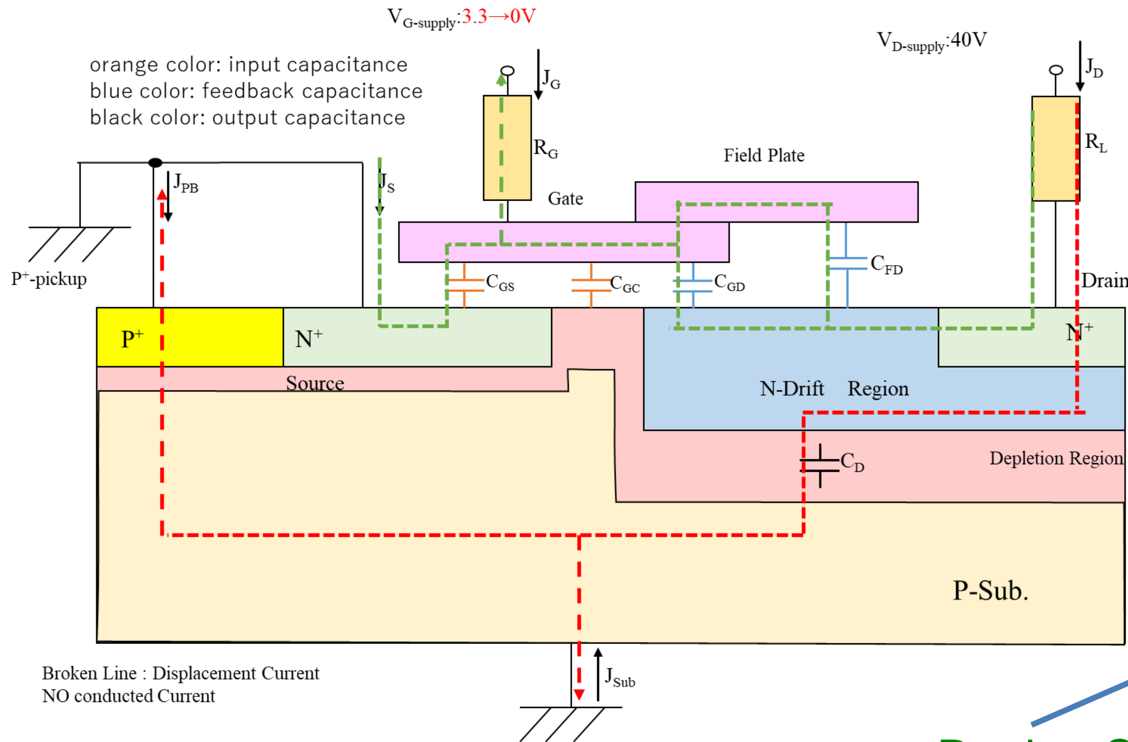
(a) Conventional device

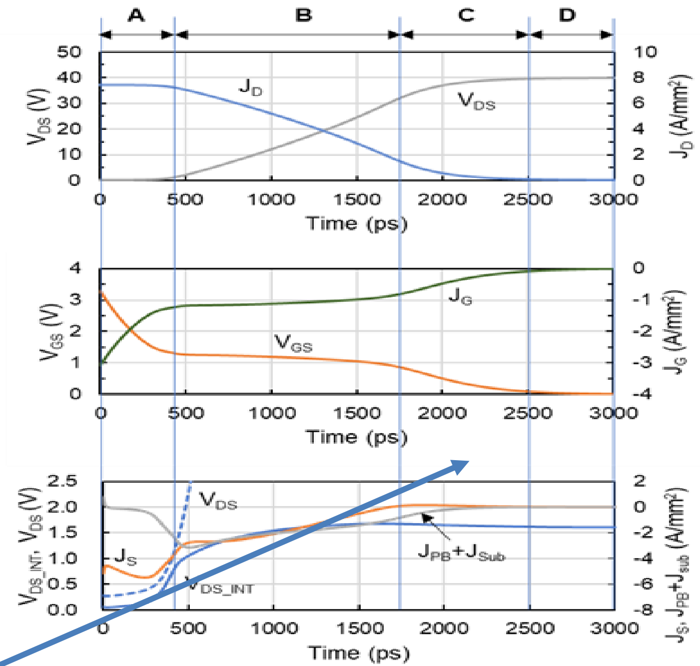
Region B

Charging C_D , $C_{GD}+C_{FD}$
In gate plateau state
(**Long, intense Miller effect**)

Turn-Off Simulation Results (Region C)

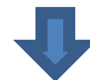
Conventional device





Region C

No source current J_S

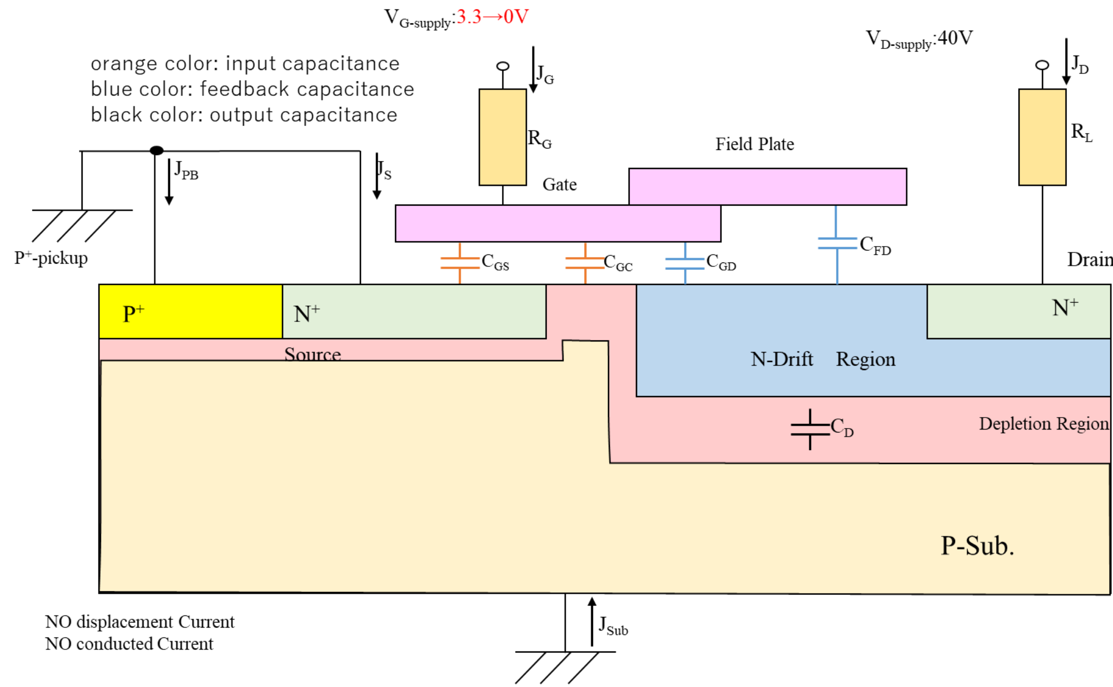


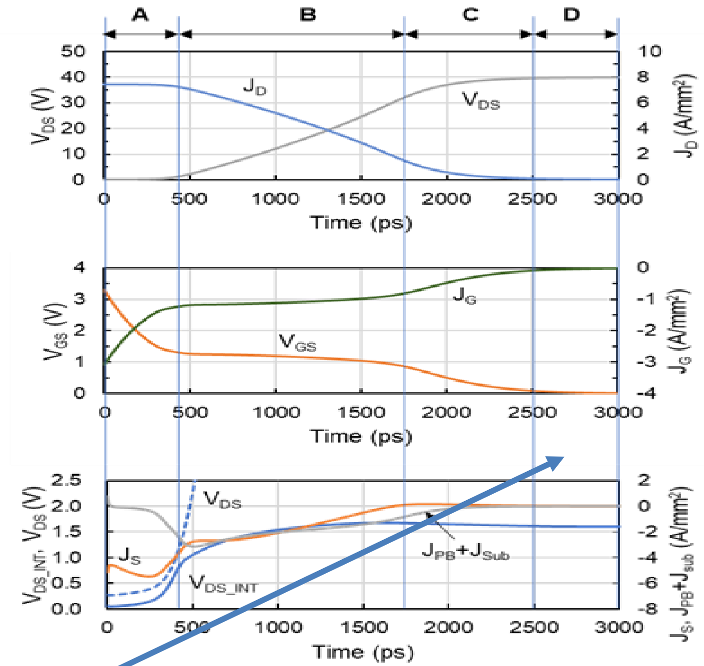
In off-state

Charging C_D, $C_{GD}+C_{FD}$

Turn-Off Simulation Results (Region D)

Conventional device





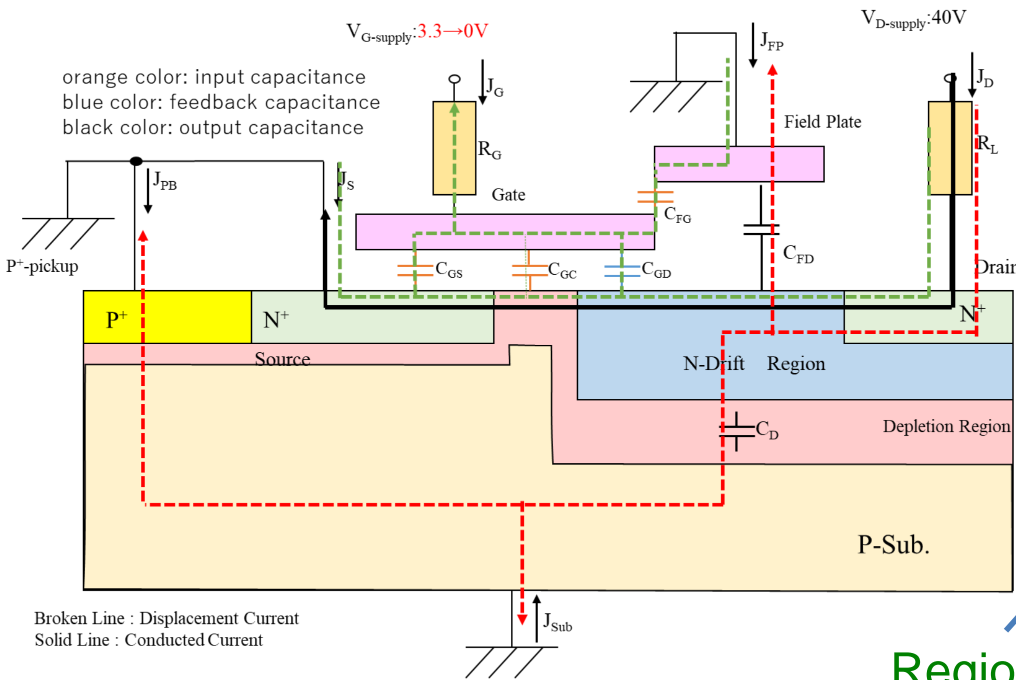
(a) Conventional device

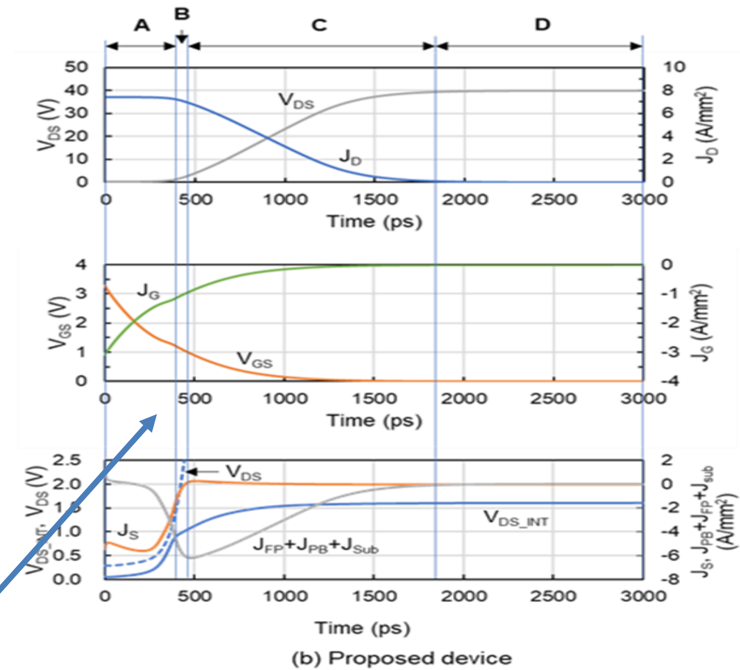
Region D

In off-state

Turn-Off Simulation Results (Region A)

Proposed device





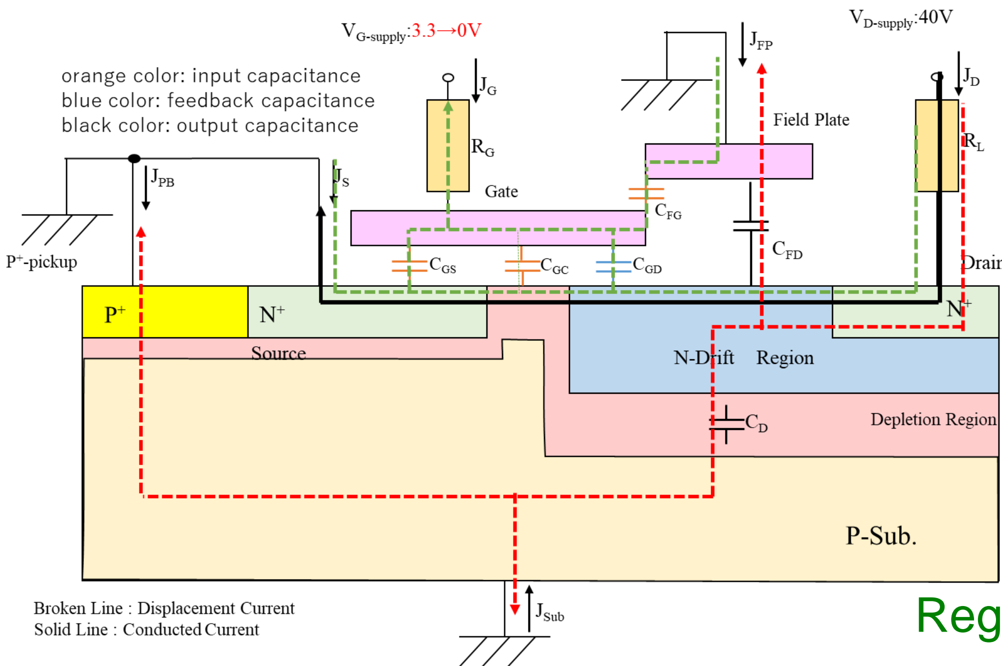
Region A

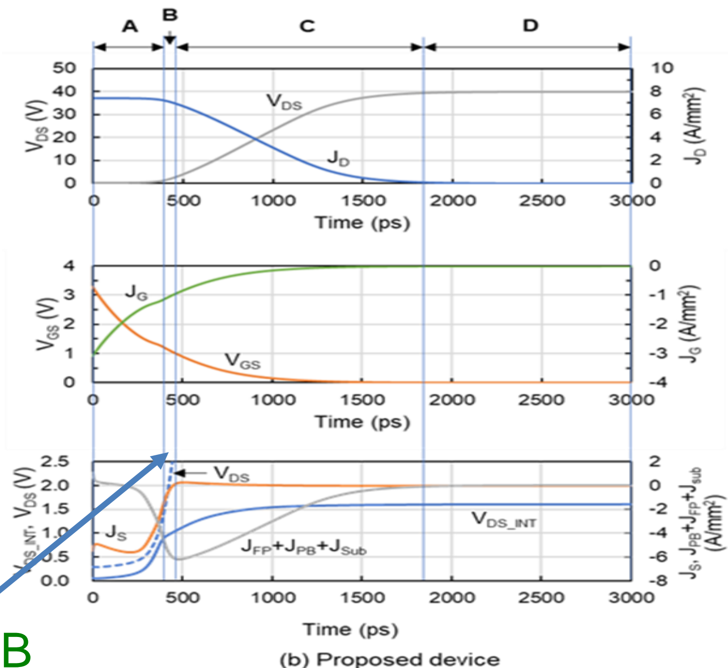
$V_{GS} > V_T$ ➡ in on-state

- Discharging
  input capacitance ($C_{GS}+C_{GC}+C_{FG}$)
  feedback capacitance (C_{GD})
- Charging output capacitance (C_D+C_{FD})
- At end of Region A, RESURF effect occurs

Turn-Off Simulation Results (Region B)

Proposed device





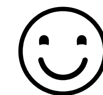
Region B

$V_{GS} \gtrsim V_T$ ⇒ at beginning of turn-off

Slight increase in V_{DS_INT}
Slight decrease in V_{GS}

⇓

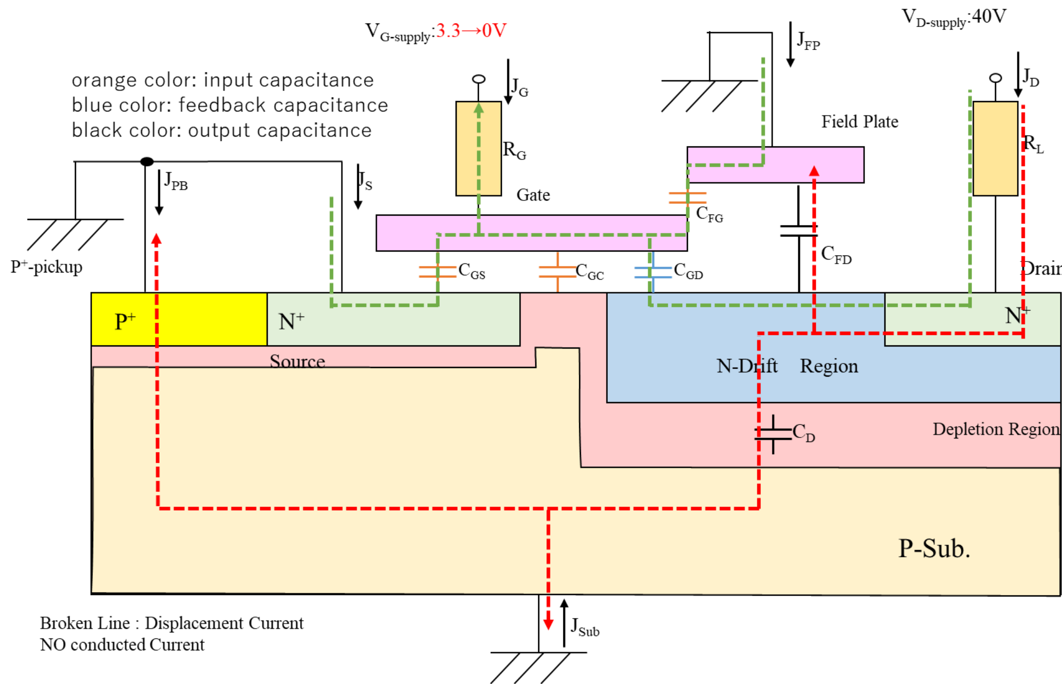
Short, weak Miller effect (no gate plateau)

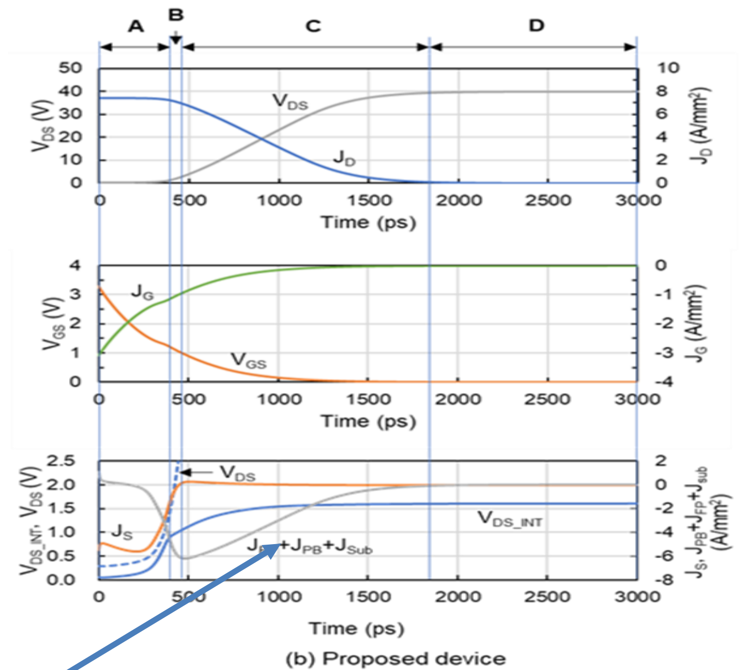


Charging output capacitance (C_D+C_{FD})

Turn-Off Simulation Results (Region C)

Proposed device





Region C

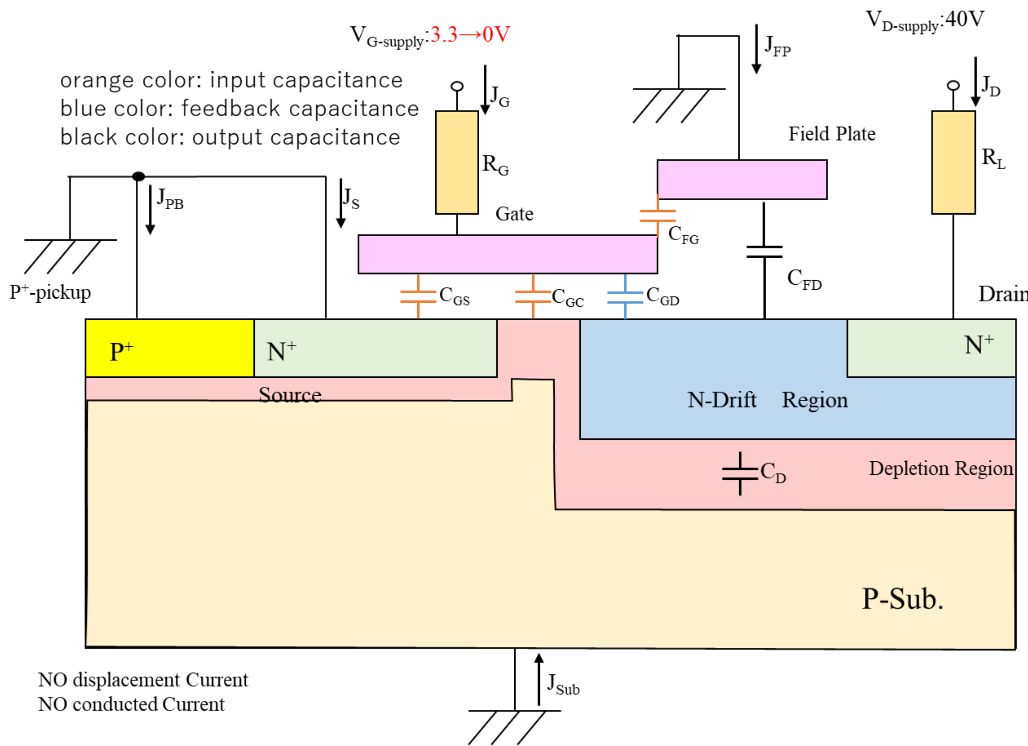
No source current J_S

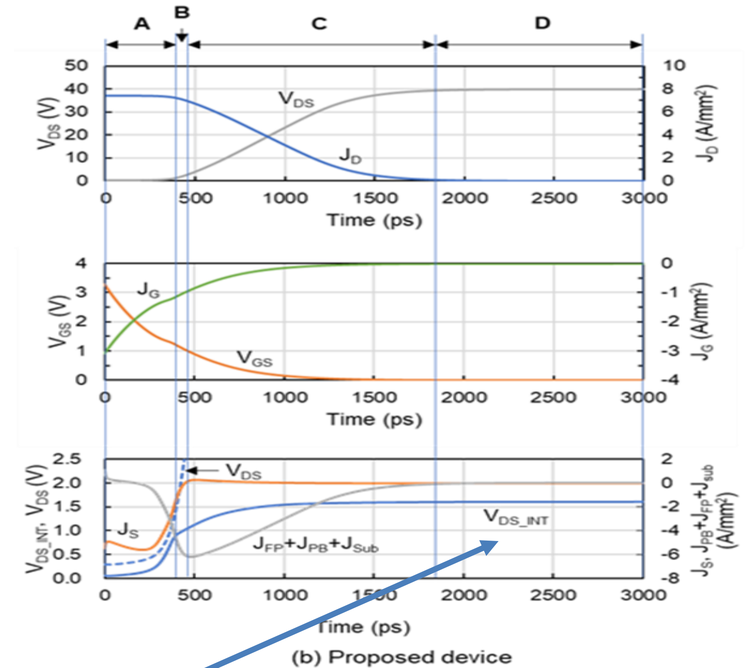
In off-state of intrinsic MOSFET

Charging C_D+C_{FD}

Turn-Off Simulation Results (Region D)

Proposed device

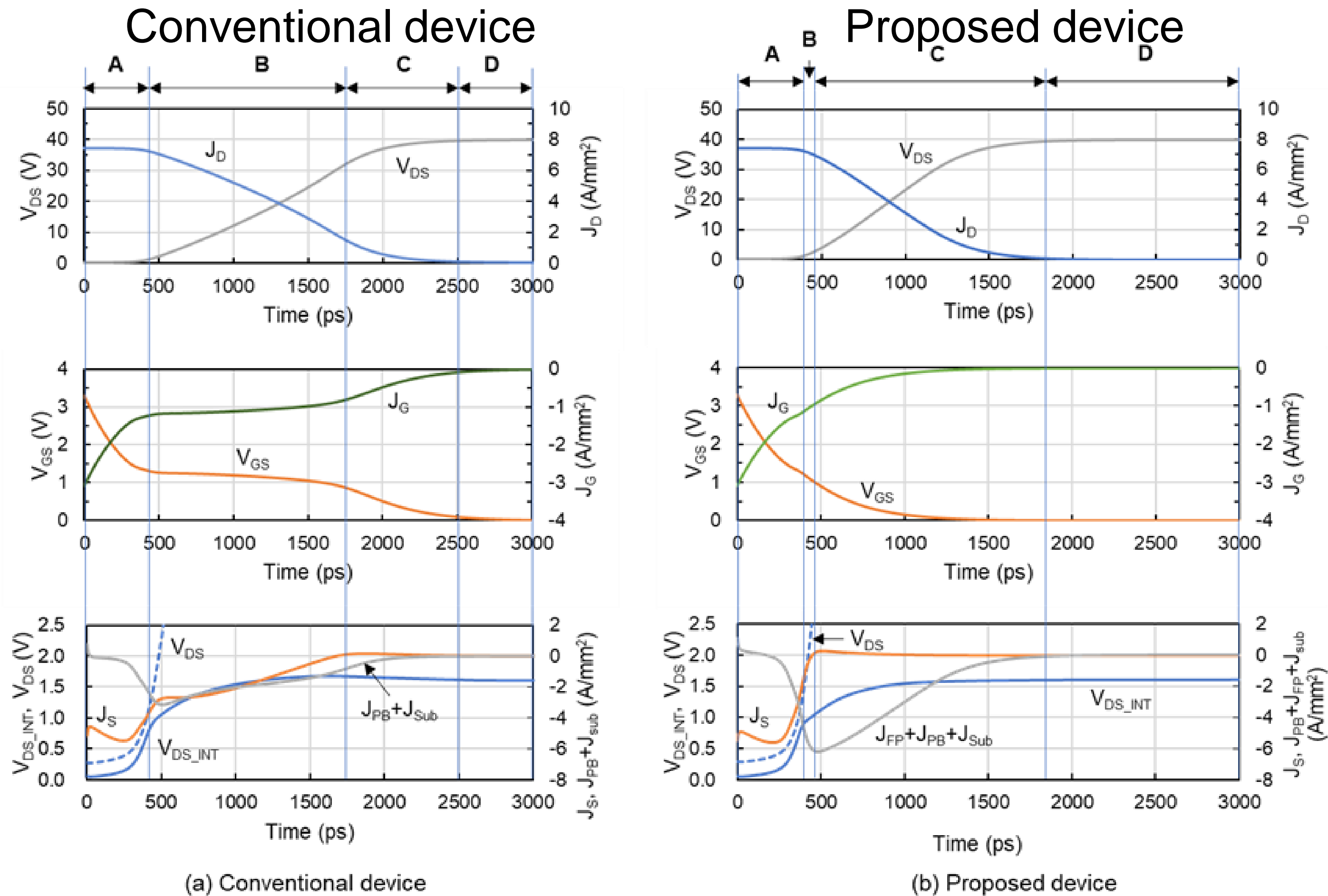




Region D

In off-state

Turn-Off Simulation Results



(a) Conventional device (b) Proposed device

Turn-off transient behaviors
for low R_G of 1.07 Ωmm² and middle R_L of 5.33 Ωmm²
with unit LDMOS layout area of 1 mm².

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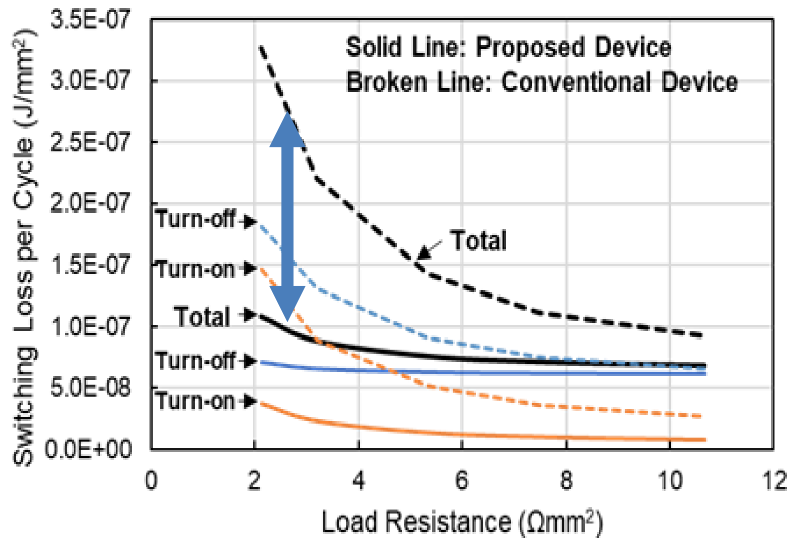
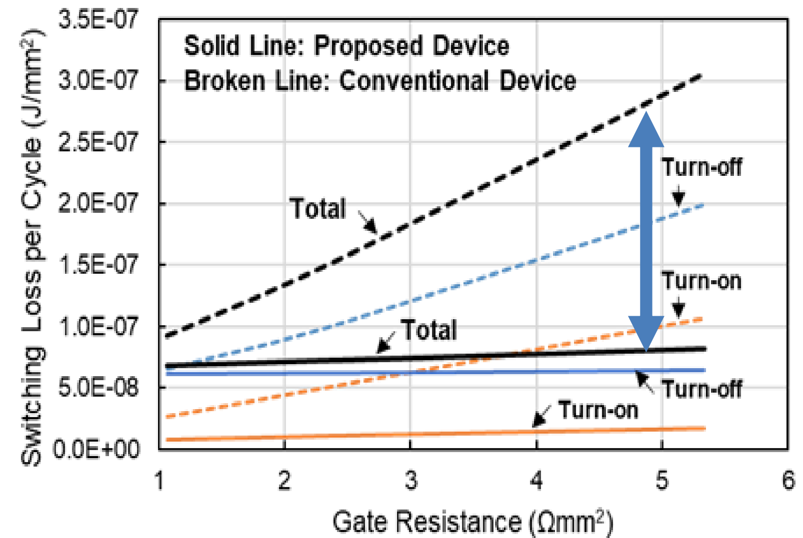
Switching Loss for R_L, R_G



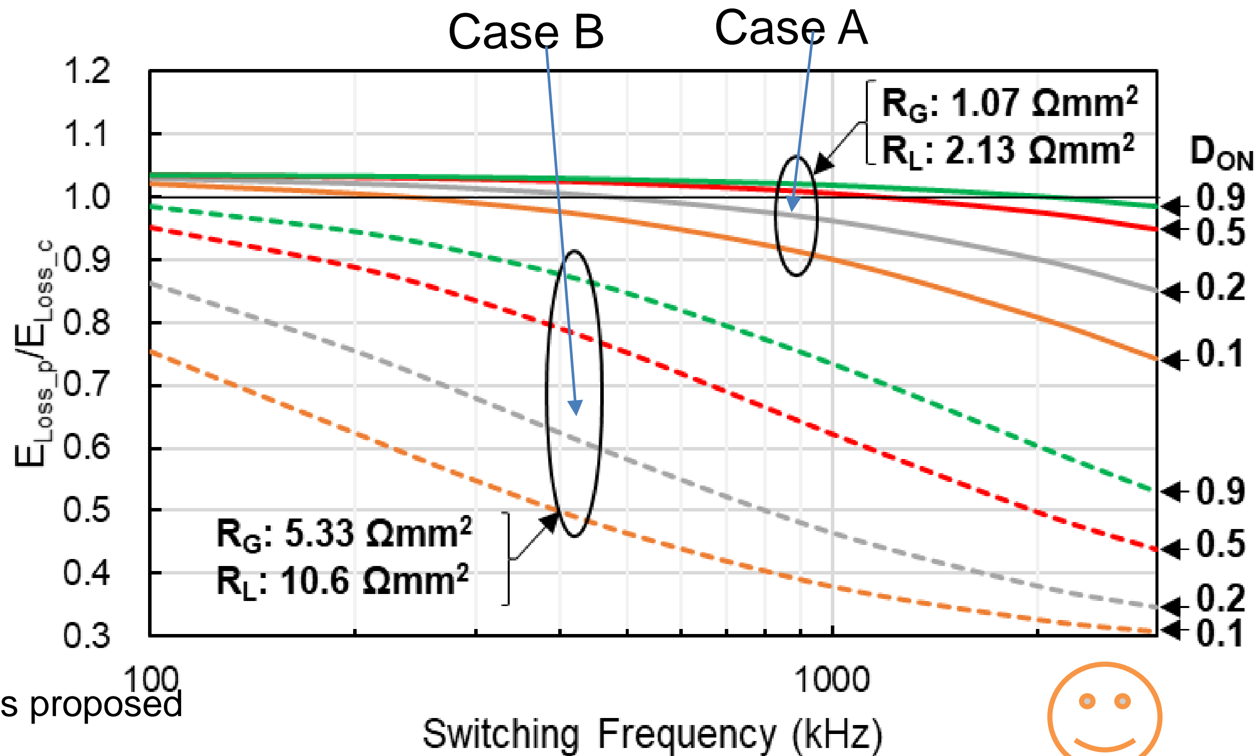
(a) Load Resistance



(b) Gate Resistance

Dependences of switching losses of
(a) R_L under a low R_G of 1.07 Ωmm^2 (high-speed switching)
(b) R_G under a high R_L of 10.7 Ωmm^2 (light load)
at unit LDMOS layout area of 1 mm^2.

Switching Frequency Dependence



Eloss-p: energy loss proposed LDMOS transistor
Eloss-c: energy loss convebtional LDMOS transistor

Switching frequency dependence of total energy loss ratio E_{Loss_P}/E_{Loss_C} at unit LDMOS layout area of 1 mm^2

The lowest value E_{Loss_P}/E_{Loss_C} of 0.31 at f = 3 MHz, D_{ON} = 0.1

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Conclusion

- Analysis of switching characteristics of the proposed LDMOS by changing R_L and R_G
- The proposed device has considerably lower feedback capacitance (C_{GD}), although it has higher output capacitance (C_D+C_{FD}).
- Under actual use condition, this capacitance structure decreases switching loss
- The lowest value of E_{Loss_P}/ E_{Loss_C} is 0.31 at f = 3 MHz, D_{ON} = 0.1.

The proposed device promises
drastically low switching loss under actual use condition.

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- Acknowledgements

Acknowledgments

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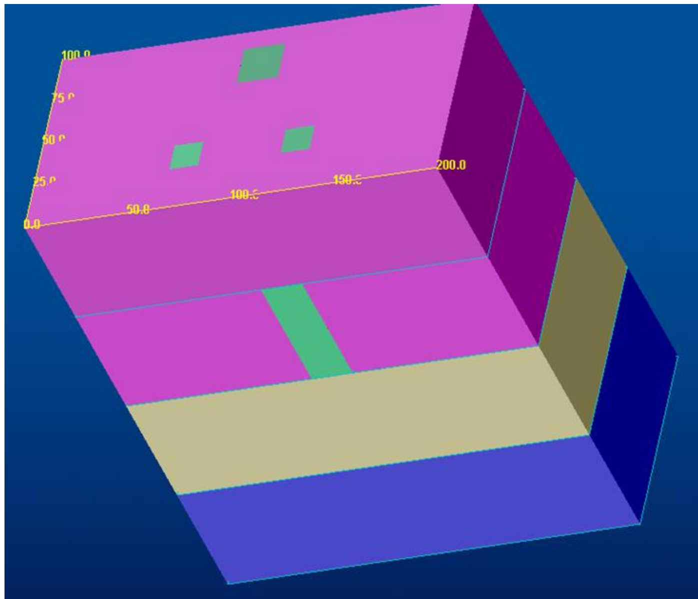

Thank you for your listening