2021 International Test Conference

Summing Node and False Summing Node Methods : Accurate Operational Amplifier AC Characteristics Testing without Audio Analyzer

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Research Objectives

- **Summing Node Method:**

  Operational Amplifier Mass Production Test

  - AC characteristics
  - High-accuracy
  - Low cost without audio analyzer

- **False Summing Node Method:**
  - To avoid oscillation and instability of video band operational amplifier under test

Outline

- Research Background
- Principle and Theory
  - Summing node method
  - False summing node method
- Simulations
  - Inverting amplifier circuit
  - Non-inverting amplifier circuit
- Experiments
- Conclusions

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Research Background

Mass production test of operational amplifier

AC characteristics (distortion, THD+N, SNR)

- **Conventional method**

▪ Accuracy

▪ Cost
▪ Test time

audio analyzers(Apx555)

Research Background

Proposal of「Summing Node Method + FFT Analysis 」

● **Usage of standard analog modules installed in ATE**

ATE:Automated Test Equipment

・Low cost
- short testing time
- without expensive measurement instrument

・High accuracy
- equivalent to audio analyzer

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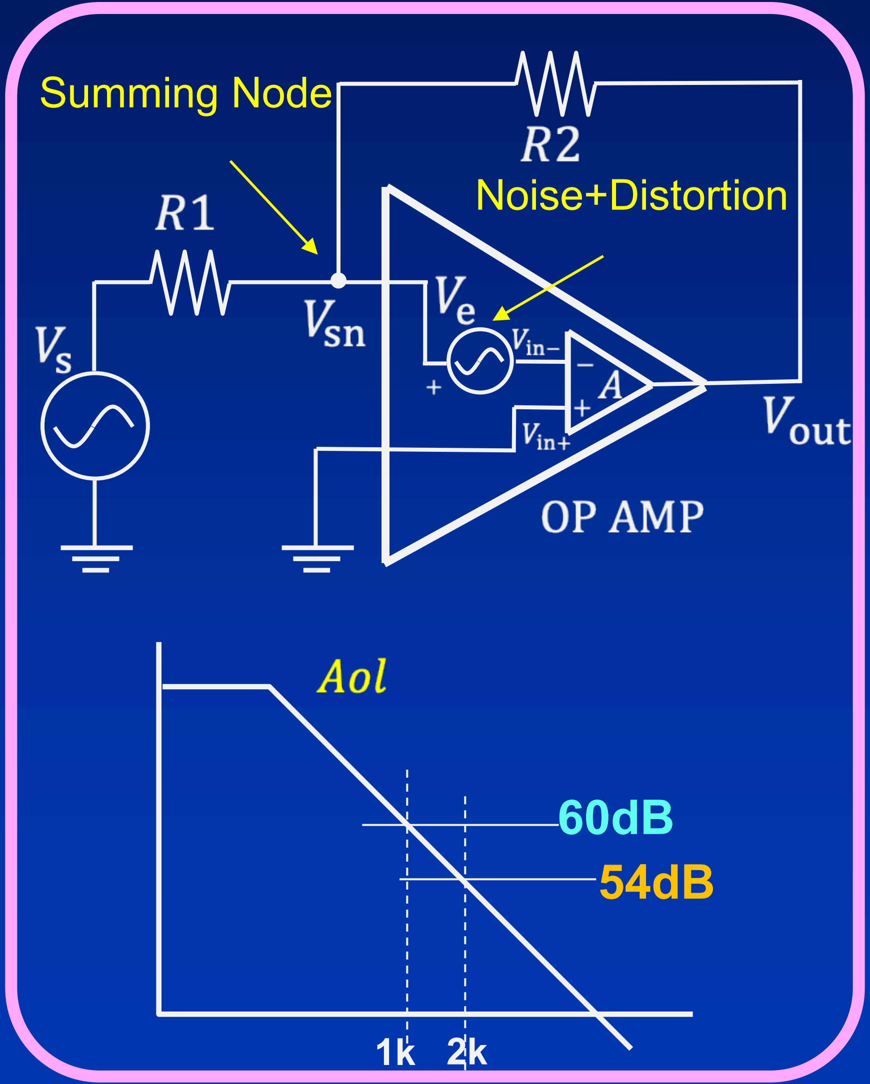
Summing Node Method



Consider noise + distortion components at summing node *V*sn by separating signal source origin and DUT origin ones

Signal Source Origin

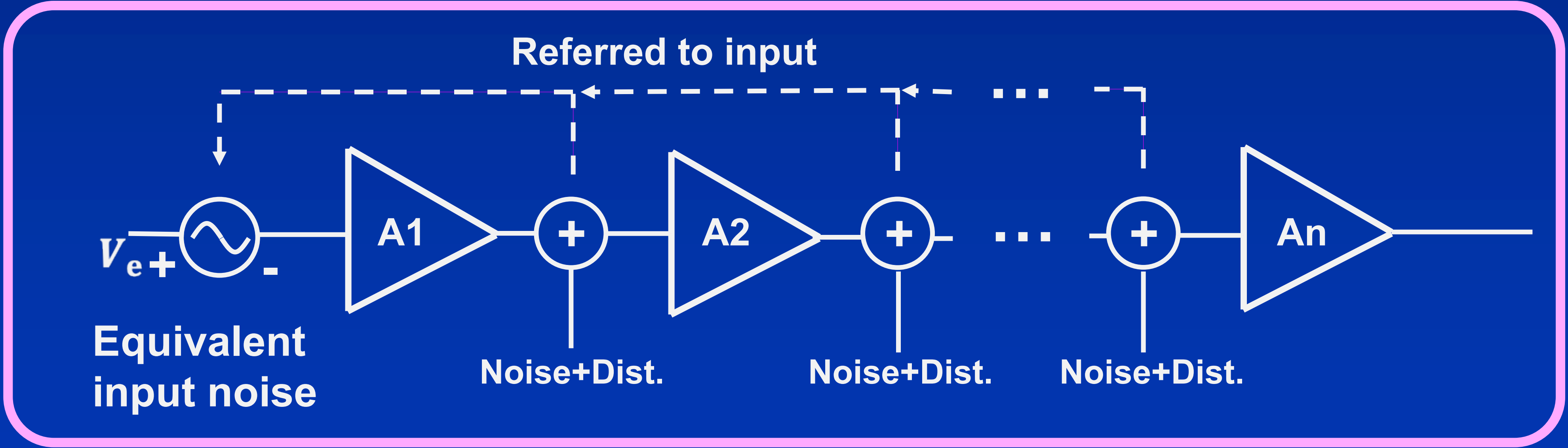
- Fundamental ⇒ compressed by 60dB
  HD2 ⇒ compressed by 54dB

In case signal source has -80dBc distortion(HD2)
⇒ compressed to -134dBc at *V*sn

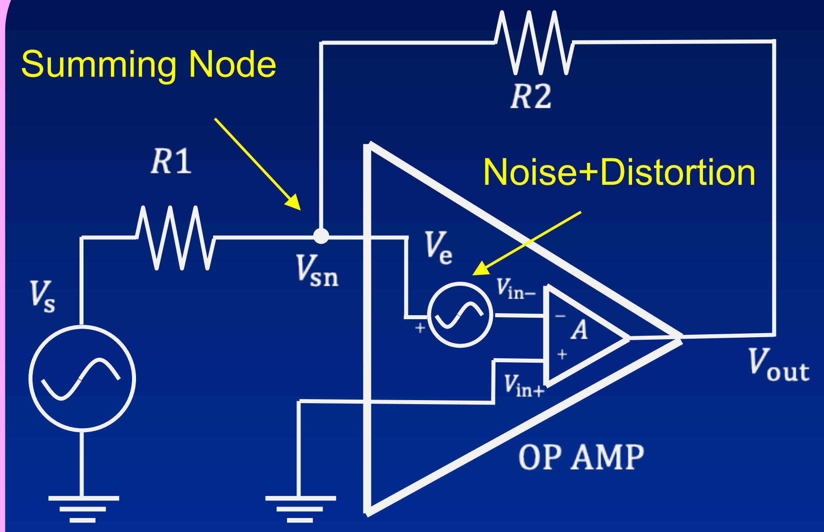
Summing Node Method

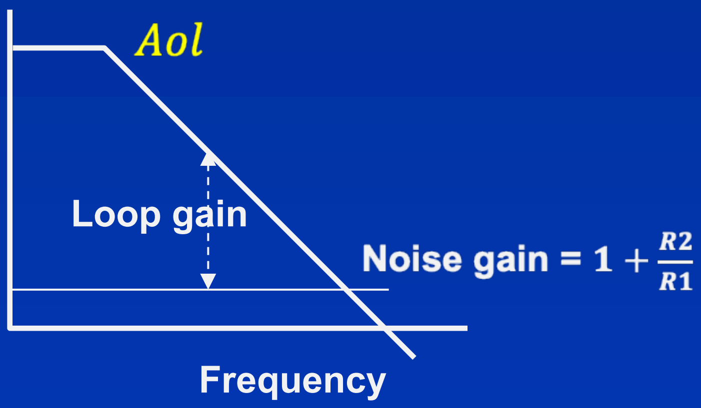
DUT origin

- Generated noise and distortion are referred to the input.
- Noise and distortion at each stage are converted to input.



Principle





In the left cirtuit

$$V_{out} = A(V_{in+} - V_{in-}) = -AV_{in-}$$

$$V_{sn} = V_e + V_{in-} = V_e - \frac{V_{out}}{A}$$

Partial pressure, superimposition

$$V_{sn} = V_s + \frac{R_1}{R_1 + R_2}(V_{out} - V_s)$$

$$= \frac{R_1}{R_1 + R_2} V_{out} + \frac{R_2}{R_1 + R_2} V_s$$

Let A $\rightarrow \infty$ be

$$V_{out} = \boxed{\left(1 + \frac{R_2}{R_1}\right)} V_e - \frac{R_2}{R_1} V_s$$

Noise gain

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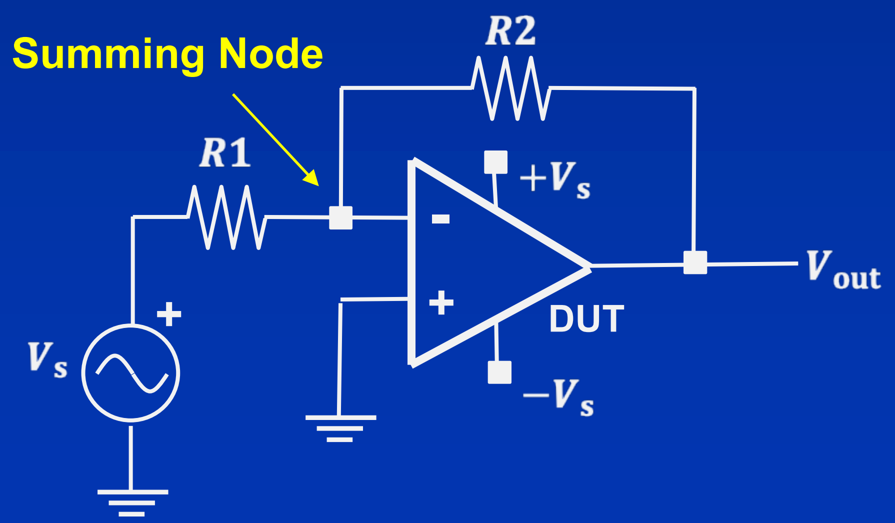
False Summing Node

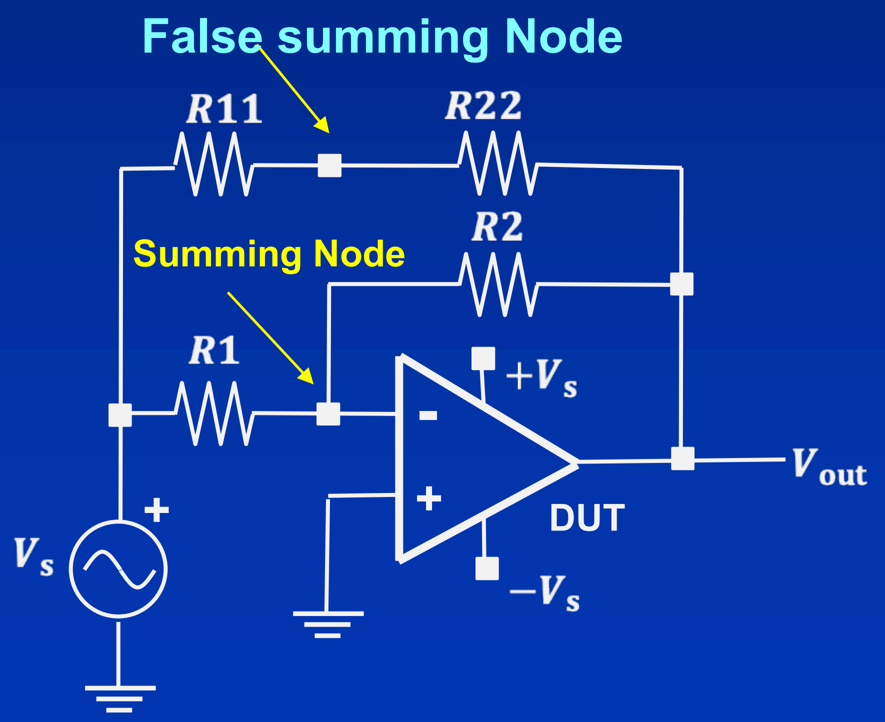
- Summing Node
  - Sensitive node to op amp characteristics

    → Not desirable to touch with observation probes. (oscillation possibility)



- False Summing Node

  Let R11=R1, R22=R2
  ⇒ Pseudo-negative feedback network



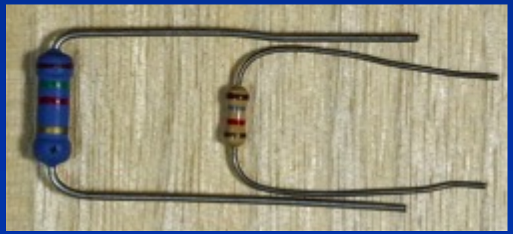
Resistor Ratios Variation Effect

Concerns with False Summing Node

- Error effect between
  feedback resistors ratio and pseudo-feedback resistors ratio

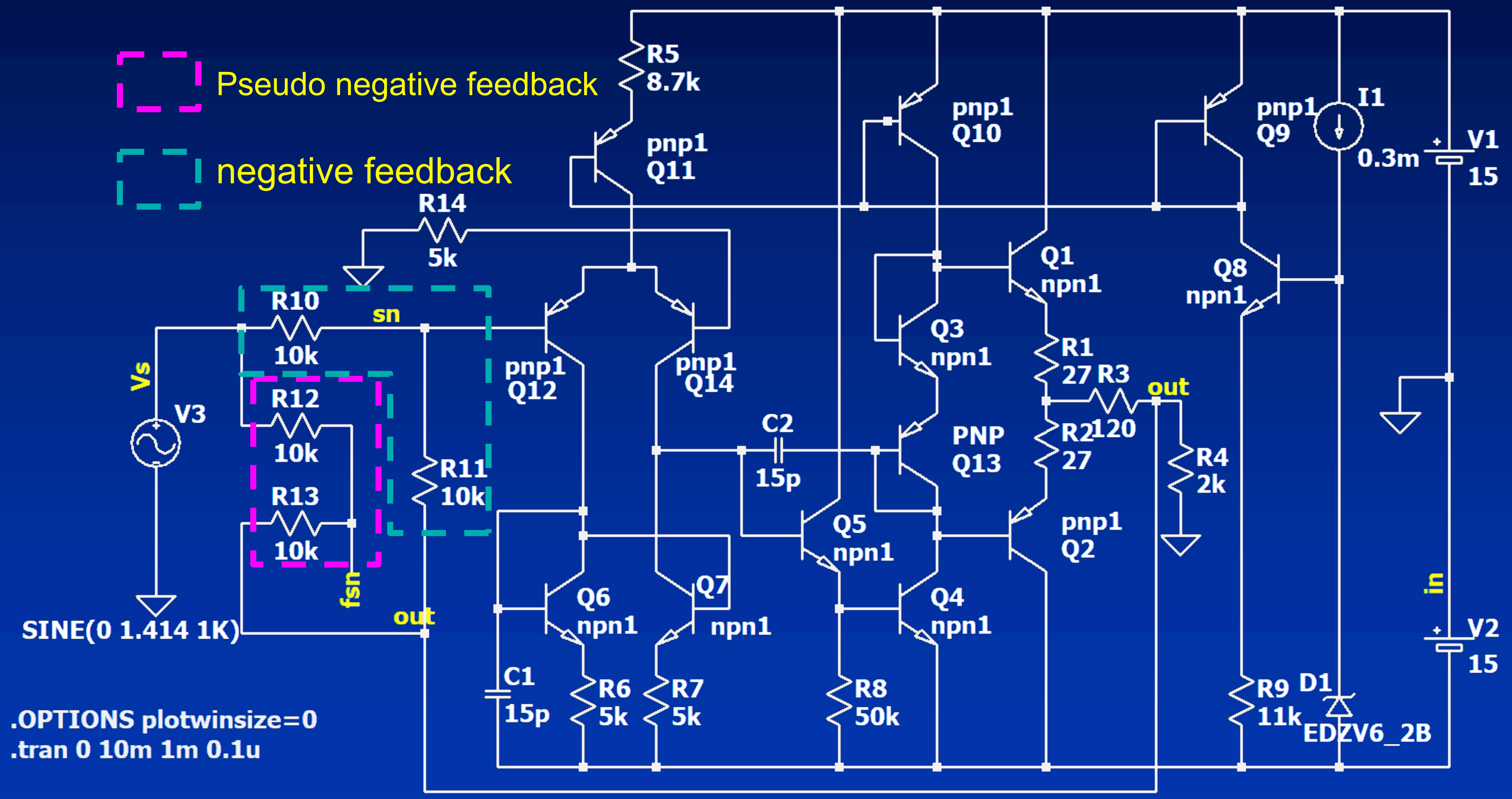
Specified Resistance Variation

- Excellent ±0.05%
- General ±1~5%



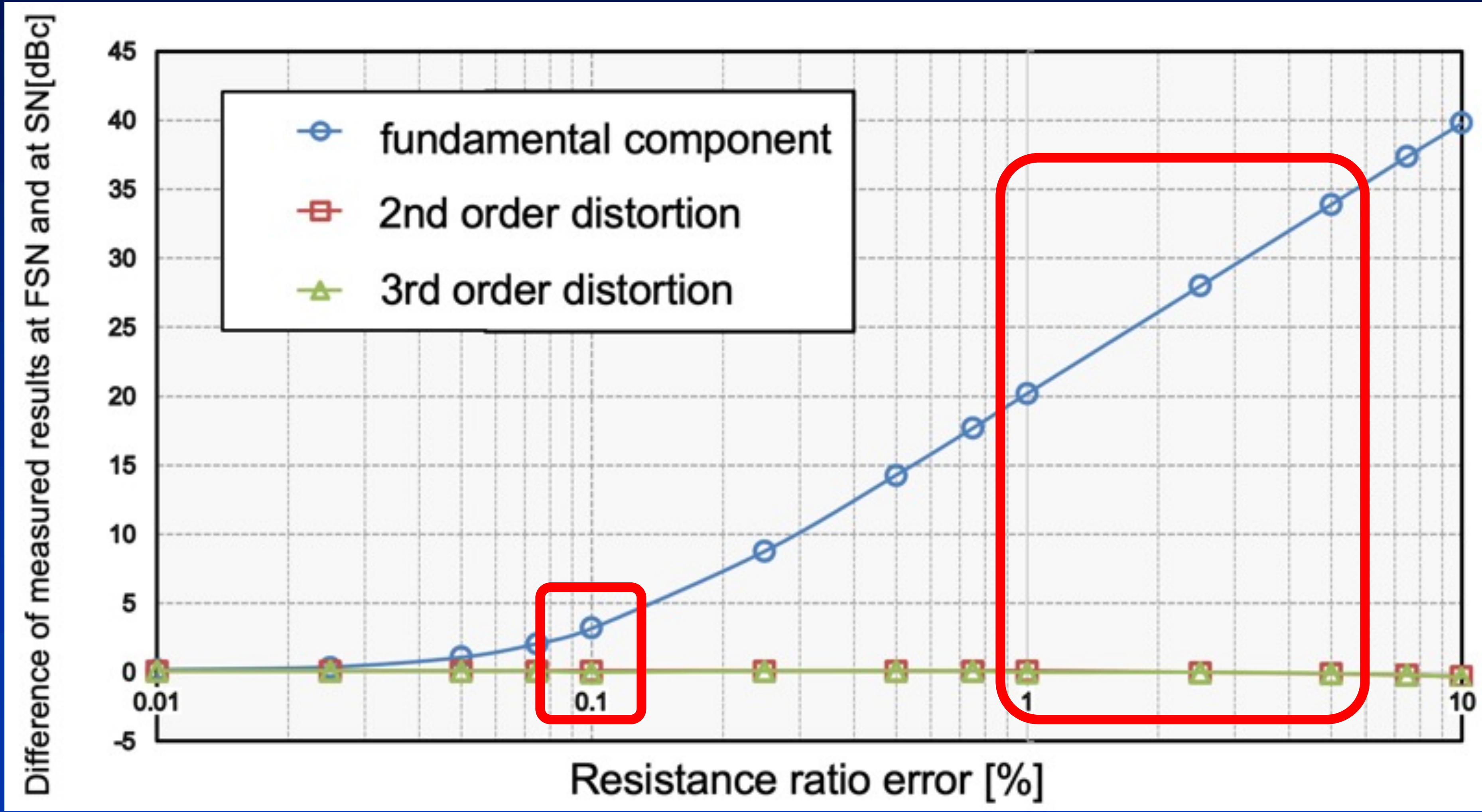
- **Each error was incorporated in simulation.**

False Summing Node Method Simulation



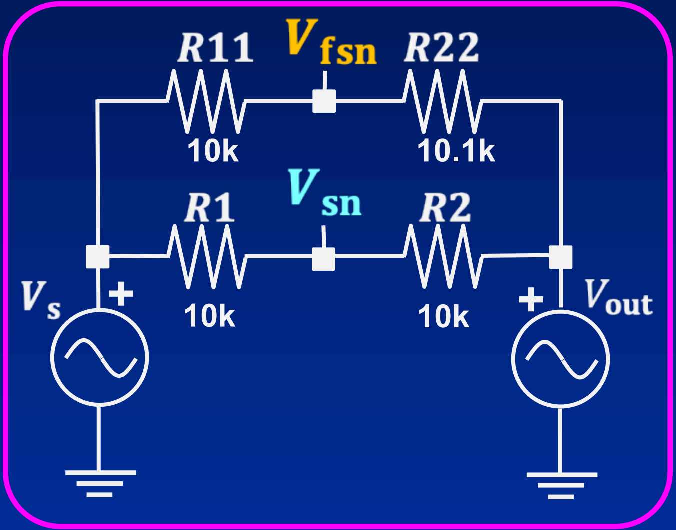
.model npn1 NPN(Is=10f Bf=120 Ikf=3 Nk=1.5 Br=2 Vaf=100 Rc=1.3 Re=50m RB=13 Cjc=5p Vjc=0.2 Mjc=0.2 Cje=12p Vje=0.75 Mje=0.33 Tr=5n Tf=500p Vceo=50 Icrating=150m)
.model pnp1 PNP(Is=10f Bf=50 Ikf=3 Nk=1.5 Br=2 Vaf=100 Rc=1.3 Re=50m RB=13 Cjc=5p Vjc=0.2 Mjc=0.2 Cje=12p Vje=0.75 Mje=0.33 Tr=5n Tf=500p Vceo=50 Icrating=150m)

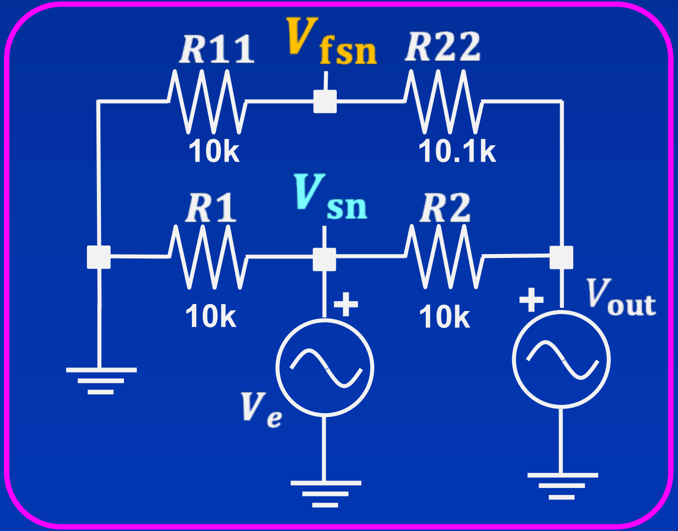
Resistors Ratio Error Effect



Negligible for HD2 and HD3 measurement with false summing node method

Resistors Ratio Error Effect on Fundamental,HD2 and HD3





Signal Source Origin

- $A_{OL} \rightarrow \infty \;\Rightarrow\; V_{sn} \rightarrow 0$
- Resistor ratio error 1%
  ⇒ -40dB (1%) signal appears at V_{fsn}

DUT Origin

- Resistor ratio error 1%
  ⇒ 1% error between V_{sn} and V_{fsn}

At V_{sn} = -120dBV (-1μV) ⇒
At V_{fsn}, 1.01μV = -119.9dBV (0.1dB error)

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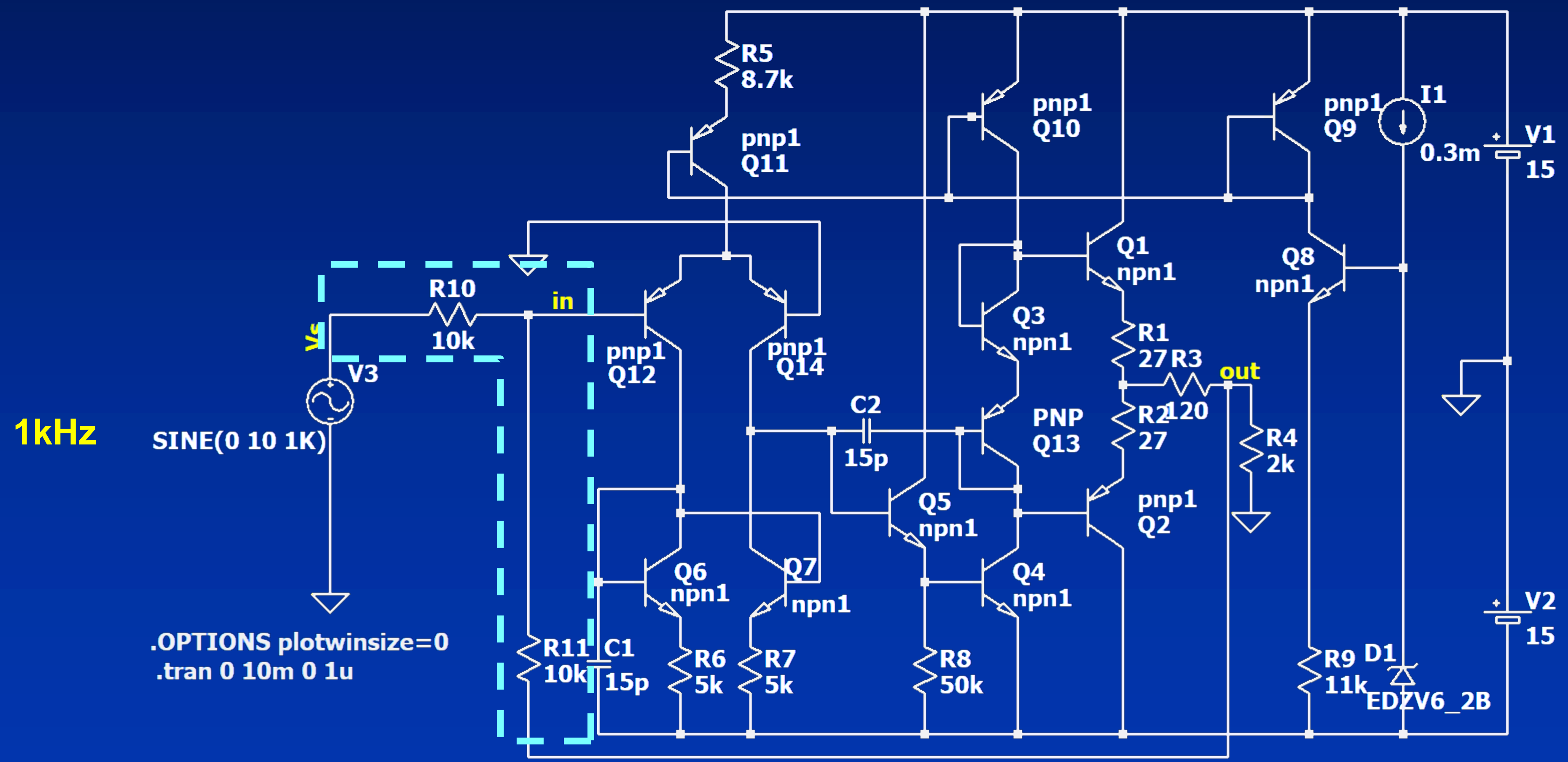
Simulation Circuit　　Inverting Amplifier



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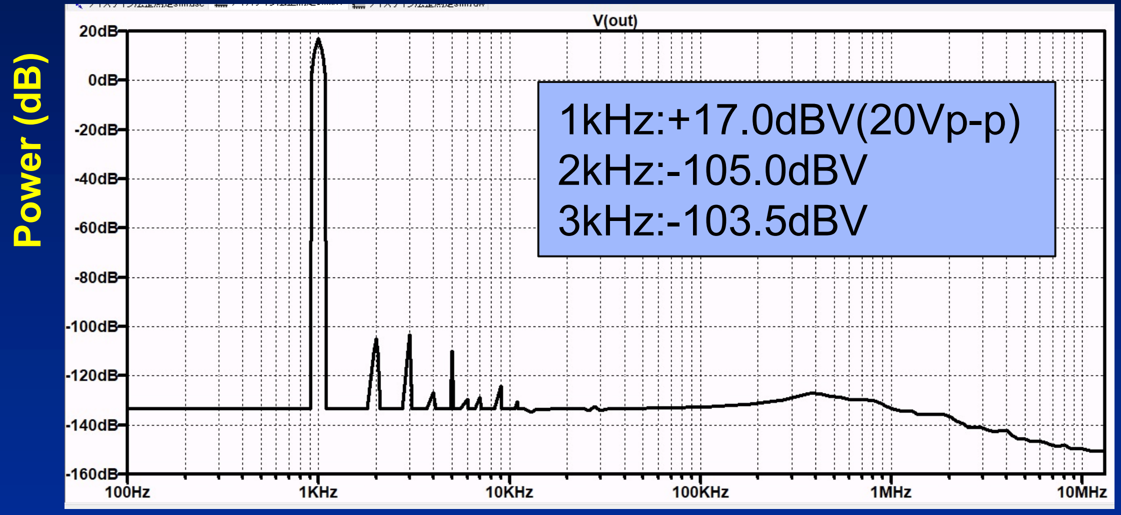
Simulation Results

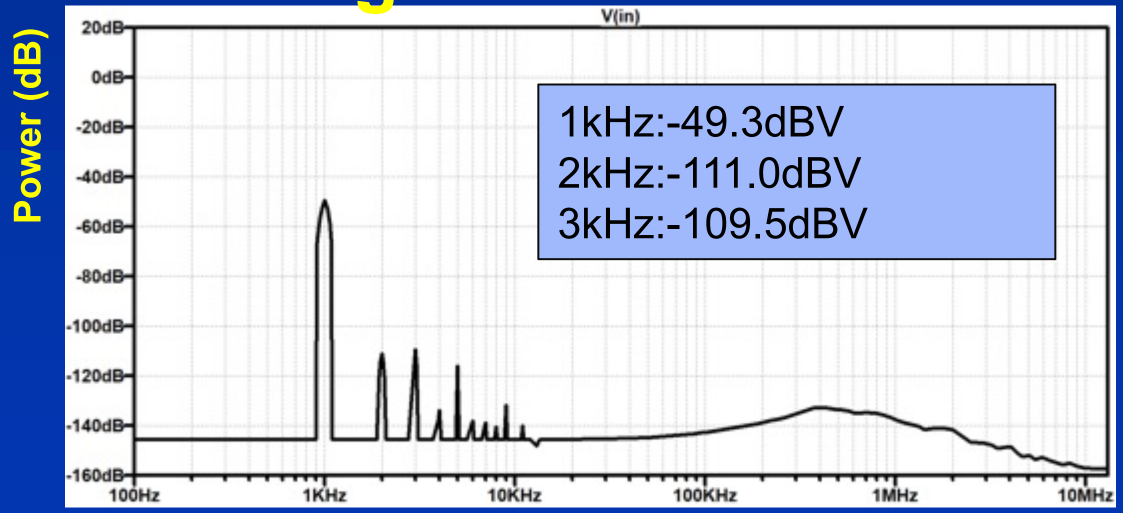
Inverting Amplifier

DUT out



Freq. (Hz)

Summing Node



Freq. (Hz)

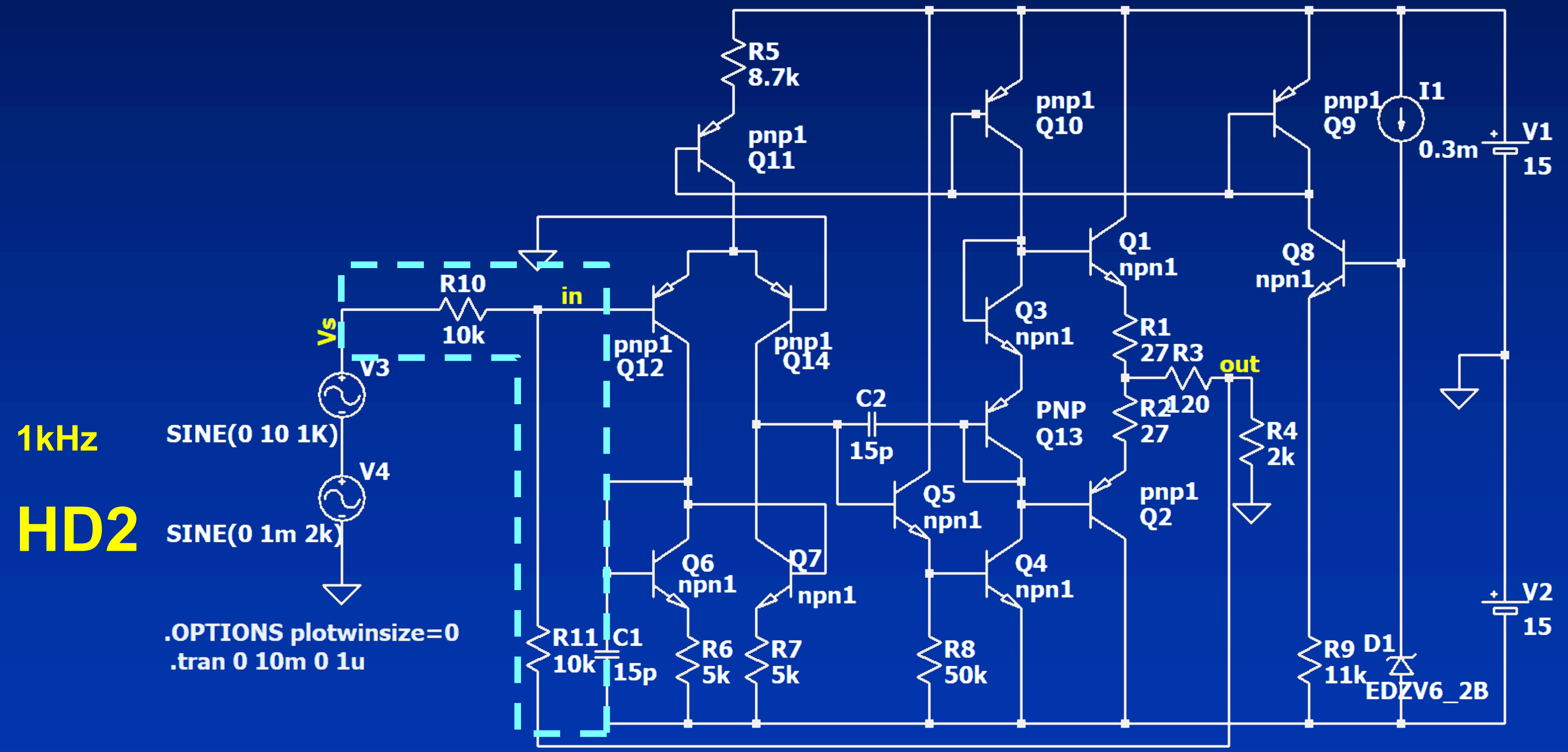
No signal source distortion case

Noise gain= 6 dB
Signal source frequency = 1kHz

HD2 :-105.5 – 17
= -122.0dBc
HD3: -103.5 -17
= -120.5dBc

HD2 : -110.0 – 17 + 6
= -122.0dBc
HD3 : -109.5 – 17 + 6
= -120.5dBc

Adding Distortion to Signal Source



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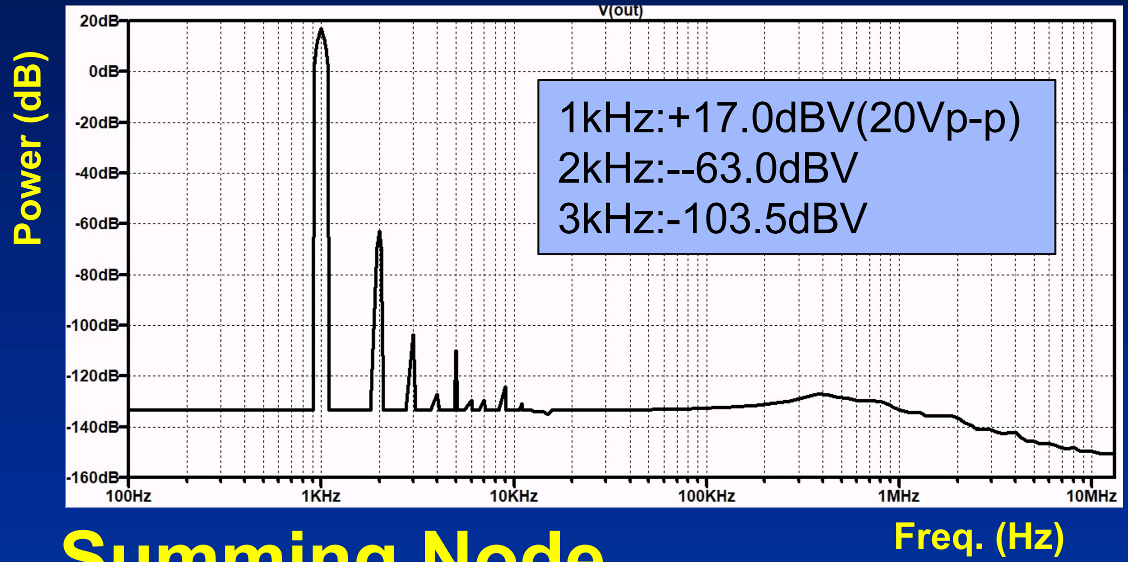
Simulation Results

Inverting Amplifier

With signal source distortion(HD2)

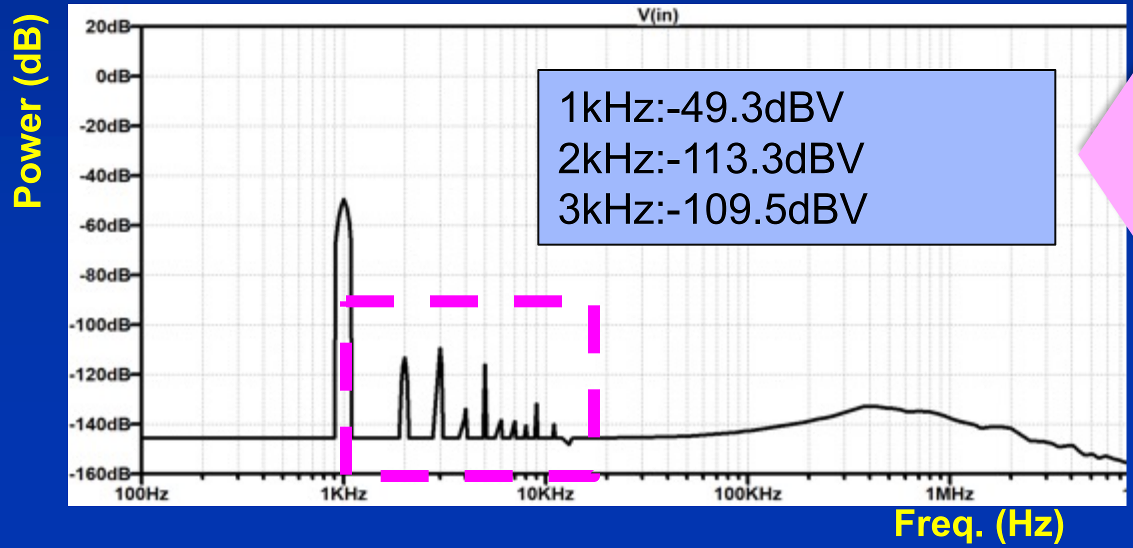
Noise gain=6dB
Signal source frequency = 1kHz

DUT out



HD2 : -63.0 – 17.0 = -80.0dBc
HD3 : -103.5 -17.0 = -120.5dBc

Summing Node



No signal source distortion
1kHz:-49.3dBV
2kHz:-111.0dBV
3kHz:-109.5dBV

Source distortion (-80dBc) does not appear

HD2 : -113.3 – 17.0 + 6 = -124.3dBc
HD3 : -109.5 – 17.6 + 6 = -120.5dBc

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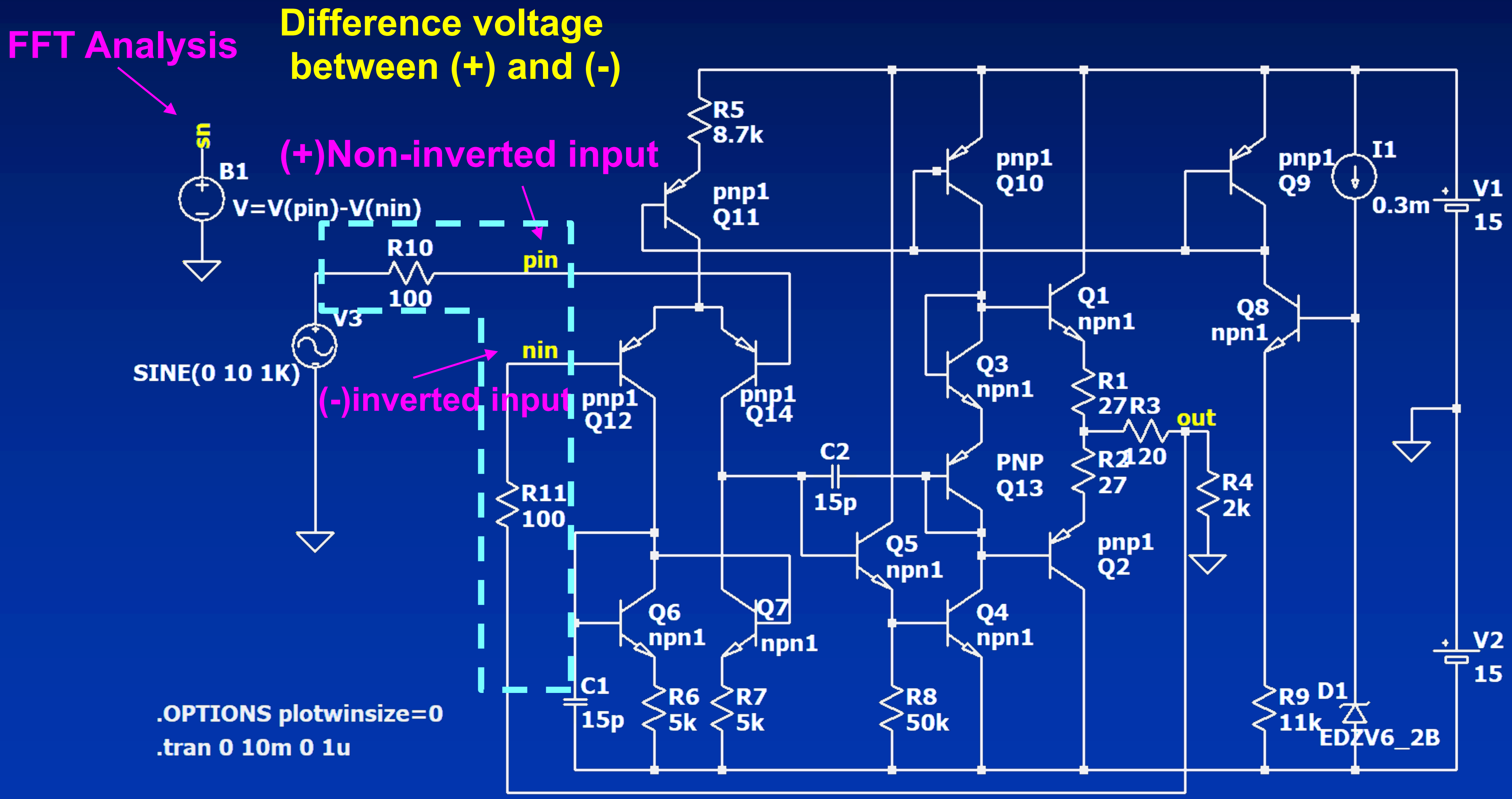
Simulation Circuit

Non-Inverting Amplifier



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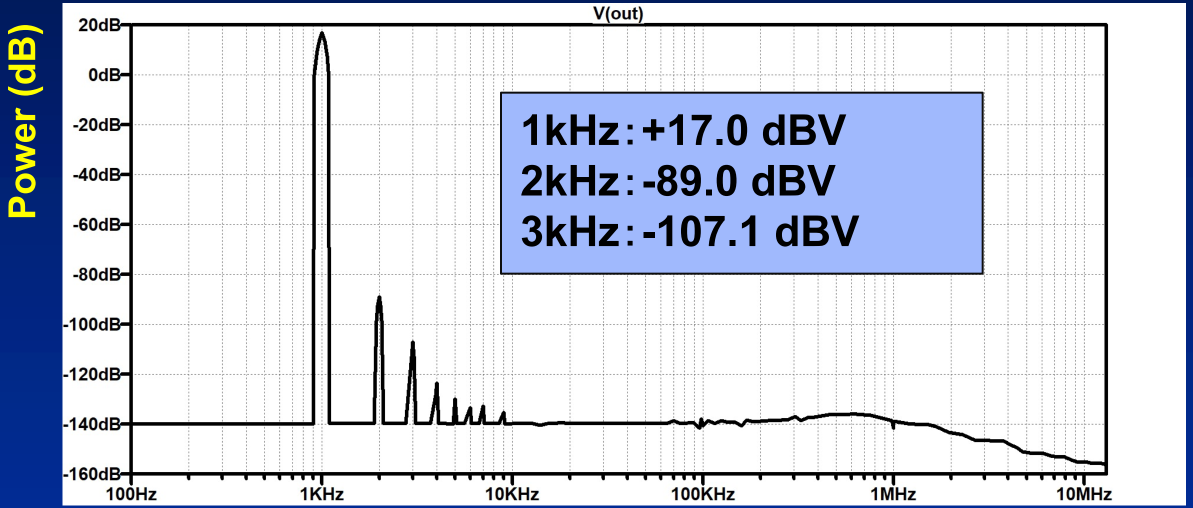
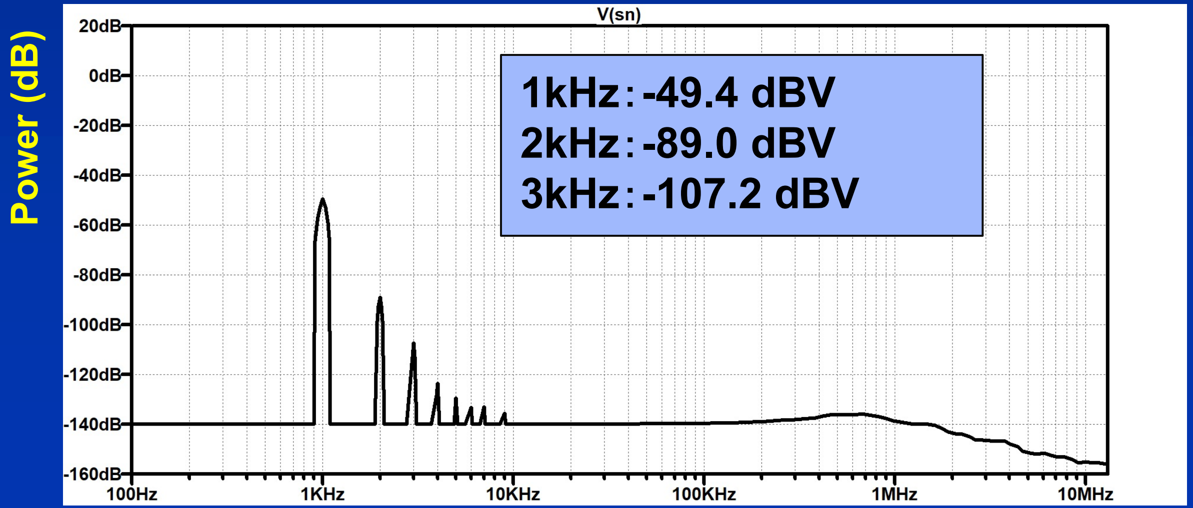
Simulation Results

Non-Inverting Amplifier

DUT out



Summing Node



No signal source distortion

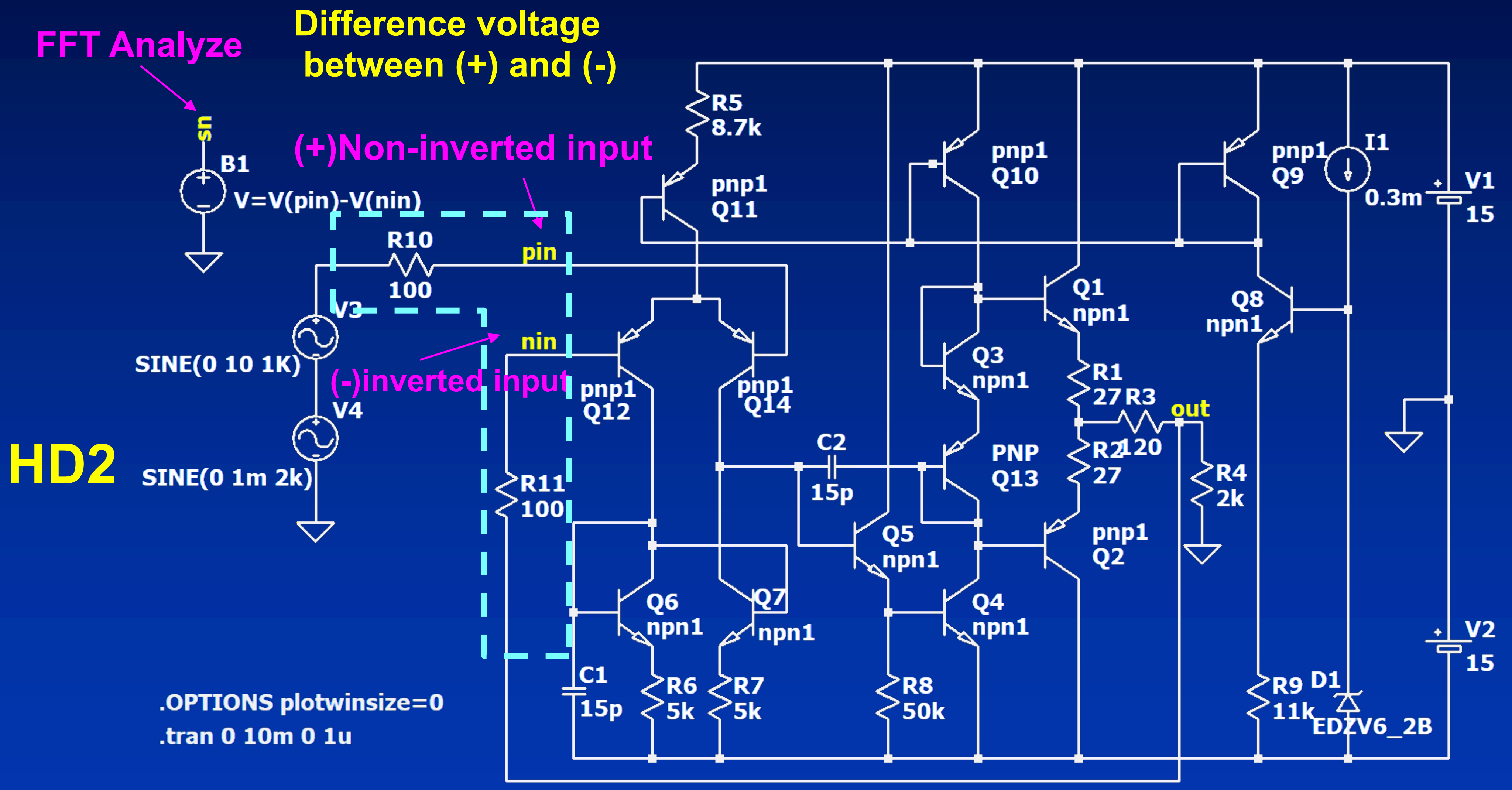
Signal source frequency = 1kHz

FFT analysis of
the difference voltage
between (+) and (-) inputs

Observed harmonic distortion level
⇒ the same as the output
due to noise gain of 1

Adding Distortion to Signal Source

Non-Inverting Amplifier



.OPTIONS plotwinsize=0
.tran 0 10m 0 1u

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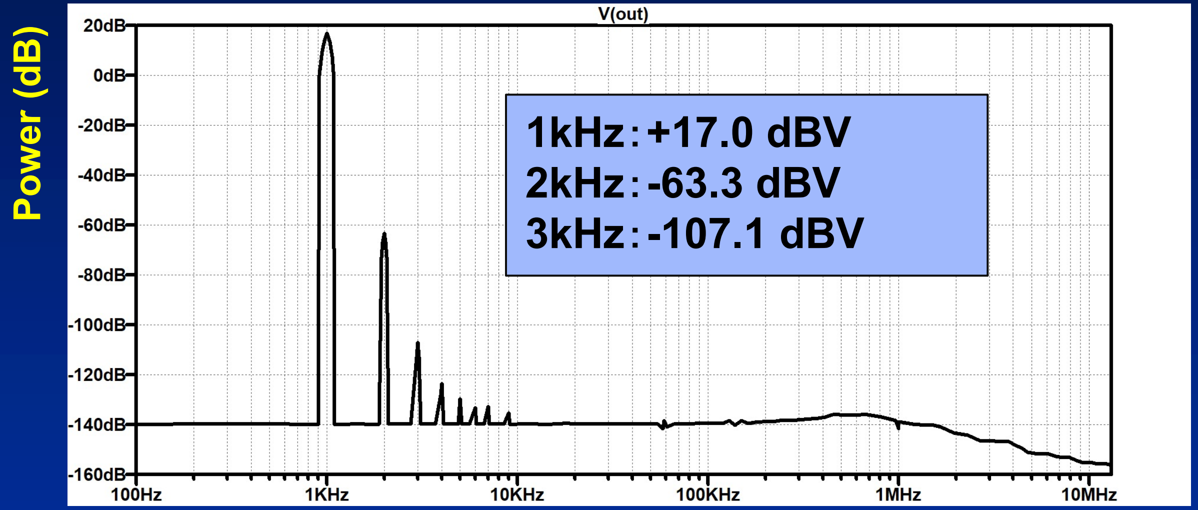
Simulation Results

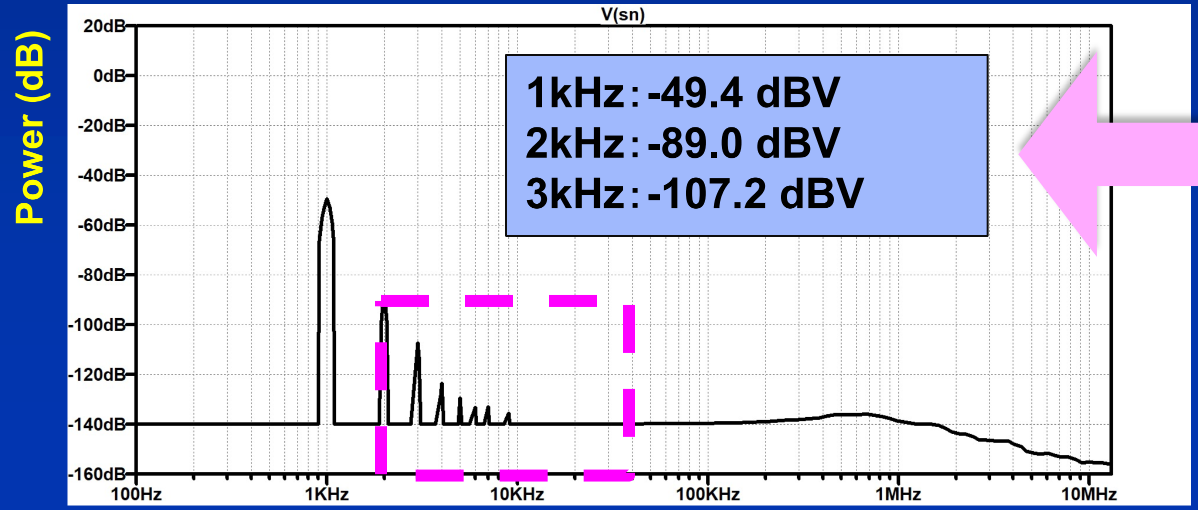
Non-Inverting Amplifier

DUT out



Freq. (Hz)

Summing Node



Freq. (Hz)

With signal source distortion(HD2)

Signal source frequency = 1kHz

FFT analysis of
the difference voltage
between (+) and (-) inputs

No signal source distortion
1kHz:-49.3dBV
2kHz:-89.0dBV
3kHz:-107.2dBV

**Source distortion (-80dBc)
does NOT appear**

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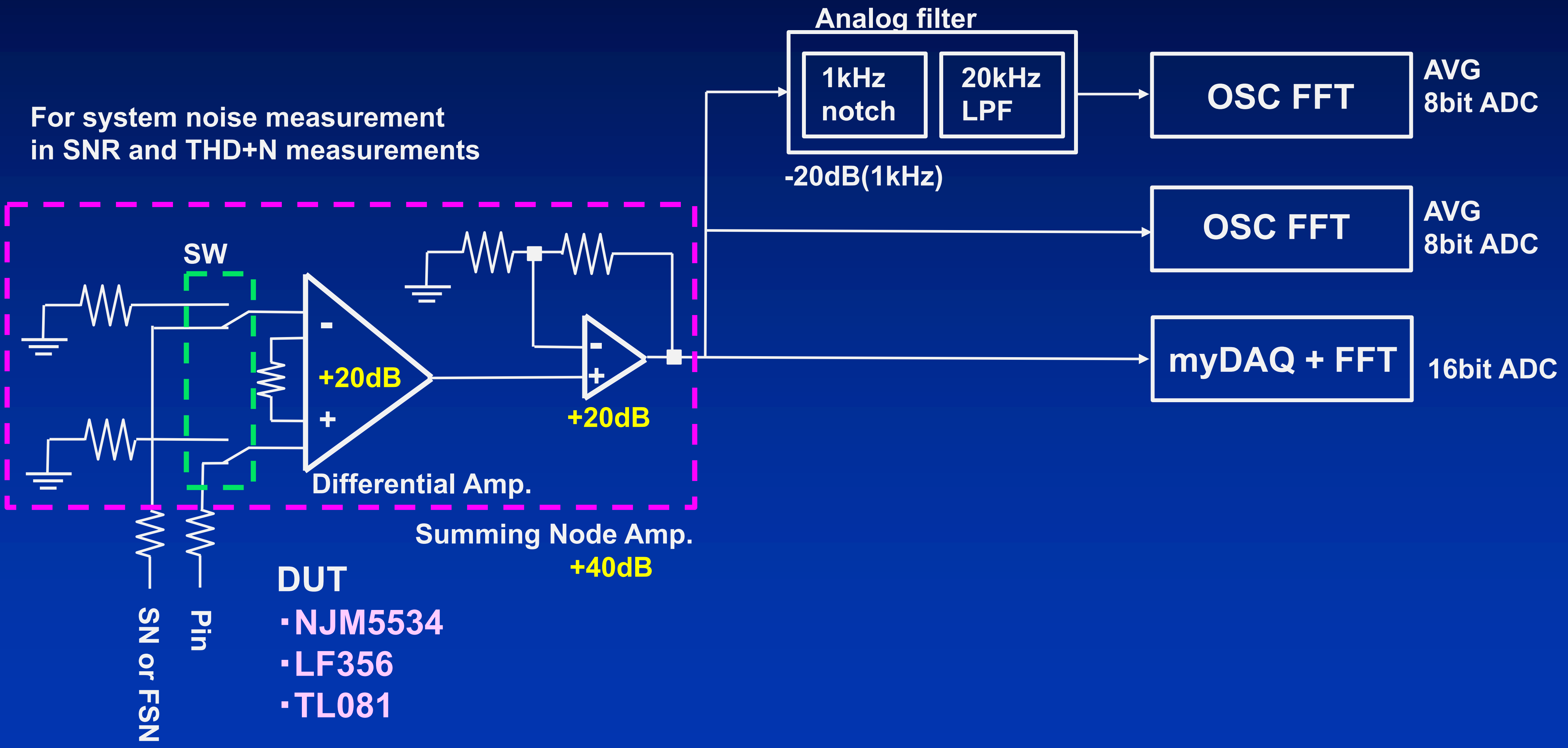
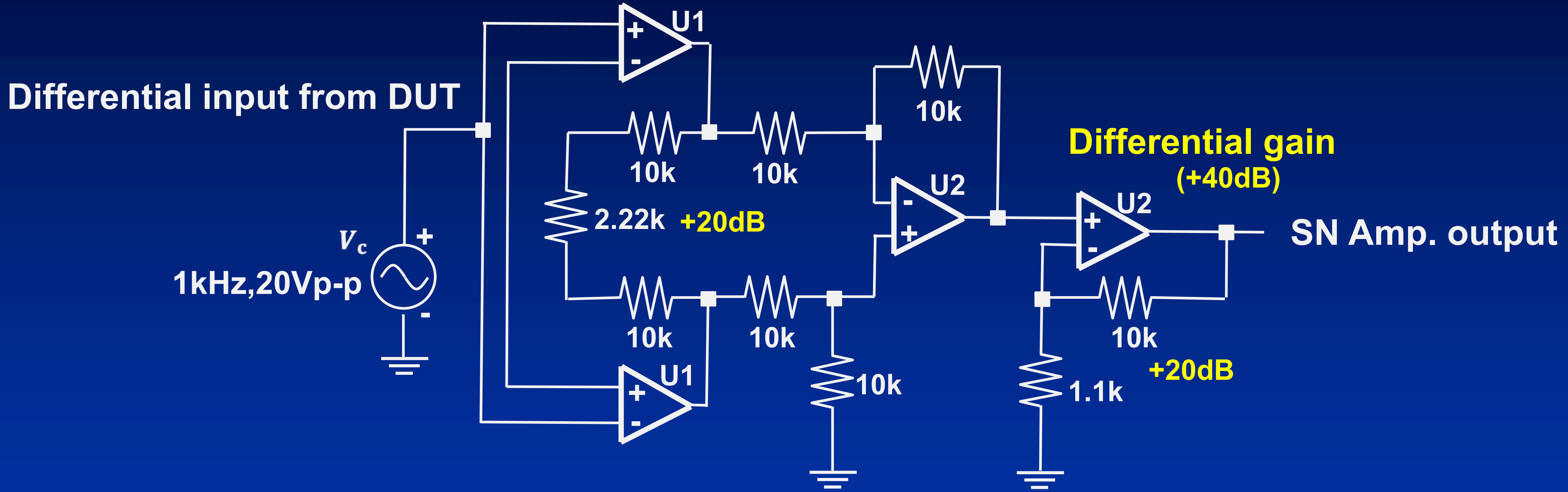
Operational Amplifier Measurement Configuration



● Both inverting and non-inverting amplifier cases

Differential Amplifier for Measurement



- CMRR of the differential amplifier input stage U1 is crucial

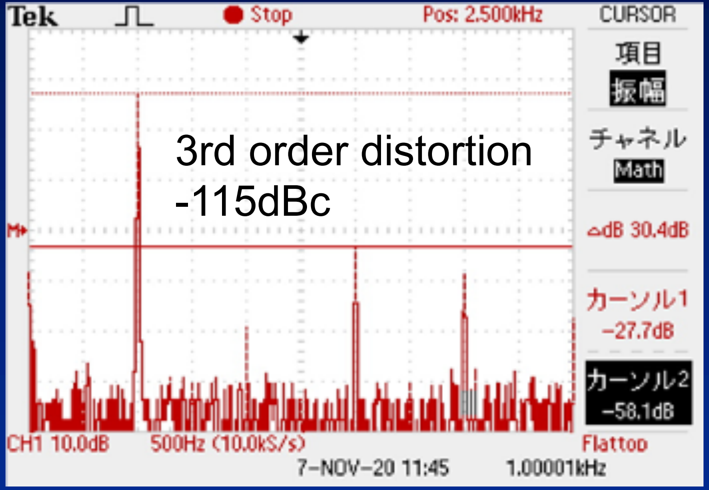
TL072

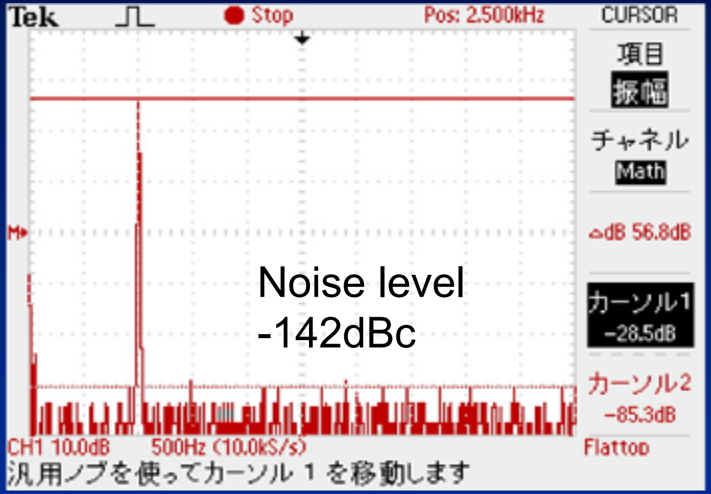
⇒ HD2 : -131dBc HD3 : -115dBc

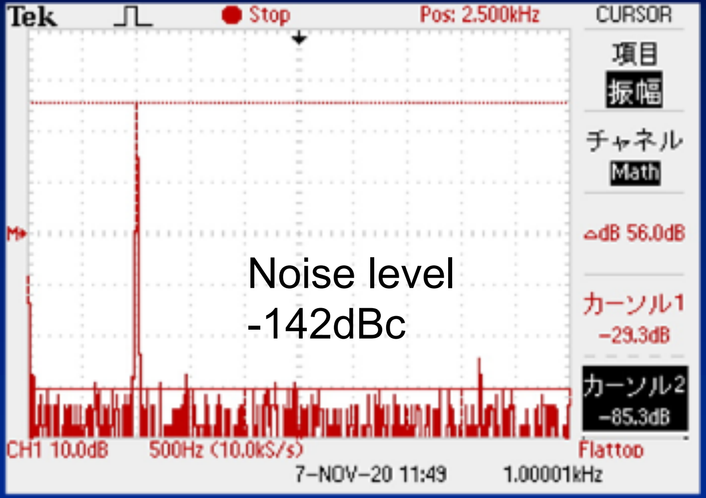
4558/5532

⇒ measurement limit : -142 dBc (noise level)

Distortion Measurement Limit with Differential Amplifier







U1(TL072)+U2(4558)
1kHz：-27.7dBV
2kHz:-74.1dBV
3kHz:-58.1dBV

CMRR:84.7dB

U1(4558)+U2(4558)
1kHz：-28.5dBV
2kHz: < -85dBV
3kHz: < -85dBV

CMRR:85.5dB

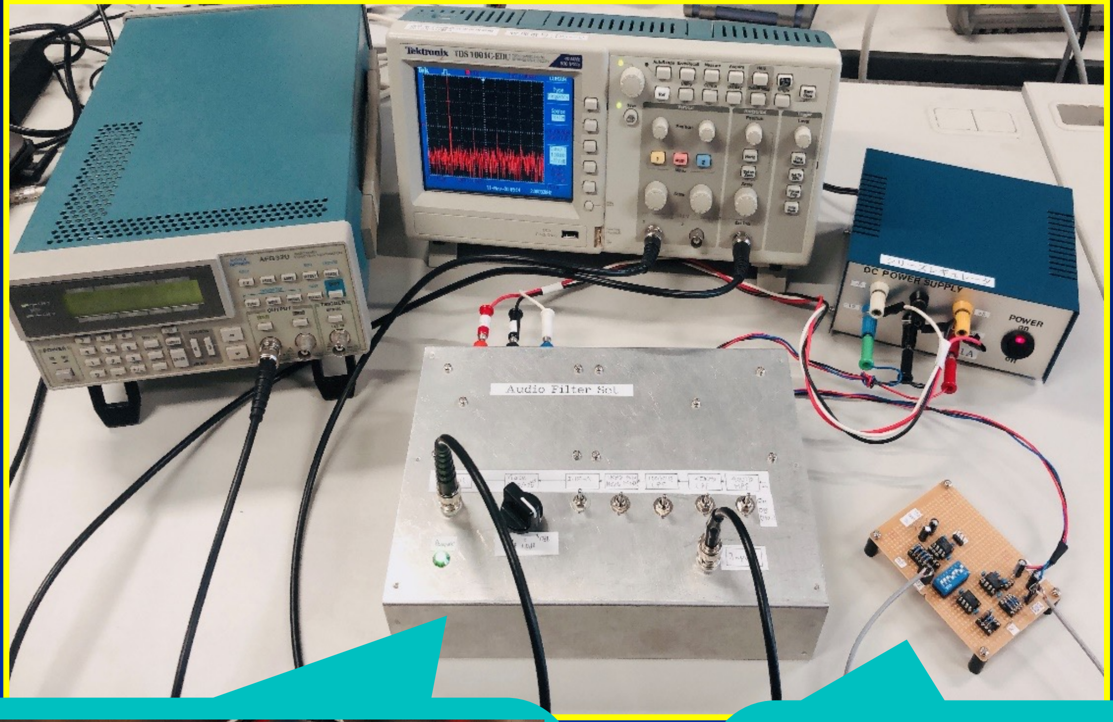
U1(5532)+U2(4558)
1kHz：-29.7dBV
2kHz: < -85dBV
3kHz: < -85dBV

distortion measurement limit :
-115dBc

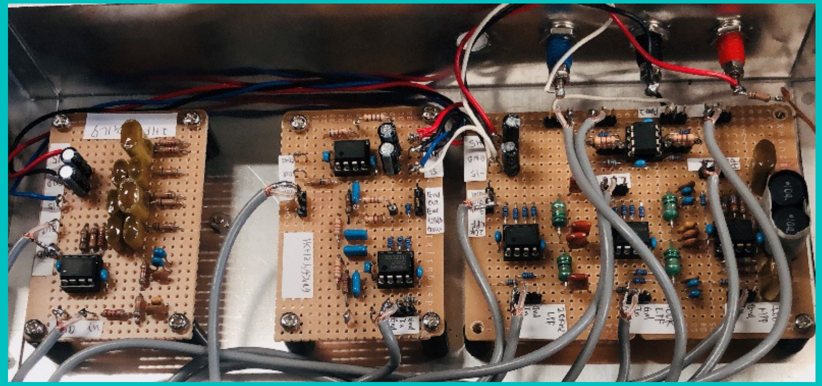
distortion measurement limit :
-142dBc

Measurement Environment using Oscilloscope

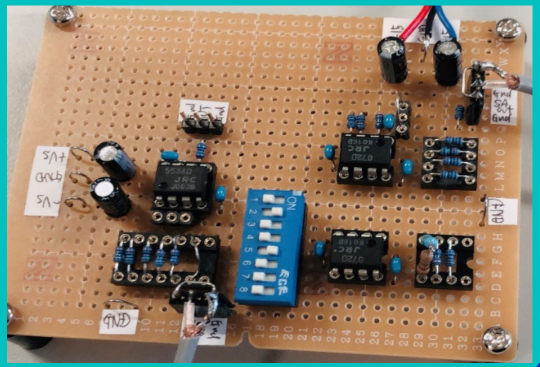
Signal Generator OSC(8bit ADC+FFT)



Series power supply

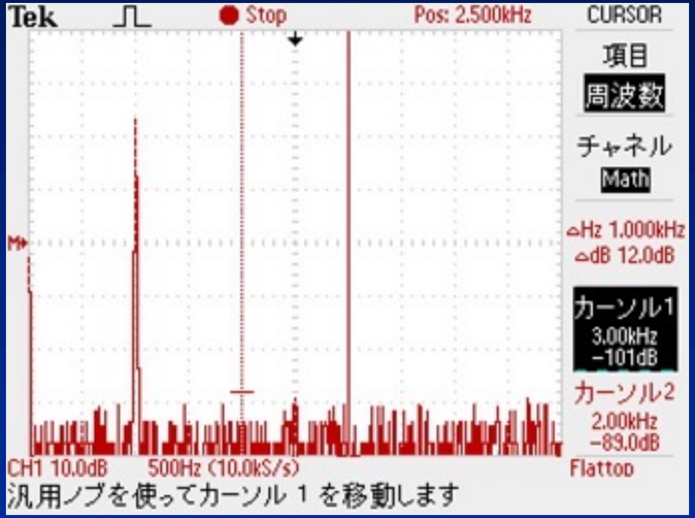


Audio filters(notch , LPF)



DUT OP AMP and Differential amplifier

Non-inverting Amplifier Experiment Results
at summing node and false summing node



At summing node

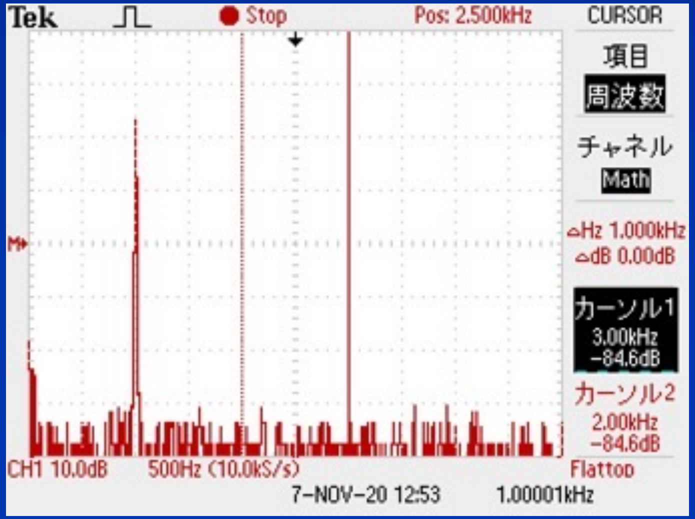
F=1kHz,20Vp-p(=+17dBV)

Without notch filter and LPF

Fundamental : -37.8dBV

HD2:-89.0dBV (-140.0dBc)

HD3:-101dBV (-152.0dBc)



At false summing node

F=1kHz,20Vp-p(=+17dBV)

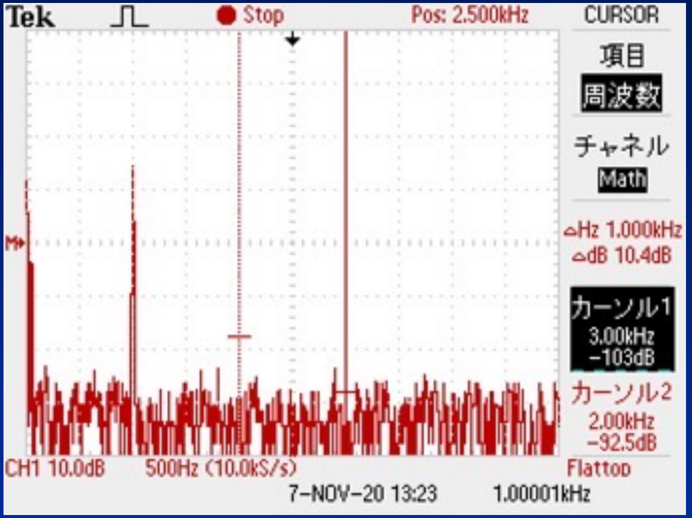
Without notch filter and LPF

Fundamental : -23.8dBV

HD2:-84.6dBV (-135.6dBc)

HD3:-84.6dBV (-135.6dBc)

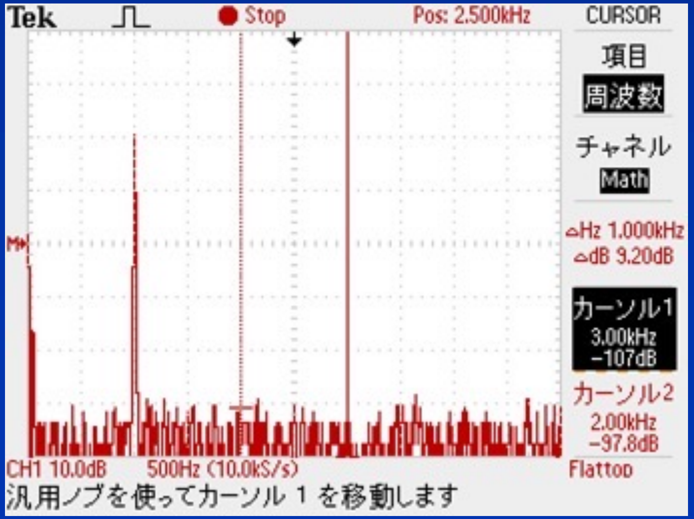
Non-inverting Amplifier Experiment Results using Oscilloscope



At summing node

F=1kHz,20Vp-p(=+17dBV)
With notch filter, LPF=20kHz

Fundamental : -60.5dBV
HD2: -92.5dBV (-143.5dBc)
HD3: -103dBV (-154.0dBc)

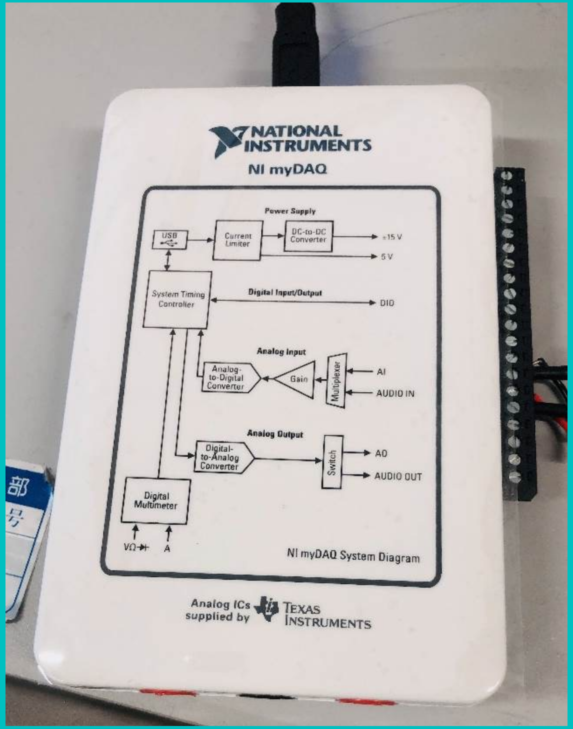


At false summing node

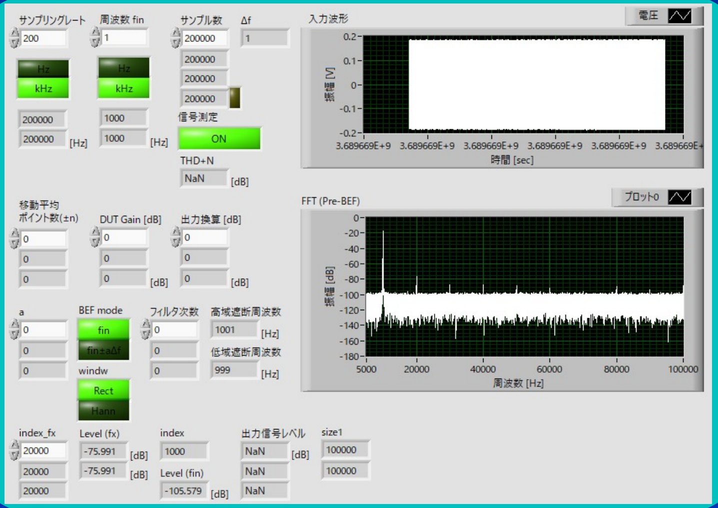
F=1kHz,20Vp-p(=+17dBV)
With notch filter, LPF=20kHz

Fundamental : -46.6dBV
HD2: -97.8dBV (-148.8dBc)
HD3: -107dBV (-158dBc)

Measurement Environment using myDAQ



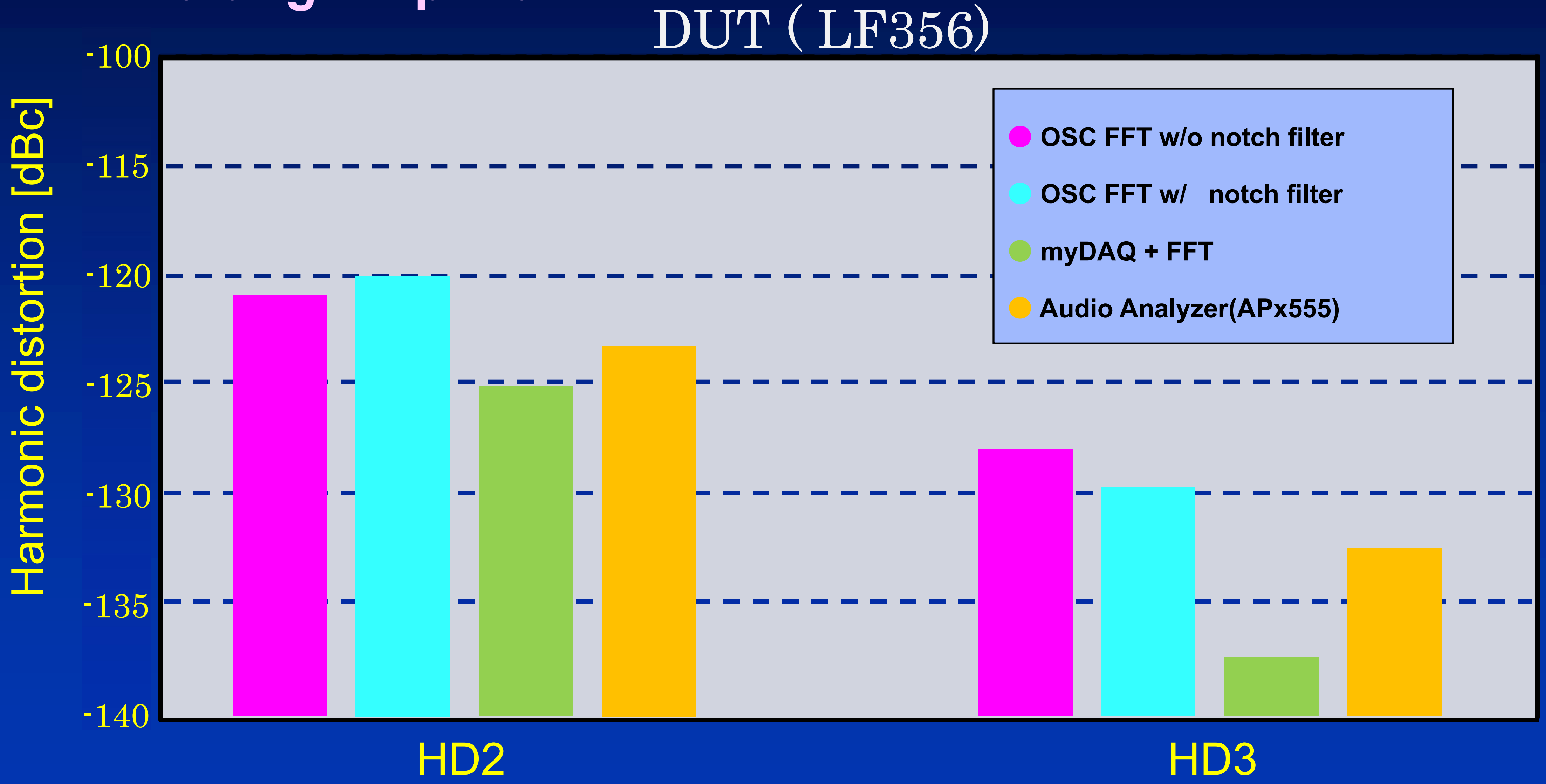
myDAQ(NI)
16bit ADC



PC screen of myDAQ measurement
(FFT analysis by LabVIEW software)

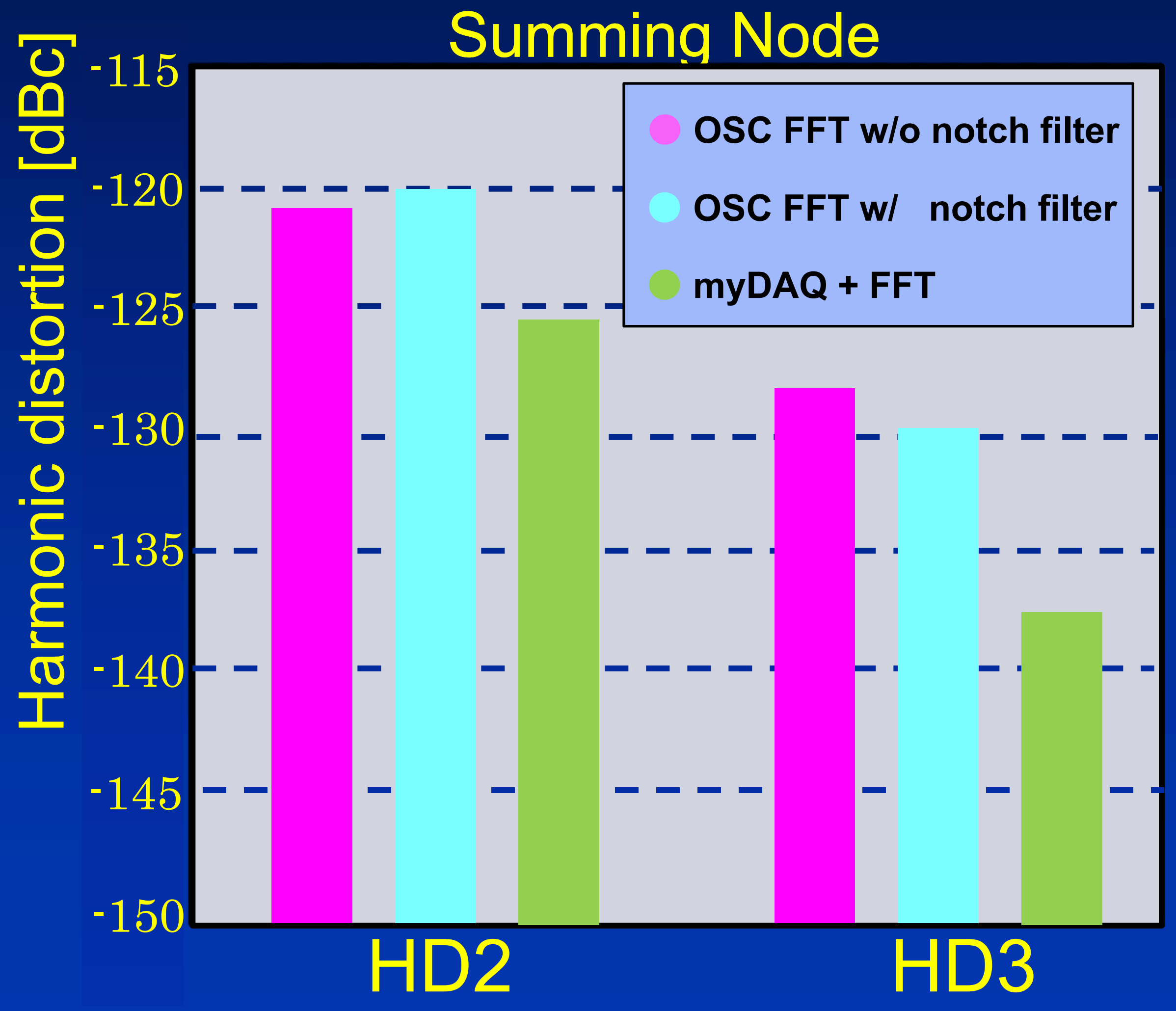
Summing Node Measurement Result Comparison

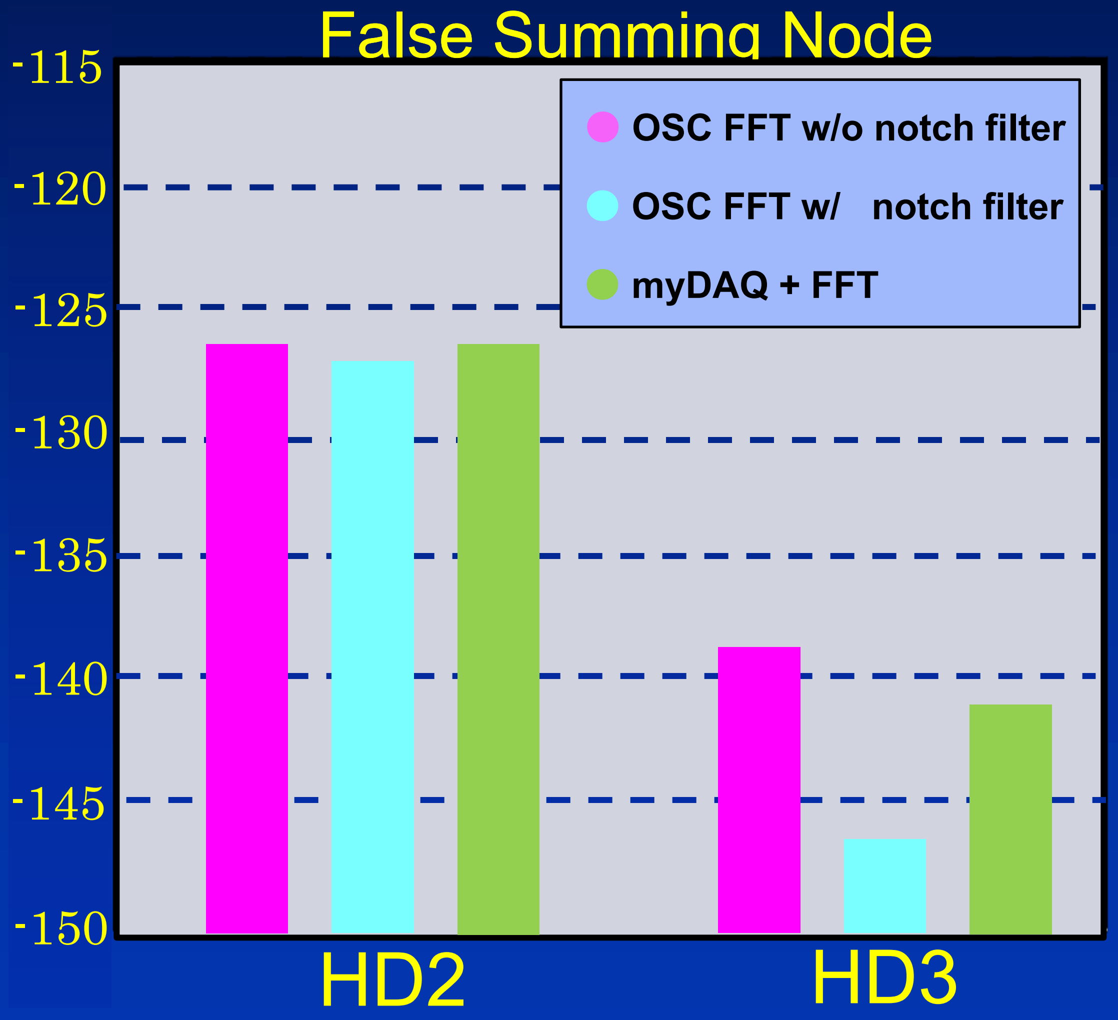
Inverting Amplifier



Comparison of SN and FSN Measurement Results

DUT (LF356)





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- Research Background
- Principle and Theory
  - Summing node method
  - False summing node method
- Simulations
  - Inverting amplifier circuit
  - Non-inverting amplifier circuit
- Experiments
- Conclusions

Conclusions

Operational Amplifier AC Characteristics Testing

● Summing Node

- Accuracy measurements,
  No need for expensive audio analyzers

● False Summing Node

- Measurable without oscillation
- Resistor ratio error effect is negligible
  ⇒ Equivalent measurement accuracy to the summing node method

● Inverting, non-inverting amplifiers measurement

- Can be handled with appropriate differential amplifier

Thank you for listening

Q & A (in ITC)

Q1.抵抗比のマッチング精度1%は、オンチップで考えられていますか？(Stephen Sunter)

A1.抵抗はオフチップを考えている。尚、オンチップでも抵抗比のマッチング精度1%は容易に達成できる。

Q2.「フィードバック回路の寄生容量とインダクタンスの増加を考慮しましたか？」(Lucel)

A2. Summing Nodeの寄生容量やインダクタンスの追加についてはシミュレーションしていない。これについては、今後検証したいと思う。しかし、False Summing Nodeを使用することで、それらの影響を無視できる。