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Grand Hyatt Jeju, Republic of Korea

Digital-to-Analog Converter Configuration Based on Non-uniform Current Division Resistive-Ladder

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OUTLINE

- Research Background and Objective
- R-2R DAC Configuration
  - R-2R Current-steering DAC
- N-ary DAC Configuration
  - Resistive Ladder with Current Division
- Connecting Resistor Ladders
  - Connection conditions
  - Proposed DAC configuration and simulation
- Conclusion and Future work

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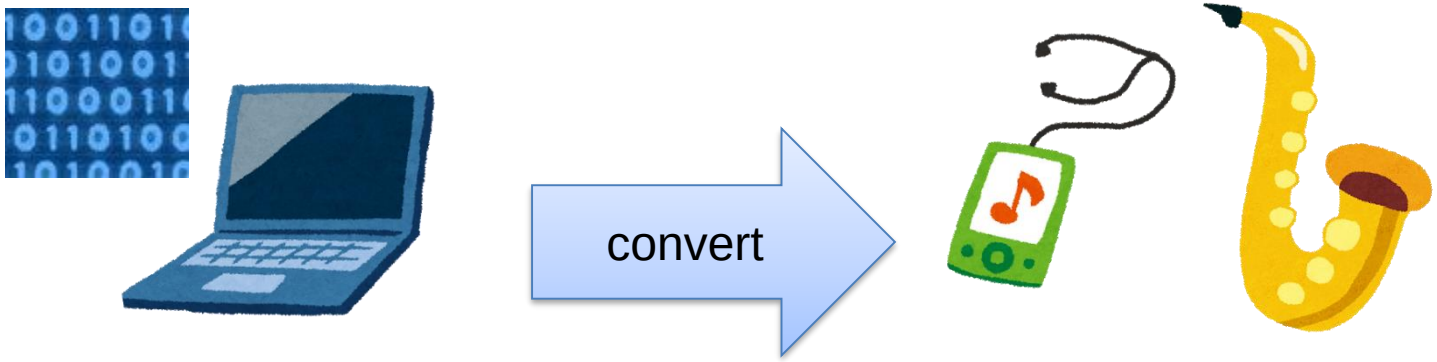
Research Background

- Digital-to-Analog Converter (DAC)
  - Output of digital signal processing results



Digital signal

Analog signal
(Voltage, sound, light, etc.)

  - Internal circuit of ADC

Objective：Investigation of resistor ladder and current-steering DAC architectures

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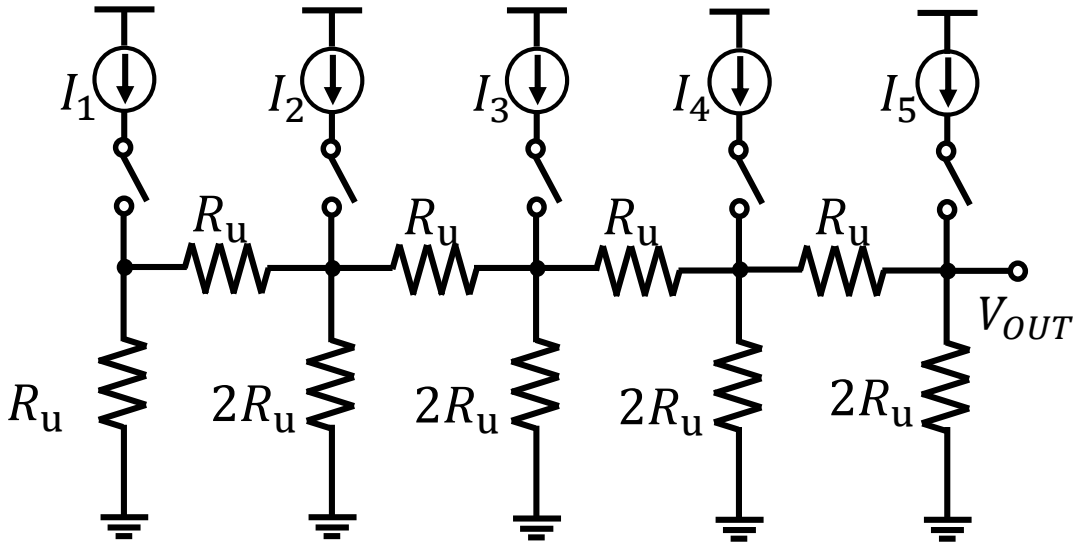
R-2R Current-Steering DAC



5-bit R-2R current-steering DAC

- Using binary weighting with a well-known R-2R ladder
  - Identical currents $I_1, \ldots, I_5$

Good

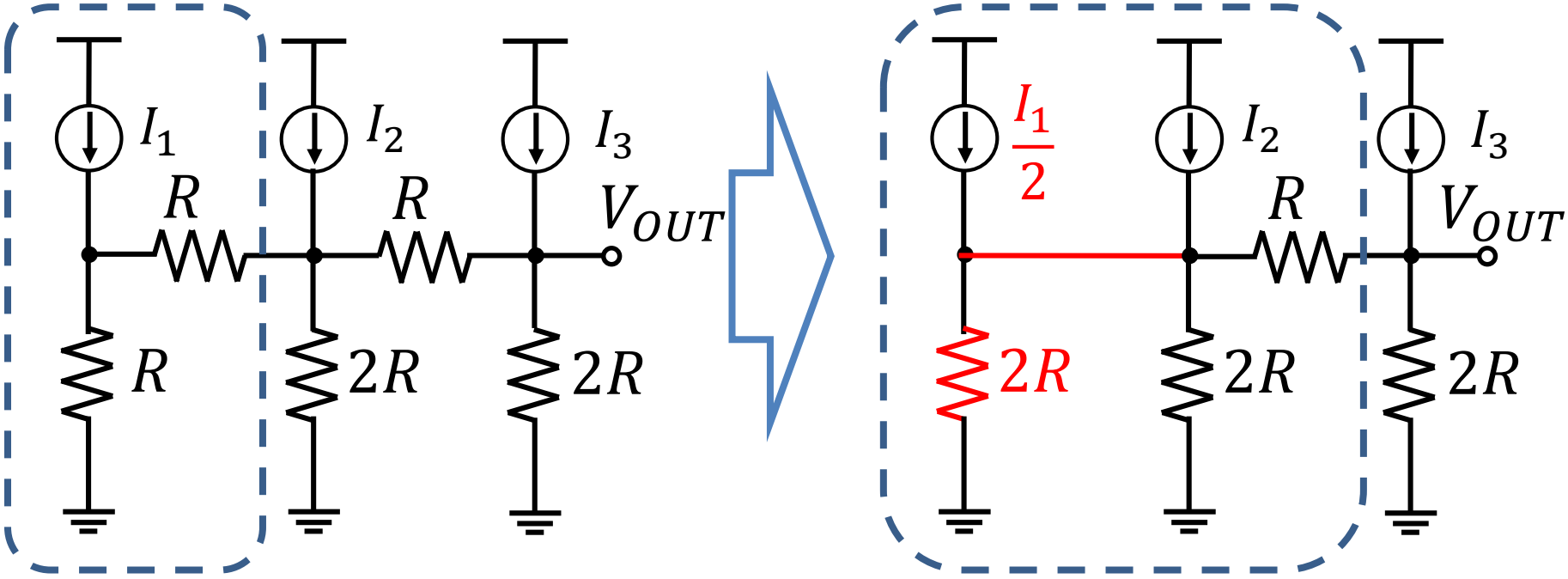
- No decoder
- Fast operation with current sources

Bad

- DNL degradation due to element mismatches
- Large glitches

Principle of operation of R-2R DAC

- Replacing a current source and resistors with equivalent circuit, using Norton theorem
  - Internal current is weighted twice for each stage

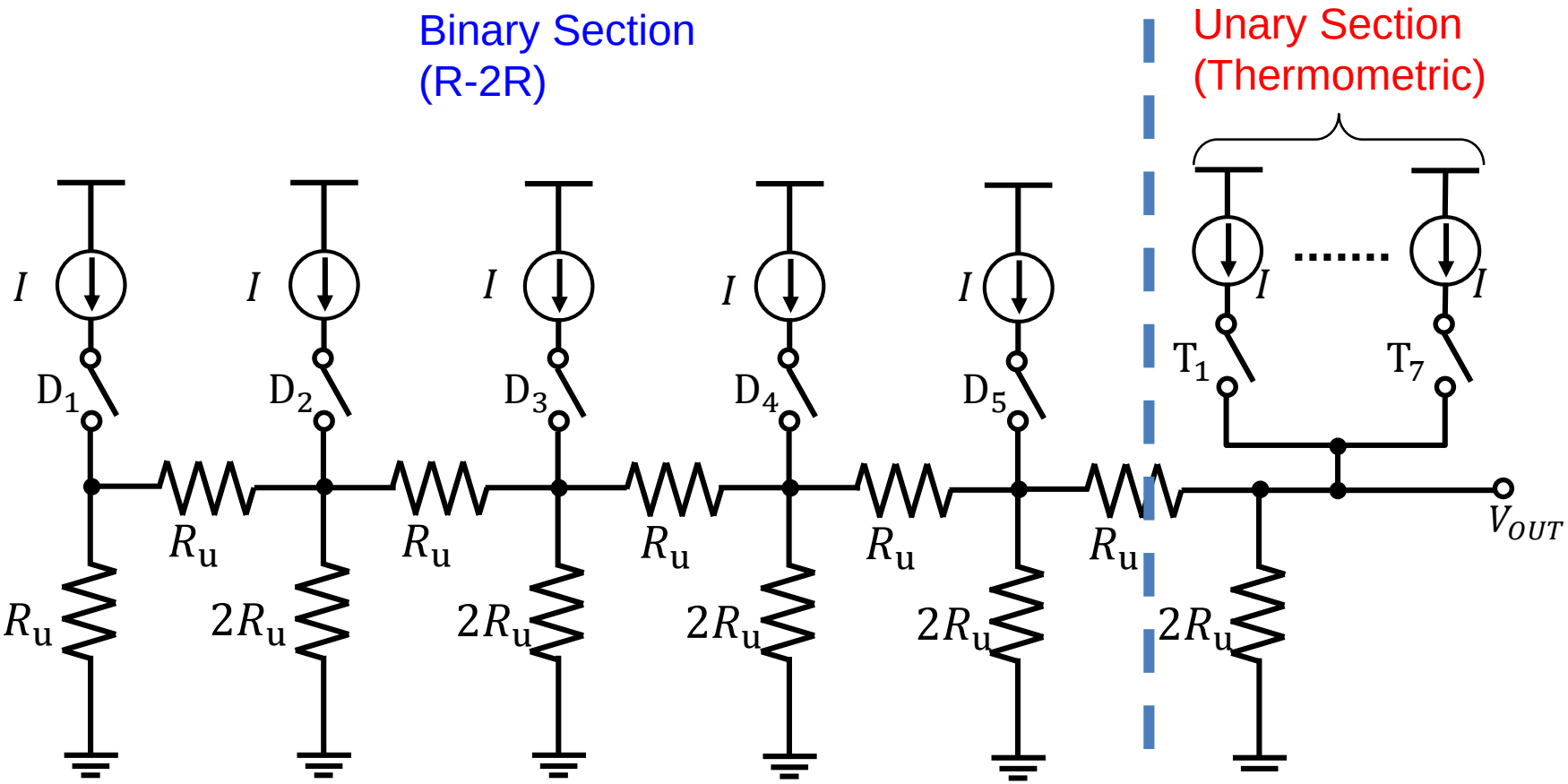


3-bit R-2R DAC

Replacement to equivalent circuit

Segmented R-2R DAC

- Glitch reduction, DNL reduction
  - Need binary-to-thermometer decoder for unary section



8-bit segmented R-2R DAC（Upper 3-bit for unary codes）

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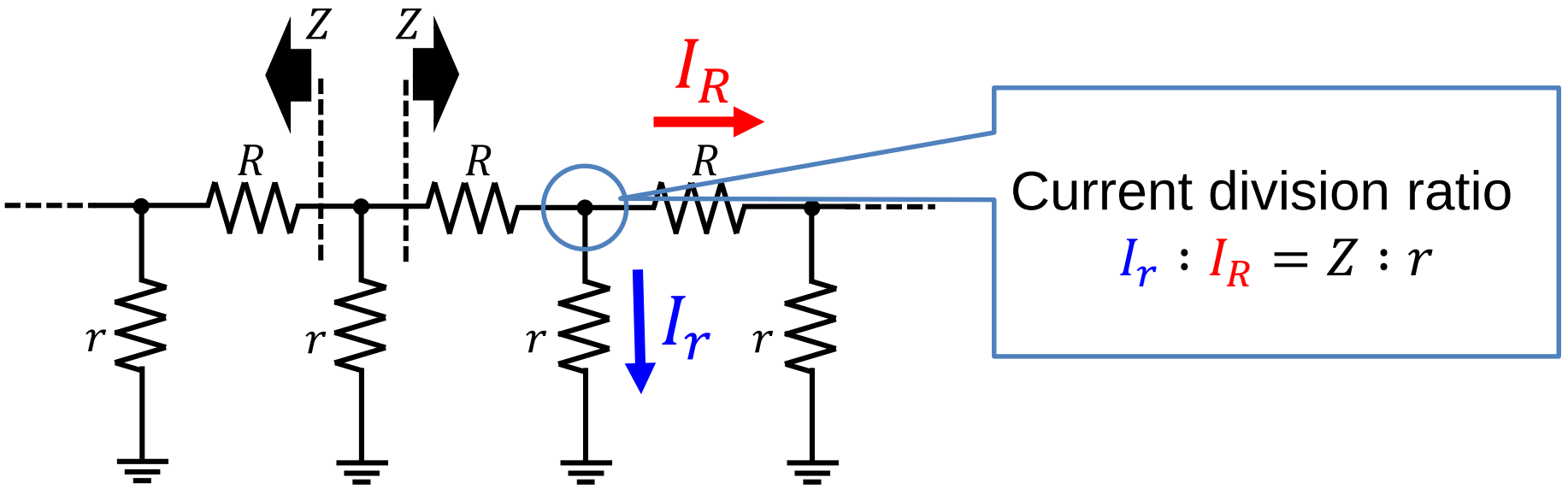
Current Division with Resistive Ladder



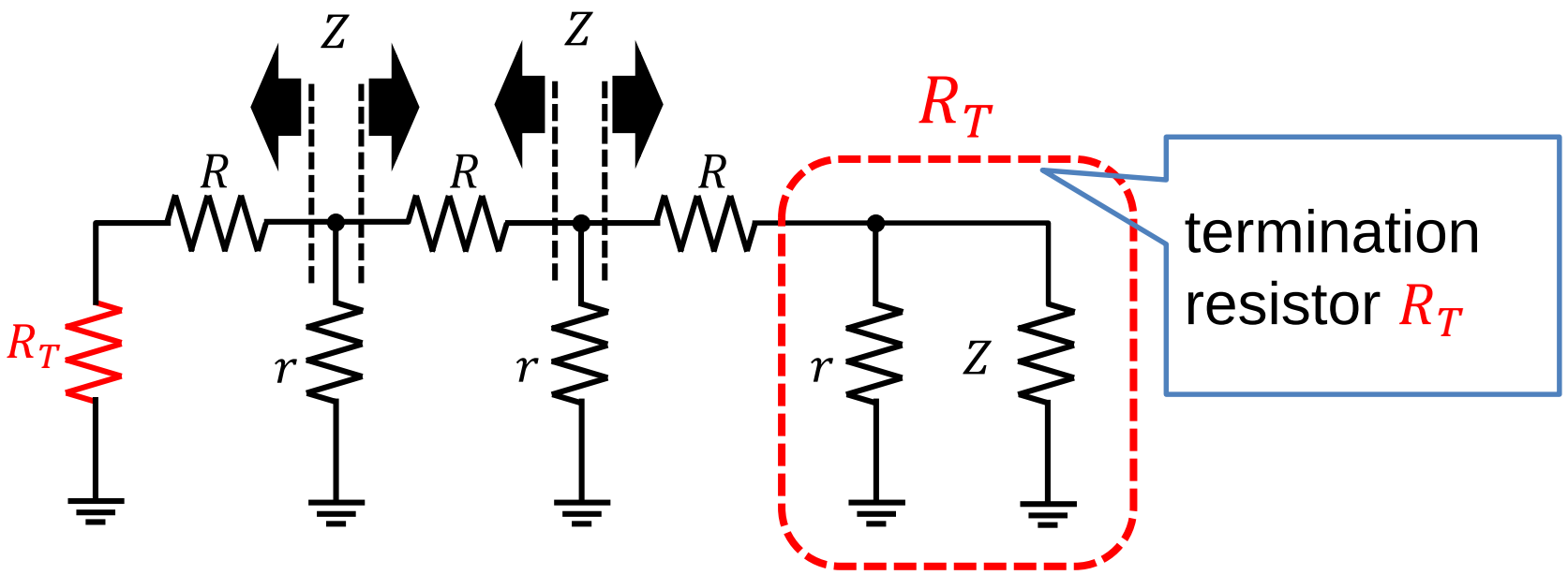
- Composite resistance Z

$$Z = \frac{R}{2} + \frac{\sqrt{R(R+4r)}}{2}$$

- For current division ratio $N-1:1$ $(N = 2,3,4,\dots)$

$$I_r : I_R = Z : r = N-1 : 1$$
$$\leftrightarrow R : r = (N-1)^2 : N$$

Finite Length of Resistor Ladder



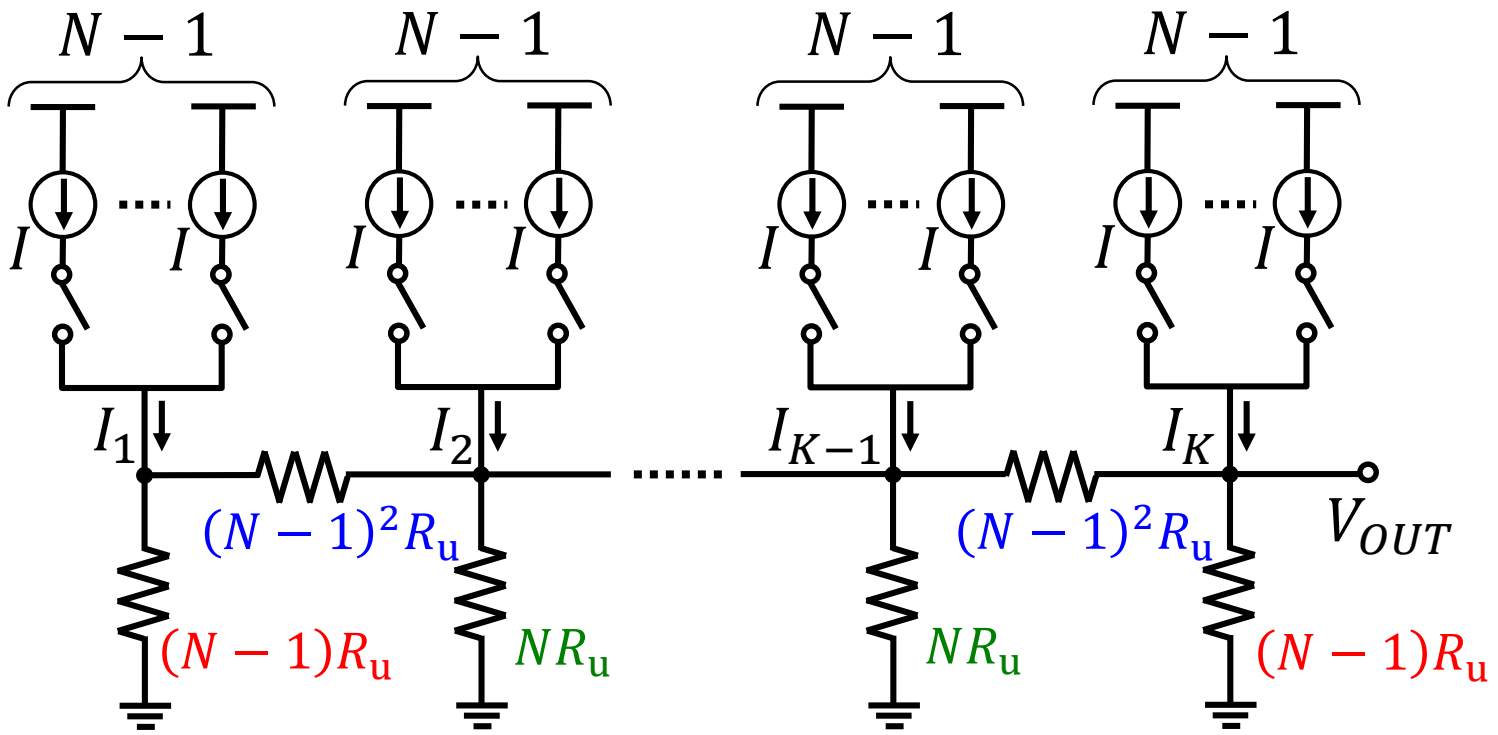
- Termination resistor R_T with current division ratio $N-1:1$

$$R_T = Z - R = \frac{R}{N-1}$$

- A new interpretation of the R-2R ladder and N-ary ladder

$$R : r : R_T = (N-1)^2 : N : N-1$$

N-ary Resistance Ladder Configuration



N : Current division ratio K : Number of ladder stages

R_u : Reference resistance I : Unit current

I_j : Current flowing into j-th node

- For N = 2 ⇒ K-bit R-2R DAC

Output Voltage and Steps

- Output voltage

$$V_{\mathrm{OUT}}(I_1, \cdots, I_K, R_{\mathrm{u}}, N, K) = (N-1)R_{\mathrm{u}} \sum_{j=1}^{K} \left(\frac{I_j}{N^{K-j}} \right)$$

- Maximum output voltage

$$V_{\mathrm{MAX}}(I, R_{\mathrm{u}}, N, K) = R_{\mathrm{u}} I \cdot N(N-1) \cdot \left(1 - \frac{1}{N^K} \right)$$

- Output voltage minimum step

$$V_{\mathrm{MIN}}(I, R_{\mathrm{u}}, N, K) = (N-1)R_{\mathrm{u}} I \cdot \frac{1}{N^{K-1}}$$

- Number of output voltages

$$N^K - 1$$

N : Current division ratio
R_{u} : Reference resistor
I_j : Current into j-th node
K : Number of ladder stages
I : Unit current

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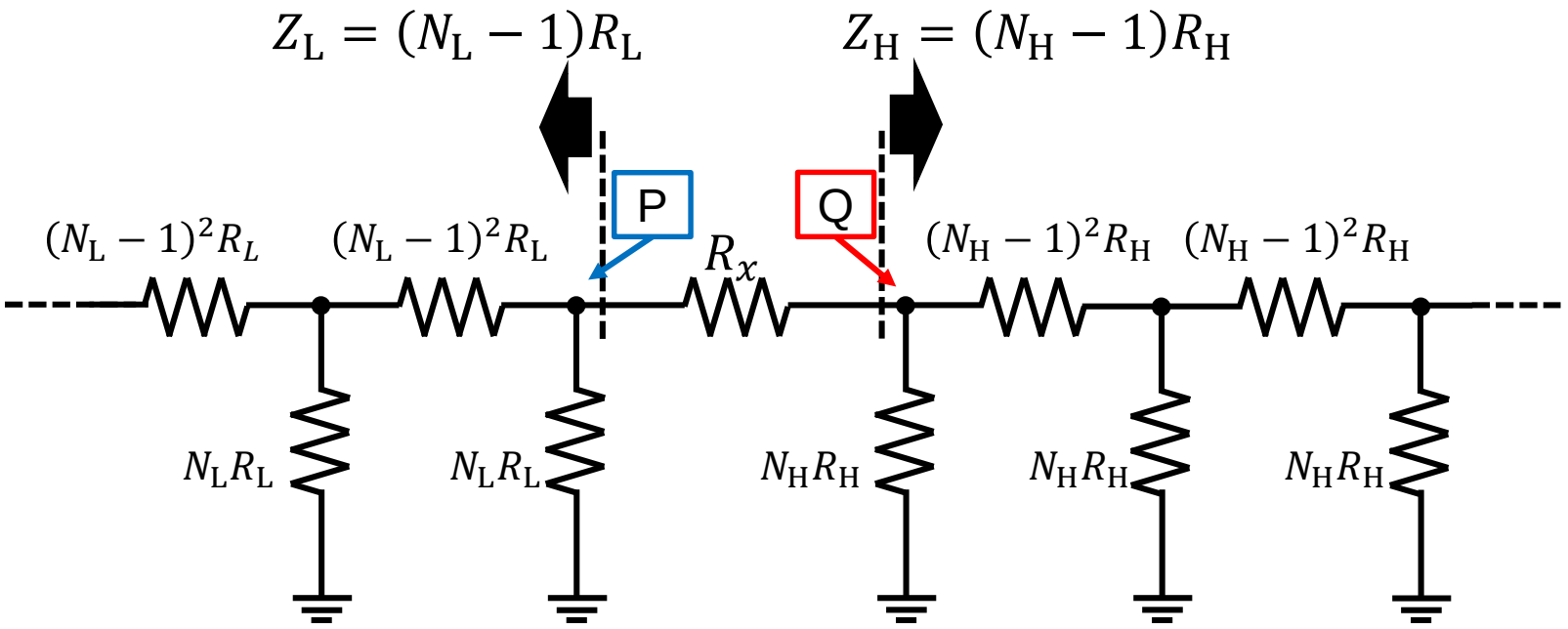
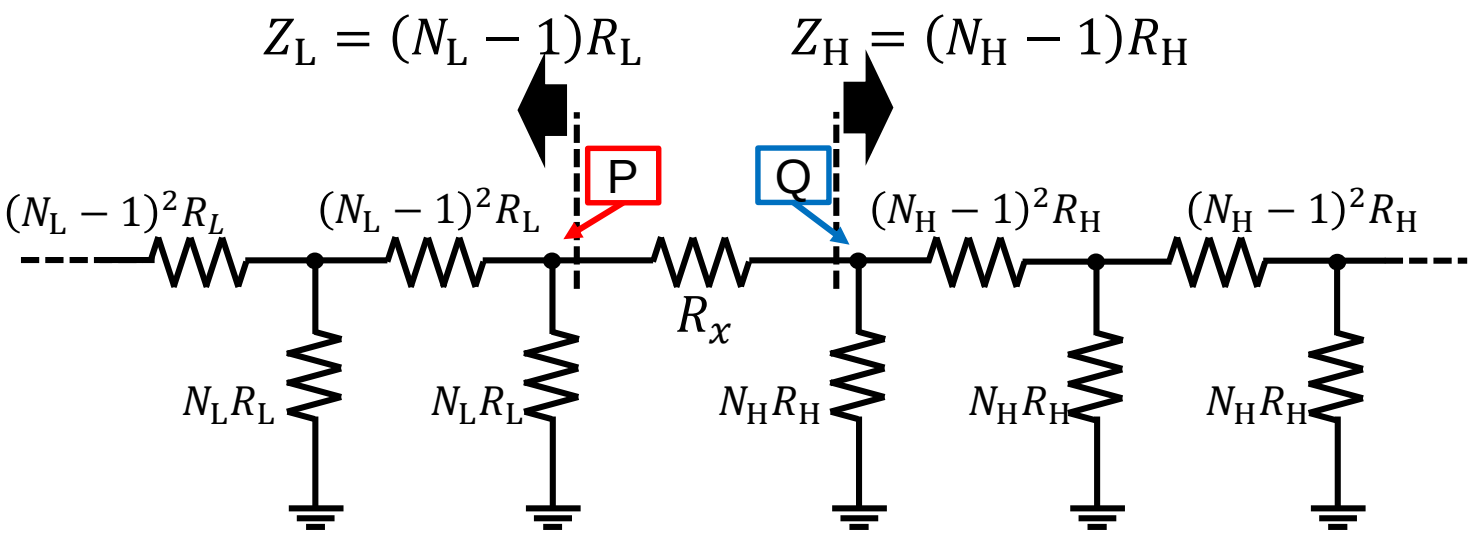
Connection of Resistive Ladders



- Parameters
  - R_x : Connection resistor
  - $N_{\mathrm{H}}/N_{\mathrm{L}}$: Upper/Lower-side current division parameter
  - $R_{\mathrm{H}}/R_{\mathrm{L}}$: Upper/Lower-side reference resistor
  - $Z_{\mathrm{H}}/Z_{\mathrm{L}}$: Resistance from node Q/P of view

Connection Conditions



- Connection conditions
  1. To the right of P ⇒ Characteristics of N_{H}-ary resistor ladder
  2. To the left of Q ⇒ Upper side N_{H}-ary characteristic is not broken

$$\begin{cases} R_x + Z_{\mathrm{H}} = N_{\mathrm{H}} Z_{\mathrm{L}} \\ R_x + Z_{\mathrm{L}} = N_{\mathrm{H}} Z_{\mathrm{H}} \end{cases}$$

⇨

$$R_{\mathrm{H}} = \frac{N_{\mathrm{L}} - 1}{N_{\mathrm{H}} - 1} R_L, \qquad R_x = (N_{\mathrm{H}} - 1)(N_{\mathrm{L}} - 1)R_{\mathrm{L}}$$

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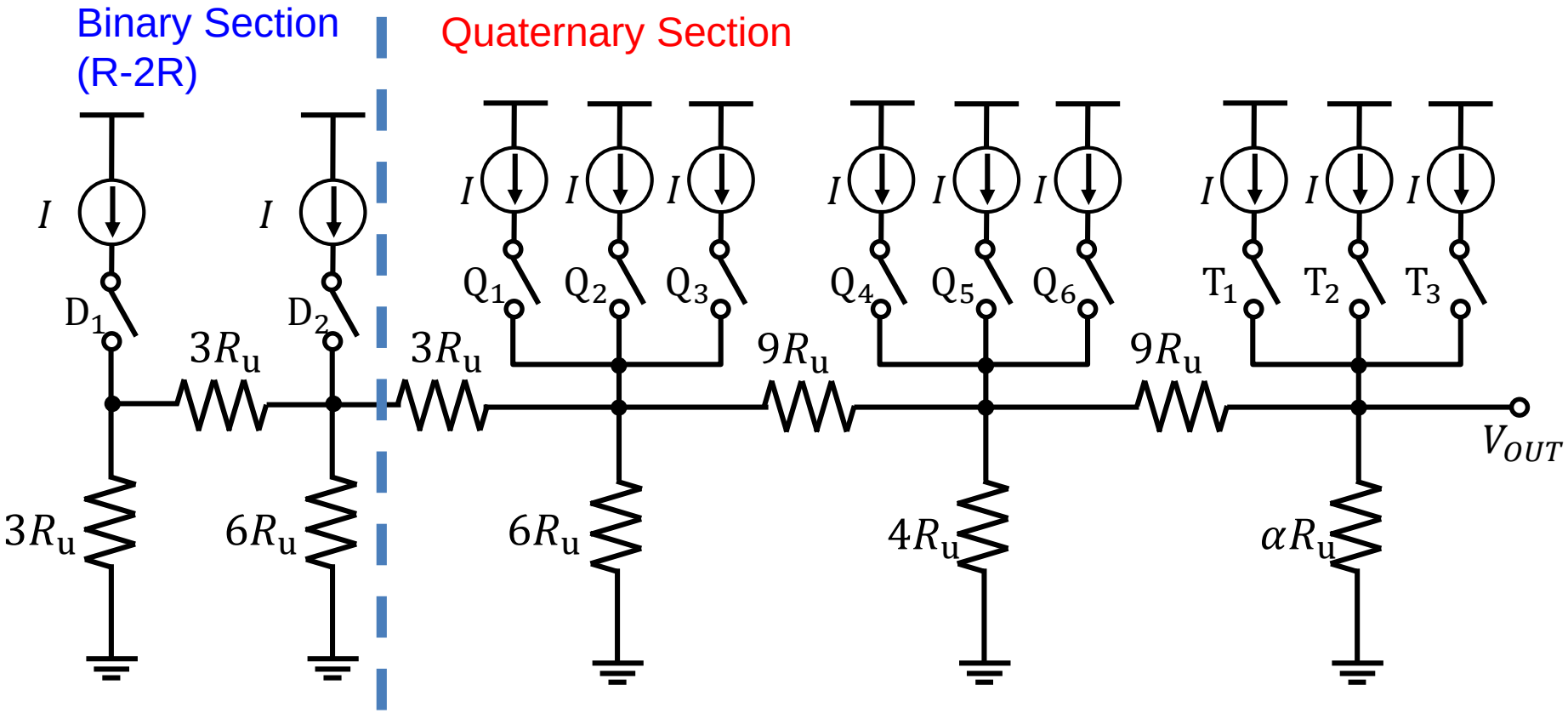
Configuration Example

- 8-bit R-2R and 9R-4R connected resistive ladder DAC

$$R_{\mathrm{L}} = 3R_{\mathrm{u}},\ R_{\mathrm{H}} = R_{\mathrm{u}},\ R_x = 9R_{\mathrm{u}}$$



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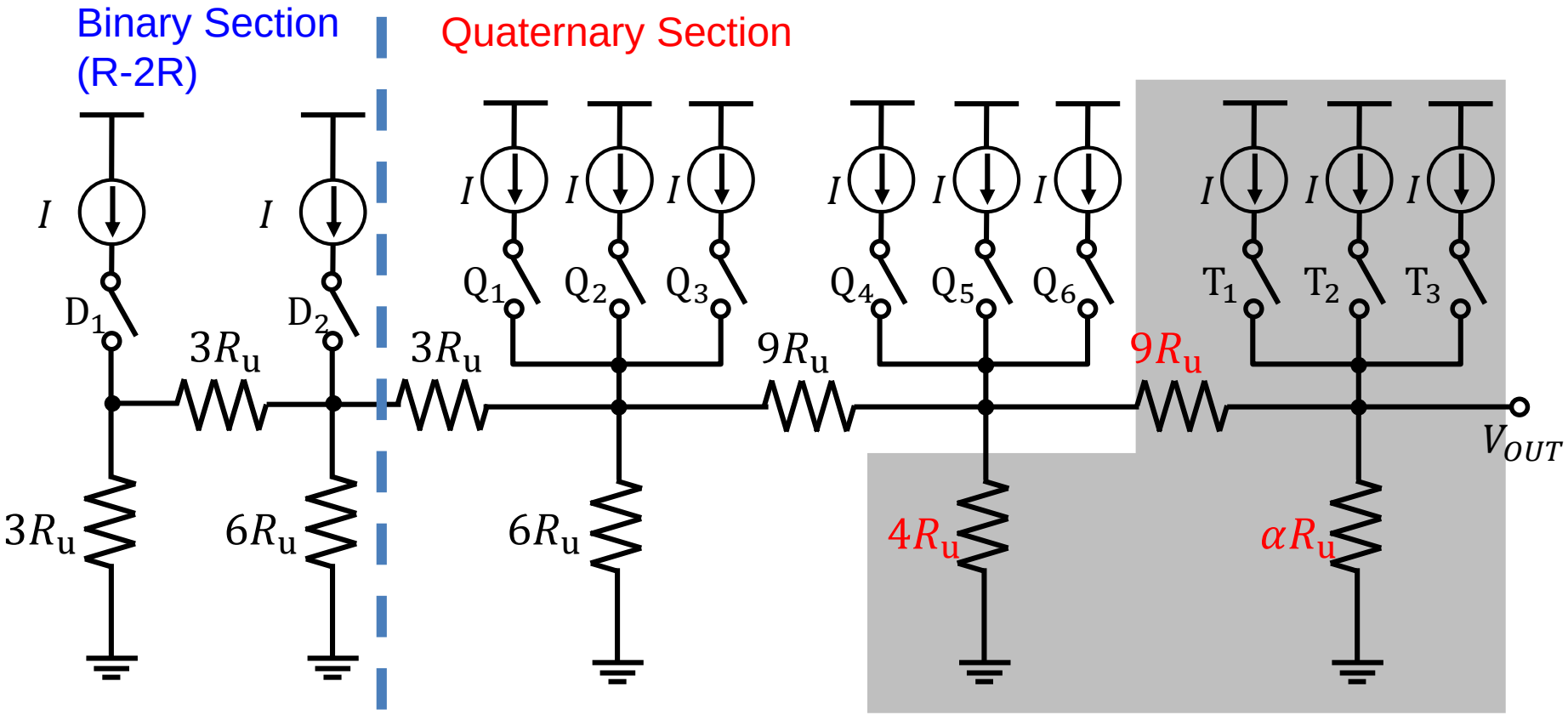
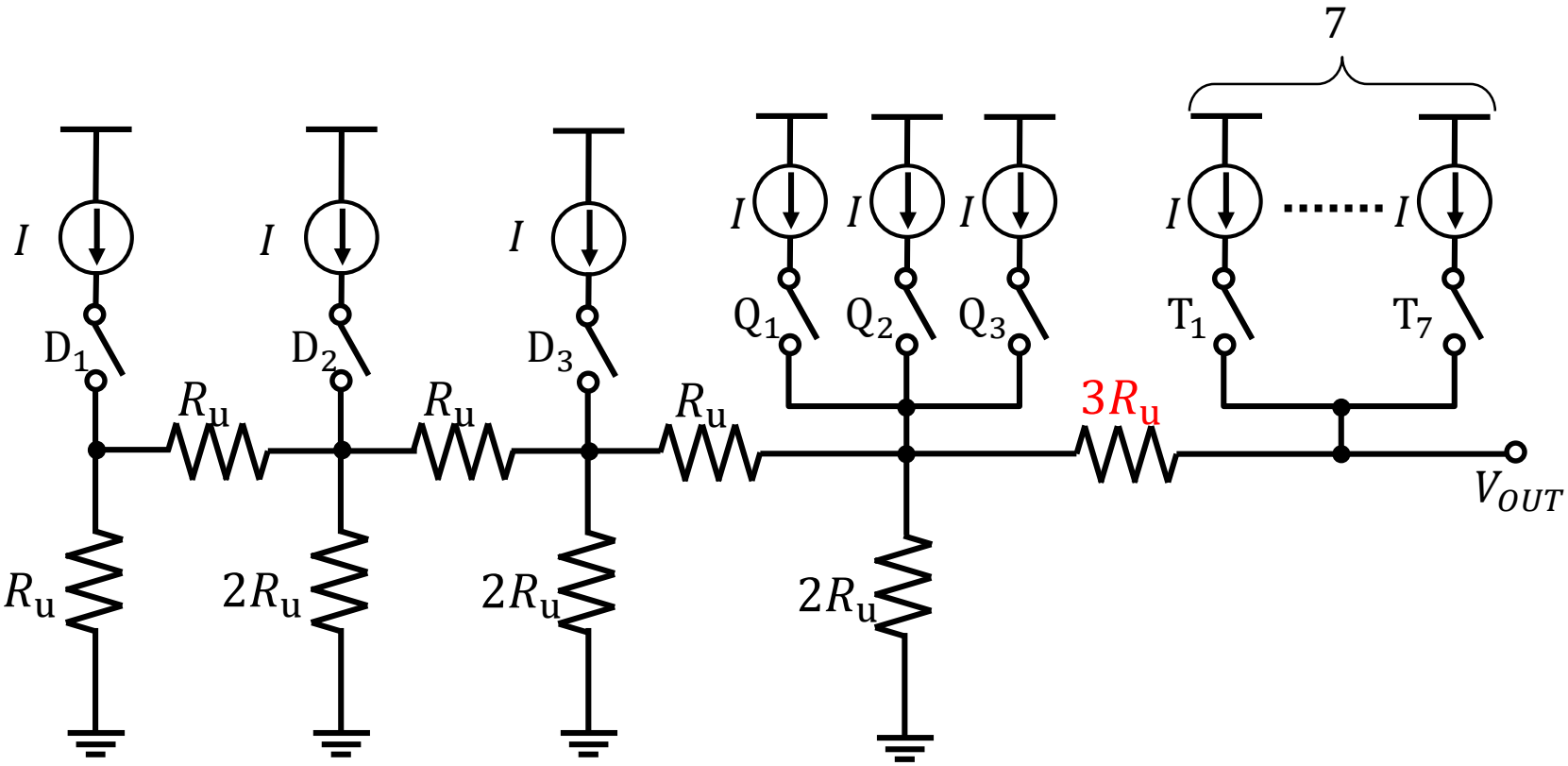
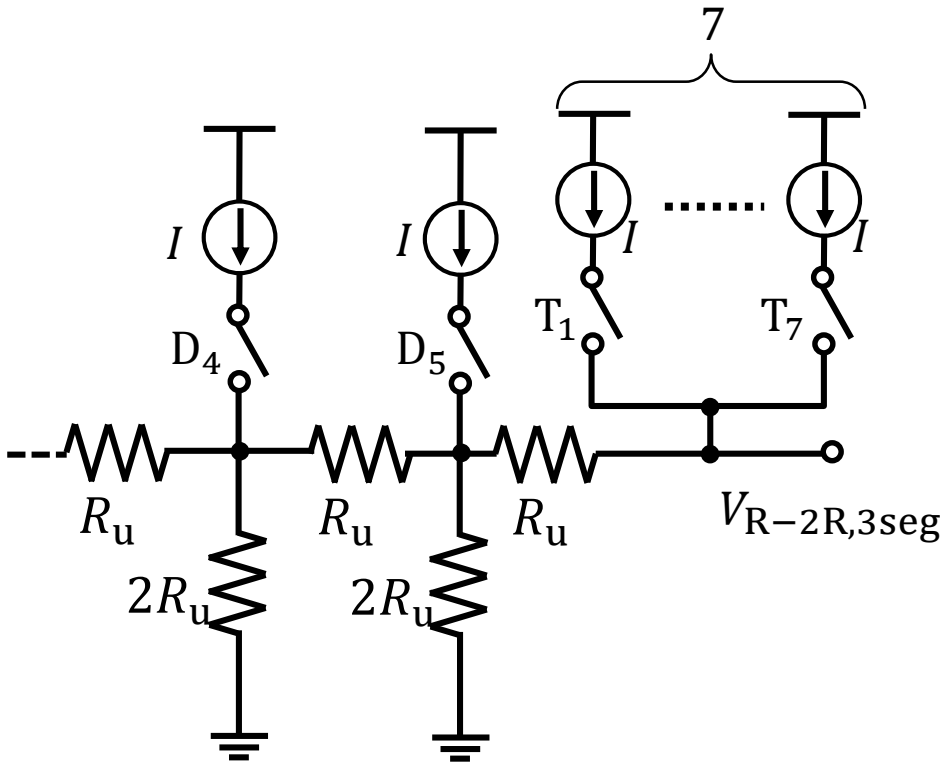


2-4-unary Connected Resistor Ladder

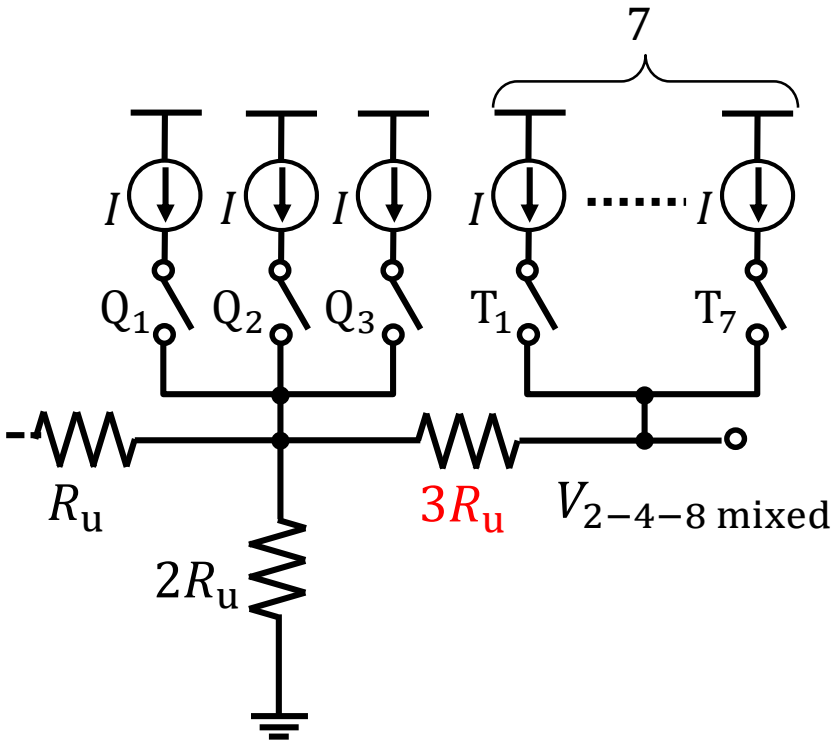


- $3R_u$ between upper and quaternary parts
  - Circuit area is the same as segmented R-2R
  - Additional thermometer decoder for 2 bits of D_4, D_5

Comparison



segmented R-2R current-steering DAC



binary-quaternary-unary connected resistor ladder

$$V_{\mathrm{R-2R,3seg.}} = \frac{1}{16} R_{\mathrm{u}} I \cdot \left\{ \sum_{\mathrm{p}=1}^{5} \left(\mathrm{D_p} \cdot 2^{\mathrm{p}-1} \right) + 32 \sum_{\mathrm{r}=1}^{7} \mathrm{T_r} \right\}$$

$$V_{\mathrm{2-4-8\ mixed}} = \frac{1}{8} R_{\mathrm{u}} I \cdot \left\{ \sum_{\mathrm{p}=1}^{3} \left(\mathrm{D_p} \cdot 2^{\mathrm{p}-1} \right) + 8 \sum_{\mathrm{q}=1}^{3} \mathrm{Q_q} + 32 \sum_{\mathrm{r}=1}^{7} \mathrm{T_r} \right\}$$

Double the gain with the same circuit area

DNL Calculation

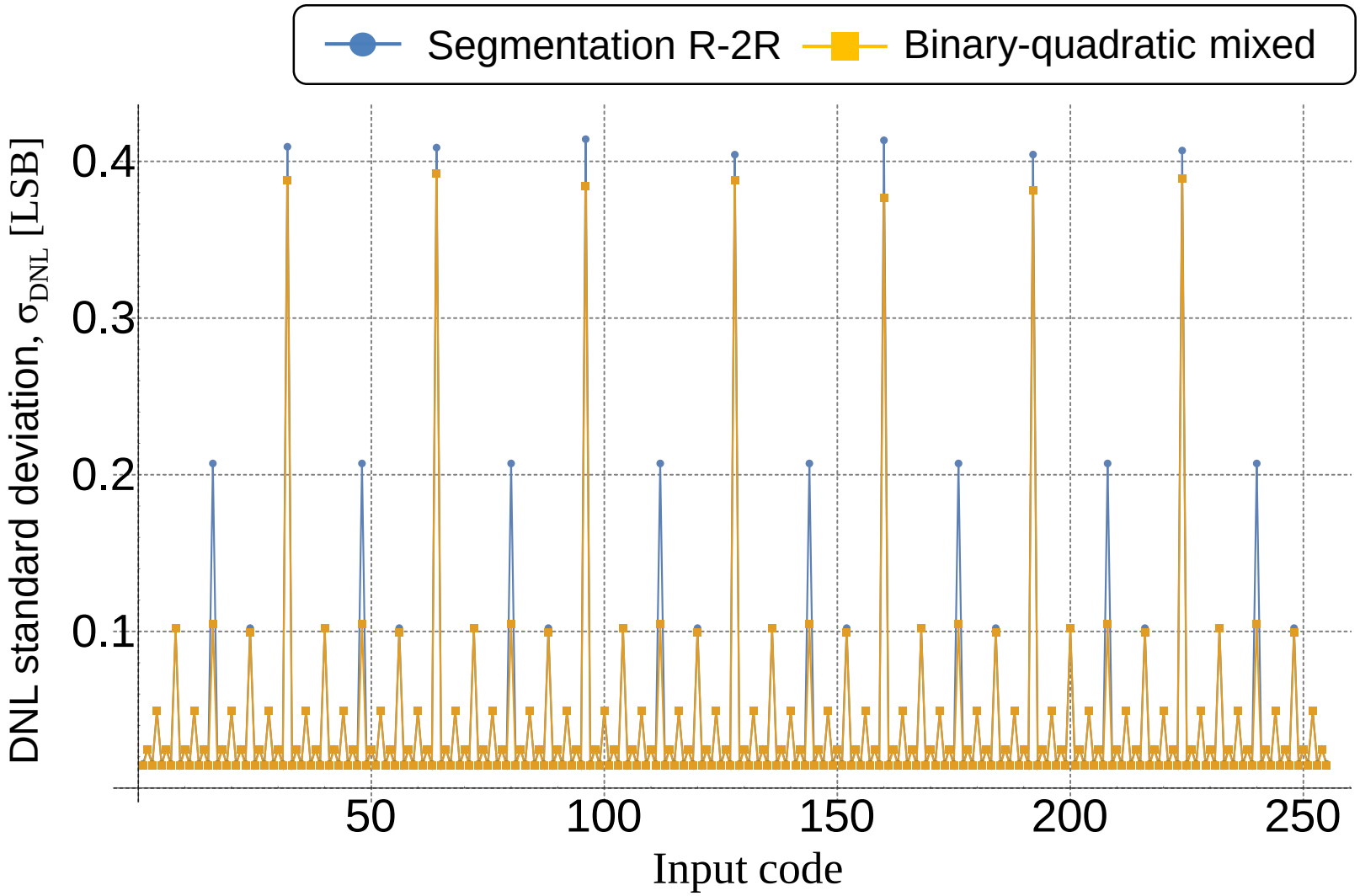
- DNL Definition

$$DNL(n) = \frac{V_{\mathrm{OUT}}(n) - V_{\mathrm{OUT}}(n-1)}{V_{\mathrm{LSB}}} - 1 \quad \text{[LSB]}$$

V_{LSB} : 1 LSB voltage

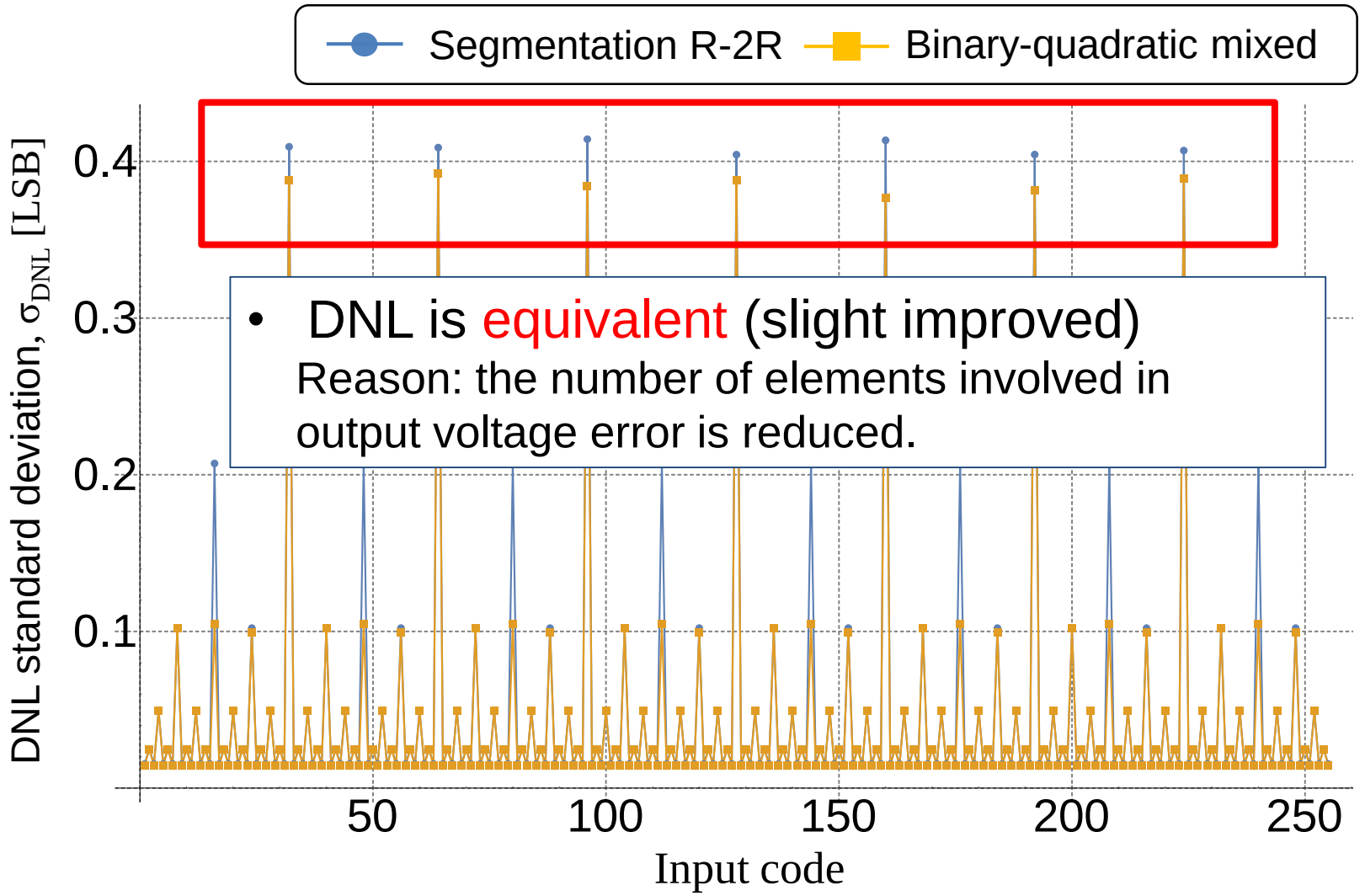
- Simulation conditions
  - Monte Carlo simulation assuming a linear circuit model consisting of resistors and current sources.
  - Number of simulation sets : 3000
  - Assume variations with Gaussian distribution in unit resistance R_{u} and unit current I
  - Standard deviation σ ⇒ 1% of the mean value

DNL Standard Deviation



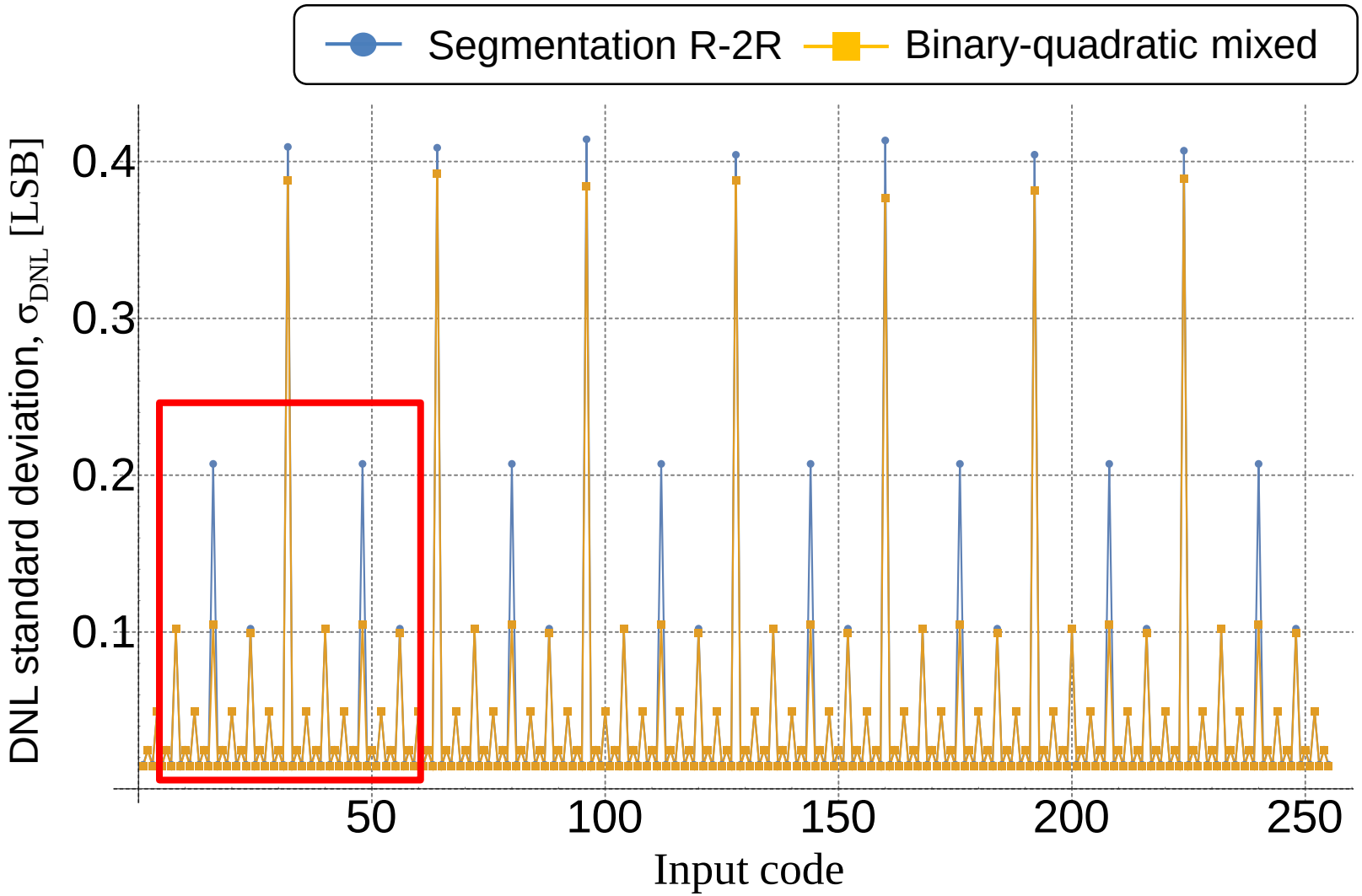
DNL Standard Deviation

- Maximum DNL



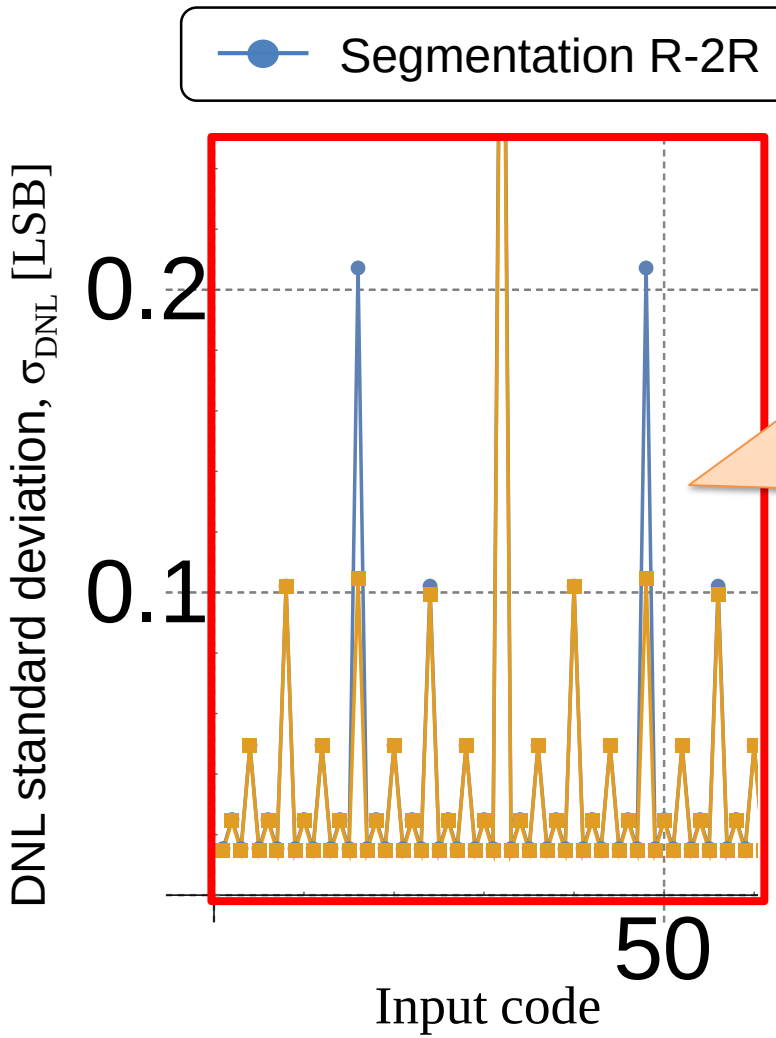
DNL Standard Deviation

- DNL with codes driving quadratic part



DNL Standard Deviation

- DNL with codes driving quadratic part



- Improved DNL with one-step quadrant equivalent code
- Equivalent to segmentation of intermediate bits

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Conclusion

- Summary
  - DACs with resistor ladders
    with non-uniform current sharing ratios
  - Segmentation between upper and lower bits
    is possible in a DAC using a resistor ladder
  - Binary-quaternary-unary connected resistor ladder DAC can increase gain with equivalent size and DNL to a conventional segmented R-2R DAC
- Challenges
  - Dynamic characteristics of the design should be evaluated including associated circuits

Q&A

Q. ゲインの値は最大どこまで取れますか、また制限はありますか。
消費電力や安定性、線形性の制限はありますか。

A. 質問頂いた内容に関して、検討を行っていないため今後の検討課題と致します。