Design Considerations for MOS Peaking Current Sources Insensitive to Supply Voltage and Temperature

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Abstract— **This paper describes MOS peaking current sources (Nagata current sources) insensitive to temperature as well as supply voltage. First, cross-point gate voltage V_{CP} is simulated and analyzed, where the drain current is insensitive to temperature. Our SPICE simulations with TSMC 0.18μm parameters show that V_{CP} depends on the channel width W, the channel length L and the drain source voltage V_{DS}; the reasons for this are analyzed based on BSIM3v3 model. MOS peaking current sources are then designed using NMOSFETs and PMOSFETs where the peak output voltages are insensitive to temperature. We show that MOS peaking current sources insensitive to temperature at the peak output current can be designed by utilizing MOSFET drain current temperature characteristics, and relatively large L, W, and cascode circuit for constant V_{DS} can realize robust MOS peaking current sources. Further, we show that those with multiple peaks make the circuit design easier than single-peak devices.**

Keywords: ***Reference current source, Nagata current source, Peaking current source, Temperature insensitivity, BSIM3***

I. INTRODUCTION

Many analog IC applications require just one reference current/voltage source [1]. As the other current sources are generated from the reference current/voltage, the reference source should be stable against changes in the environment.

One example is the peaking current mirror invented by Minoru Nagata in 1966 [1, 2]; it is now widely used as a simple current source without start-up circuit. It was originally a bipolar transistor circuit, but now it is implemented as a MOS IC. It does not require parasitic bipolar transistors and an operational amplifier, compared to a bandgap reference circuit; some CMOS processes do not guarantee the parasitic bipolar transistor quality, but the peaking current source can be used even there.

Its circuit and simulation results are shown in Fig. 1. With NMOSFETs, its output current has a peak with respect to the supply voltage (or the input current). When it is biased at the vicinity of the peak, its output current changes only slightly with respect to the input current. Here it is assumed that the output voltage V_{OUT} is a constant for simplicity, though it would be reliant on V_{DD} depending on the load circuit.

It is desirable to have also temperature insensitive characteristics of the output current. Conventional bipolar and MOS peaking current sources realize the temperature-insensitive characteristics by using a resistor with a positive temperature coefficient [3]. However, this approach is not always possible inside an IC, and sometimes an external resistor with positive temperature coefficient has to be used. Our solution is a multiple-peak current source insensitive to temperature as well as the supply voltage, where the temperature coefficients of the resistors can be positive, negative or zero provided their coefficient values are known [4]; cross-point gate voltage V_{CP} is fully utilized, where the drain current is insensitive to temperature.

In this paper, we show that even single-peak MOS Nagata current sources can be insensitive to temperature at the peak output current. Also, the characteristics of cross-point voltage V_{CP} are analyzed with SPICE simulations using TSMC 0.18um CMOS parameters as well as the BSIM3v3 model [5]. It is shown that as W decreases, V_{CP} decreases due to the narrow channel effect, and as L decreases, V_{CP} increases due to the short channel effect, while as V_{DS} increases, V_{CP} decreases due to the Drain Induced Barrier Lowering (DIBL) effect. Hence, it is shown that robust current sources with constant V_{DS} can be realized with relatively large W and L. Further, it is relatively easy to realize multiple-peak current sources with temperature and supply voltage insensitivity. Also, reference current sources of the source-type with PMOSFETs and the sink-type with NMOSFETs are shown.

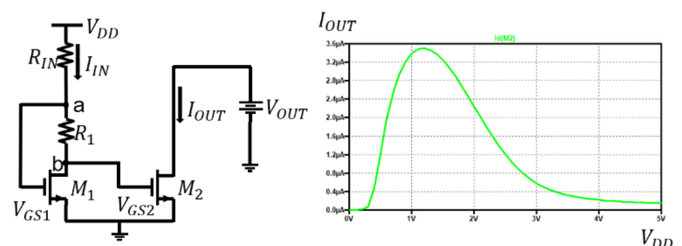


Fig. 1. Original Nagata current source and its simulation result.

II. TEMPERATURE CHARACTERISTICS OF MOSFET

Fig. 2 plots the NMOSFET drain current temperature characteristics. We see that there is a fixed operation point (V_{CP}) insensitive to temperature. When the gate voltage is lower than V_{CP}, the drain current becomes large at high temperature due to the threshold voltage (V_T) decrease, whereas when the gate voltage is higher, the drain current becomes small at high temperature due to the electron mobility (μ) decrease. We use this feature proactively to realize a Nagata current source with temperature insensitivity.

First, we show SPICE simulation results of the VCP dependency on L, W and VDS; they are then analyzed using BSIM3v3 CMOS model. Both results agree well.

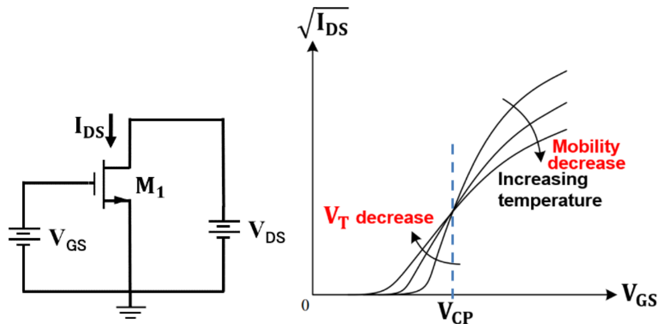


Fig. 2. Drain current temperature characteristics of NMOSFET.

2.1 SPICE Simulation

We have performed SPICE simulations using TSMC 0.18µm CMOS parameters of the level 49 MOS model (Figs. 3, 8), and the following are observed for both NMOSFET and PMOSFET.

(i) As the channel length L increases, VCP decreases. (NMOS case in Fig. 4, PMOS case in Fig. 9.)
(ii) As the channel width W increases, VCP increases. (NMOS case in Fig. 5, PMOS case in Fig. 10.)
(iii) As the drain-source voltage VDS increases, VCP decreases. (NMOS case in Fig. 6, PMOS case in Fig. 11.)
(iv) dVGS/dT < 0 for VGS < VCP. dVGS/dT > 0 for VGS > VCP. (NMOS case in Fig. 7, PMOS case in Fig. 12.)

(A) NMOSFET case

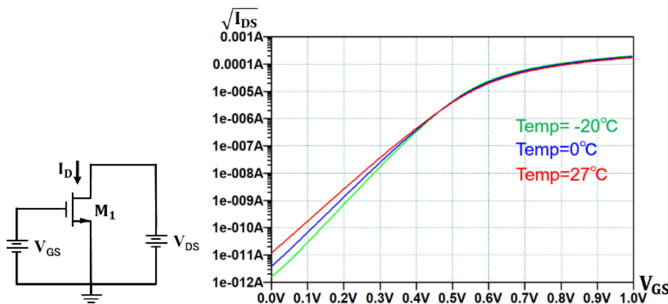


Fig. 3. Drain current characteristics with respect to VGS for W=1µm, L=0.18µm, VDS=0.5V, VCP=461mV.

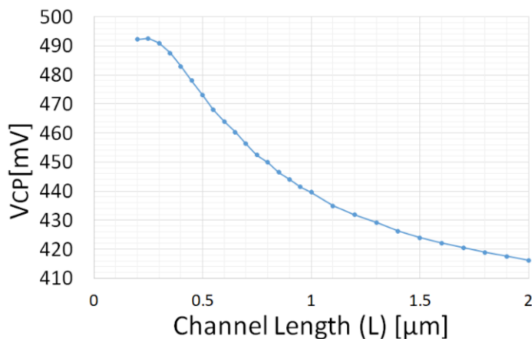


Fig. 4. VCP with respect to the channel length L for W=4µm, VDS=0.5V

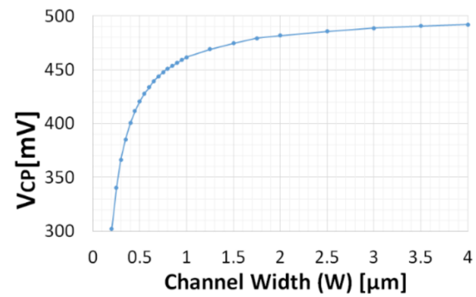


Fig. 5. VCP with respect to the channel width W for L=0.18µm, VDS=0.5V.

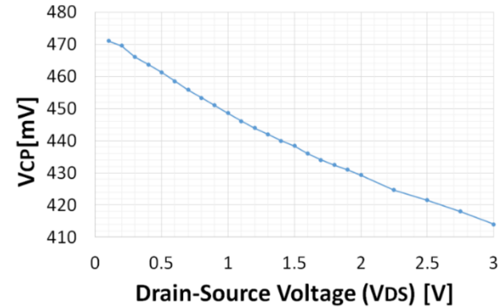
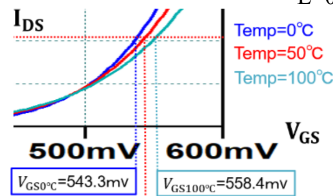


Fig. 6. VCP with respect to the drain-source voltage VDS for W=1µm, L=0.18µm

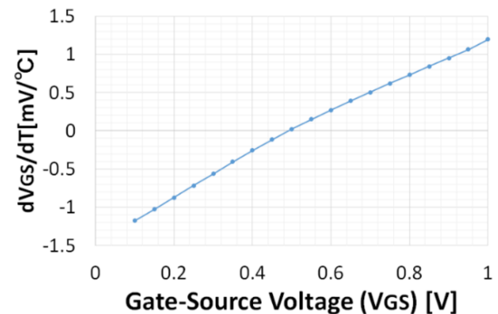


$$dV_{GS0\sim50℃}/dT = \frac{V_{GS50℃} - V_{GS0℃}}{50-0} = \frac{550-543.3}{50} = 0.134$$

$$dV_{GS50\sim100℃}/dT = \frac{V_{GS100℃} - V_{GS50℃}}{100-50} = \frac{558.4-550}{50} = 0.168$$

$$dV_{GS}/dT = \frac{0.134+0.168}{2} = \mathbf{0.151mV/℃}$$

(a)



(b)

Fig. 7. For a given drain current ID, the temperatue coefficent of dVGS/dT is obtained with respect to VGS for W=4µm, L=0.18µm, VDS=0.5V.

(B) PMOSFET case

Figs. 8-12 shows the simulation results for the PMOS case.

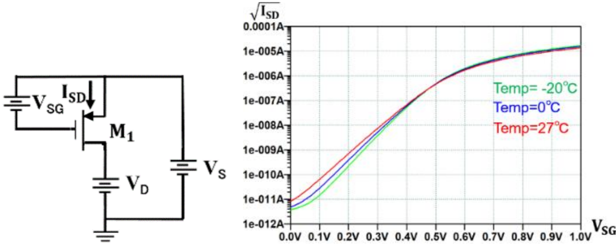


Fig. 8. Drain current characteristics with respect to V_{SG} for W=0.2μm, L=0.18μm, V_{SD}=0.5V, V_{CP}=479mV.

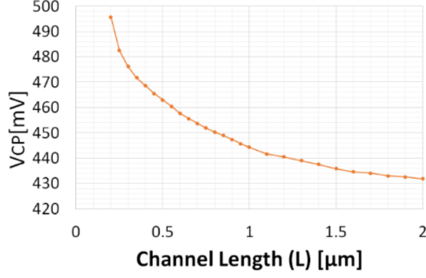


Fig. 9. V_{CP} with respect to the channel length L for W=4μm, V_{SD}=0.5V.

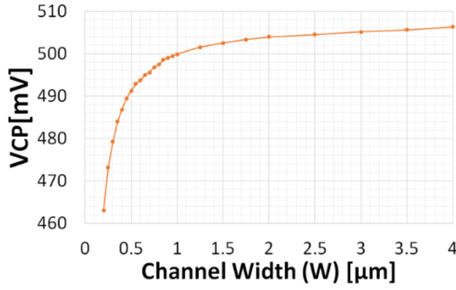


Fig. 10. V_{CP} with respect to the channel width W for L=0.18μm, V_{SD}=0.5V.

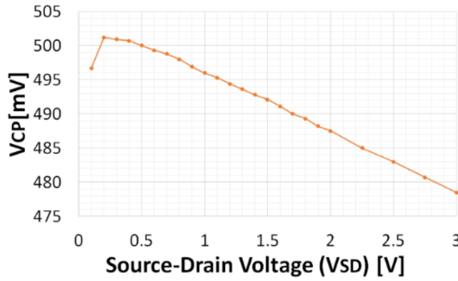


Fig. 11. V_{CP} with respect to the drain-source voltage V_{SD} for W=1μm, L=0.18μm.

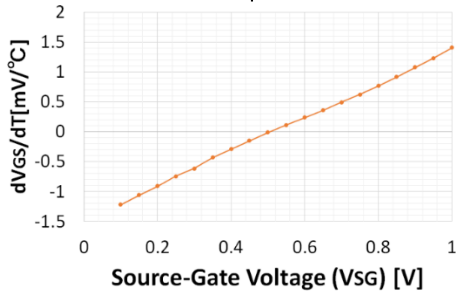


Fig. 12. For a given drain current I_D, the temperatue coefficent of dV_{SG}/dT is obtained with respect to V_{SG} for W=4μm, L=0.18μm, V_{SD}=0.5V.

2.2 Analysis based on BSIM3v3 MOS Model

TSMC 0.18μm CMOS parameters in our simulations are for the level 49 model, which is equivalent to the BSIM3v3 model [6]. Hence this section analyzes the simulation results in Section 2.1 using the BSIM3v3 model in [5].

The drain saturation current at temperature T1 is given by

$$I_{DS1} = \frac{1}{2\alpha}\mu_1 C_{ox}\frac{W}{L}(V_{GS}-V_{T1})^2\big(1+f_1(V_{DS},V_{GS})\big)$$

Here

$$f_1(V_{DS},V_{GS}) = \frac{V_{DS}-V'_{DS}}{V_A},$$

$$\text{for} \quad V_{DS} \geq V'_{DS} \quad \text{and} \quad V'_{DS} = \frac{V_{GS}-V_{T1}}{\alpha}$$

Notice that $f_1(V_{DS}, V_{GS})$ is insensitive to temperature for small V_{DS} and large Early voltage in MOSFET V_A.

Similarly, the drain saturation current at temperature T2 is given by

$$I_{DS2} = \frac{1}{2\alpha}\mu_2 C_{ox}\frac{W}{L}(V_{GS}-V_{T2})^2\big(1+f_2(V_{DS},V_{GS})\big)$$

At the crossover point voltage, V_{CP}, I_{DS1}=I_{DS2} and V_{GS1}=V_{GS2}=V_{CP}, which yields:

$$V_{CP} = \frac{V_{T1} - \sqrt{\frac{\mu_2(1+f_1)}{\mu_1(1+f_2)}}V_{T2}}{1-\sqrt{\frac{\mu_2(1+f_1)}{\mu_1(1+f_2)}}} \approx \frac{V_{T1}-\sqrt{\frac{\mu_2}{\mu_1}}V_{T2}}{1-\sqrt{\frac{\mu_2}{\mu_1}}} = \frac{\sqrt{\mu_1}V_{T1}-\sqrt{\mu_2}V_{T2}}{\sqrt{\mu_1}-\sqrt{\mu_2}}$$

We see that V_{CP} depends on electron mobility μ and threshold voltage V_T. As the temperature increases, μ decreases and V_T decreases.

Threshold voltage V_T is affected by channel length *L* due to the short channel effect and channel width *W* due to the narrow channel effect, as well as the drain-source voltage V_{DS} due to the Drain Induced Barrier Lowering (DIBL) effect:

(i) As channel length *L* decreases, the drain leakage current at high temperature increases further, and hence threshold voltage V_T decreases. Hence V_{CP} increases. Suppose that V_{T1} is the threshold voltage at high temperature and V_{T2} is the one at low temperature. Then V_{T1} >V_{T2}. For short channel *L*, V_{T2} decreases further so V_{CP} increases.

(ii) As the channel width decreases, the drain leakage current decreases, and hence V_T increases. Then V_{CP} decreases. For narrow channel *L*, V_{T2} increases so V_{CP} decreases.

(iii)As drain-source voltage V_{DS} increases, V_T decreases due to the DIBL effects by ΔV_T. From the BISIM3v3 model, we have the following:

$$\Delta V_T = \left[\exp\left(-DSUB\frac{L}{2\lambda}\right) + 2\exp\left(-DSUB\frac{L}{\lambda}\right)\right] \text{x}\left(ETA0 + ETAB\cdot V_{BS,eff}\right)V_{DS}.$$

Here, DSUB, ETA0, and ETAB are fitting parameters and the values specified by the TSMC parameters are used. Also effective bulk-to-source voltage $V_{BS,eff}=0$ is used in the calculations. Also $\lambda = \sqrt{\frac{\varepsilon_s t_{ox} d_B}{\varepsilon_{ox}\beta_3}}$ is the characteristic length with the following parameters: ε_s: permittivity of silicon, ε_{ox}: permittivity of SiO_2, t_{ox}: gate oxide thickness, d_B: depth of depletion region below the channel, β_3: fitting parameter (≒1).

We obtain ΔV_T for *L*=0.18μm as follows:

(i) Calculation from BSIM3v3 model with 1st-order approximation:

V_{CP} (V_{DS}=0.5V) = 462mV
V_{CP} (V_{DS}=2.0V) = 452mV
V_{CP} (V_{DS}=2.0V) – V_{CP} (V_{DS}=0.5V) = - 10mV.

(ii) Simulation results in Fig.6:

V_{CP} (V_{DS}=0.5V) = 462mV
V_{CP} (V_{DS}=2.0V) = 430mV
V_{CP} (V_{DS}=2.0V) – V_{CP} (V_{DS}=0.5V) = - 32mV.

Both resulting V_{CP} values at V_{DS}=0.5V, simulation and calculation, agree well, though those at V_{DS}=2.0V are slightly different. In both cases, ΔV_T is negative and hence we consider that V_{CP} decrease due to V_{DS} increase can be explained by the DIBL effect.

The simulation results in Fig. 7 can be explained as follows: For $V_{GS} > V_{CP}$, as the temperature rises, I_{DS} decreases due to the mobility reduction. Therefore, for constant I_{DS}, $dV_{GS}/dT > 0$. On the other hand, for $V_{GS} < V_{CP}$, $dV_{GS}/dT < 0$ for constant I_{DS}.

III. Reference Current source Design consideration

We consider from the observations in Section II that the design of the reference current or voltage sources insensitive to temperature utilizing the NMOS and PMOS drain current temperature characteristics should obey the following:

(i) For small *L,* the slope $|dV_{CP}/dL|$ is large due to the short channel effect (Figs. 4, 9), which means that V_{CP} would be rather sensitive to process variation. Channel length *L* larger than 1µm may be a good choice to alleviate the process variation effect.

(ii) For small *W*, the slope $|dV_{CP}/dW|$ is large due to the narrow channel effect (Figs. 5, 10), which means that V_{CP} would be rather sensitive to process variation. Channel width *W* larger than 1µm may be a good choice to alleviate the process variation effect.

(iii) V_{CP} varies with V_{DS} (Figs 6, 11), and hence a constant V_{DS} is desirable, such as using a cascode circuit.

IV. Single-Peak current source

(A) NMOSFET case

Fig. 13 shows the NMOS single-peak current source at several temperatures; we see that the temperature insensitivity point (VCP) exists and also that the output current is insensitive to the supply voltage (Vdd).

Fig. 14 shows the output current sensitivity to the output voltage V_{OUT} and also the temperature for the circuit in Fig. 13. We see that the insensitivity point (V_{CP}) changes when V_{OUT} changes, which is not desirable.

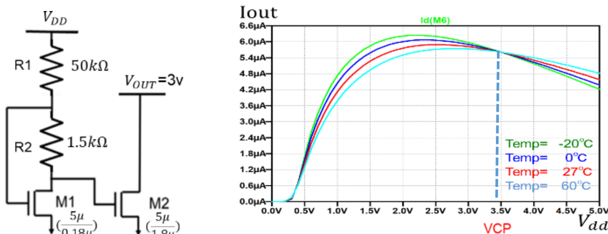


Fig. 13. NMOS single-peak current source and its simulation results for several temperatures.

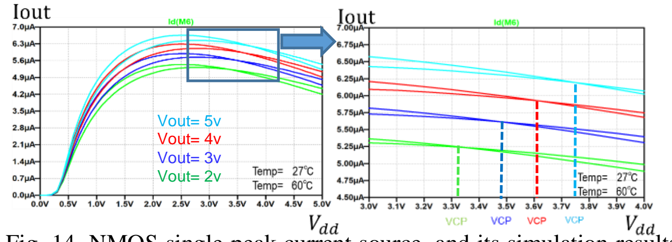


Fig. 14. NMOS single-peak current source, and its simulation results for several output voltages (VOUT) at temperatures at 27°C, 60°C.

Fig. 15 shows the NMOS cascode single-peak current source with several temperatures and we see that the temperature insensitivity point (VCP) exists and there also the output current is insensitive also to the supply voltage (Vdd).

Fig. 16 shows the output current sensitivity to the output voltage V_{OUT} and also the temperature for the circuit in Fig. 15. We see that the insensitivity point (V_{CP}) does not change even when V_{OUT} changes, thanks to the cascode configuration; the drain voltage of M2 remains almost constant, even when V_{OUT} changes.

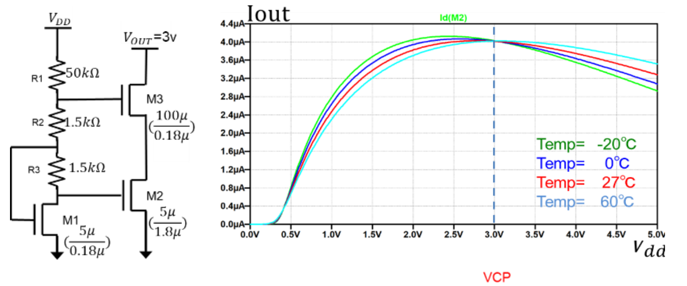


Fig. 15. NMOS cascode single-peak current source and its simulation results for several temperatures.

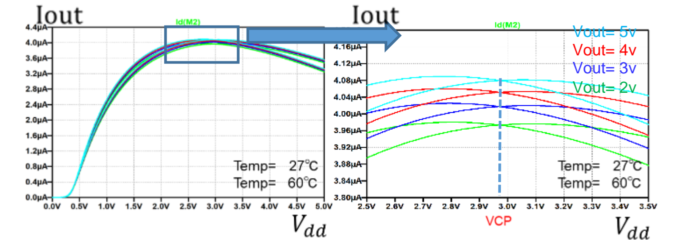


Fig. 16. NMOS cascode single-peak current source, and its simulation results for several output voltages (VOUT) at temperatures at 27°C, 60°C.

(B) PMOSFET case

Fig. 17 shows the PMOS single-peak current source at two temperatures; we see that the temperature insensitivity point exists and also that the output current is insensitive to the supply voltage (Vdd). However, when the load resistor (Rout) is changed, the drain voltage of M2 changes ,and Iout changes due to the channel length modulation effect and the DIBL effect of the threshold voltage. Also its temperature characteristics change due to the temperature dependence of the threshold voltage including the DIBL effect and that of hole mobility in the channel.

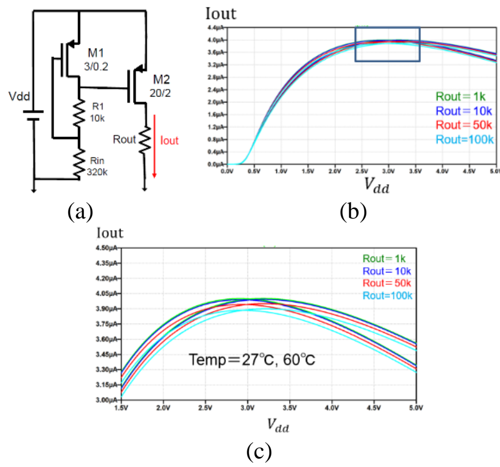


Fig. 17. PMOS single-peak current source, and its simulation results for several values of load resistor (Rout) at temperatures at 27°C, 60°C. (a) Circuit. (b) Simulation results. (c) Enlarged simulation results of the boxed part in Fig. 17 (b).

Fig. 18 shows the PMOS cascode single-peak current source at two temperatures; we see that the temperature insensitivity point exists and that the output current is insensitive to the supply voltage (Vdd). Furthermore, even if the load resistor (Rout) is changed, the drain voltage of M2 changes, but Iout does not change. Note that its temperature characteristics does not change; in Fig. 18 (b), (c), all Iout's for Rout =1k, 10k, 50k, 100k are almost equal and not distinguishable.

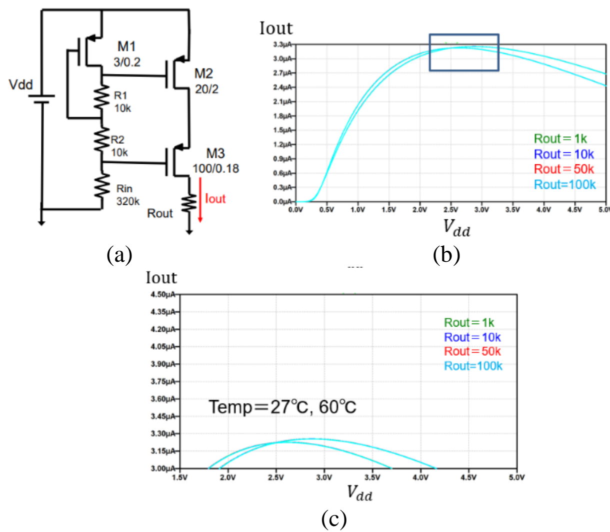


Fig. 18 PMOS cascode single-peak current source, and its simulation results for several values of load resistor (Rout) at temperatures at 27°C, 60°C. (a) Circuit. (b) Simulation results. (c) Enlarged simulation results of the boxed part in Fig. 18 (b).

V. MULTIPLE-PEAK CURRENT SOURCE

Fig. 19 shows an NMOS multiple-peak current source and its simulation results. We see that the output current is insensitive to supply voltage and temperature variations for supply voltage of 2.0V. Using multiple peaking current sources makes it easier to design current sources that are insensitive to temperature and supply voltage. Here the output current is set to be constant using four peaks, but the number of peaks need not be limited to four. The number of peaks, the resistance value, L and W are the degrees of design freedom. This method is applicable whether it is positive or negative, if the resistor temperature coefficient is known.

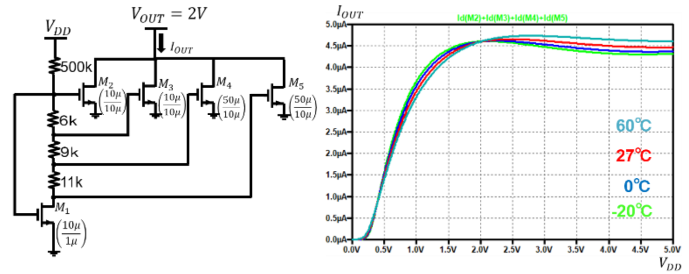


Fig. 19. NMOS multiple-peaking current source and simulation result.

Fig. 20 shows the circuit with cascode connection that allows this circuit to suppress the fluctuation in the output current against the fluctuation of the output voltage (Fig. 21).

Fig. 22 shows a circuit in which the resistor in Fig. 20 is replaced by a drain-gate connected MOSFET. NMOS usage can reduce the chip area.

Fig. 23 shows PMOS multiple-peaking current source and its simulation results for several temperatures. Fig. 24 shows those for various output voltages (VOUT).

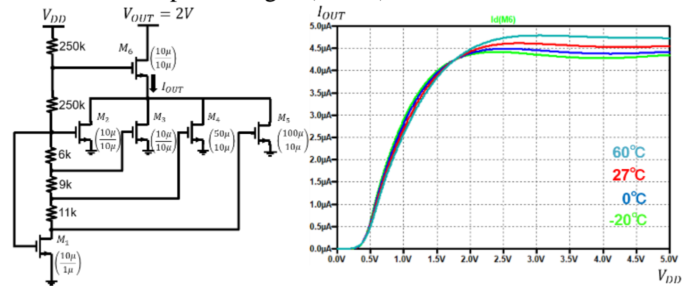


Fig. 20. NMOS cascode multiple-peak current source and its simulation result.

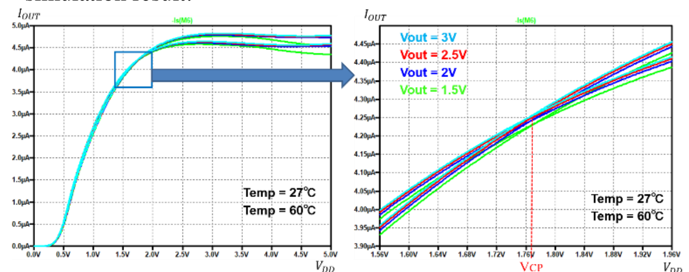


Fig. 21 NMOS cascode multiple-peak current source, and its simulation results for several output voltages (VOUT) at temperatures at 27°C, 60°C.

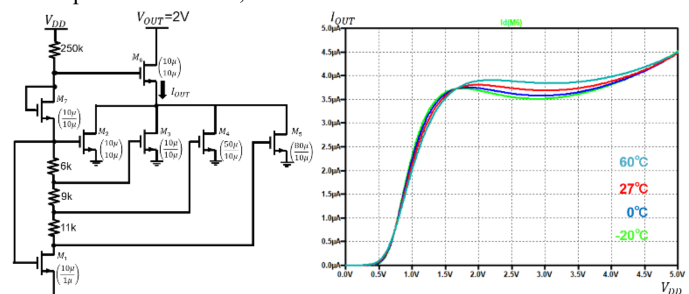


Fig. 22. NMOS cascode multiple-peak current source where the resistor is replaced with MOSFET, and its simulation result.

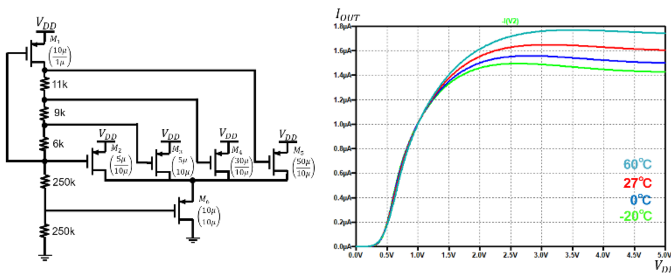


Fig. 23. PMOS multiple-peaking current source and its simulation result.

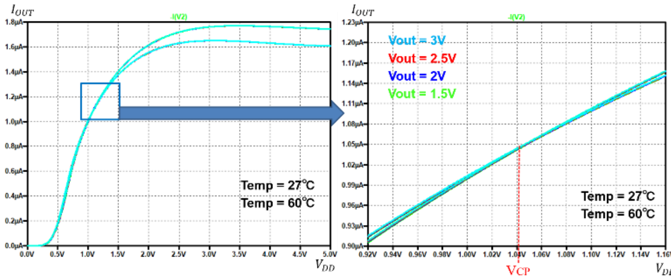


Fig. 24 PMOS cascode single-peak current source, and its simulation results for several output voltages (VOUT) at temperatures at 27°C and 60°C.

VI. CONCLUSION

In this paper, we have described reference current sources that provide a constant output current insensitive to not only power supply voltage but also temperature variation. They use single-peak or multiple-peak current sources with different peaks utilizing MOS drain current temperature characteristics. We have verified their characteristics with SPICE simulations as well as analysis based on CMOS physics and the BISM3 model. The following observations are obtained:

(i) Both NMOS and PMOS peaking current sources insensitive to supply voltage and temperature can be realized if the resistor temperature coefficient values are known *a priori.*

(ii) For small L, the drain current temperature characteristic is sensitive to L variation due to the short channel effect. Then using relatively large L can realize robust circuits from the temperature characteristic viewpoint.

(iii) For small W, the drain current temperature characteristic is sensitive to W variation due to the narrow channel effect. Then using relatively large W can realize robust circuits from the temperature characteristic viewpoint.

(iii) The drain-source voltage (Vds) affects the drain current temperature characteristics, so that Vds of the output current generation MOS should be kept constant, as achieved by using the cascode configuration.

(iv) Multiple-peak current sources make it relatively easy to realize temperature and supply voltage insensitivities, compared to single-peak current sources.

(v) PMOS peaking current sources with temperature insensitivity are relatively difficult to design, compared to the NMOS equivalent.

The following are final remarks:

(i) Single-peak current sources with BJTs cannot use the technique described here. There, as the temperature increases, the output current increases if the temperature coefficient of the resistor is zero or negative.

(ii) Fig. 25 shows variations of MOS peaking current sources and both can be insensitive to supply voltage and temperature.

(iii) We have also designed another MOS reference current source utilizing the cross-point voltage (V_{CP}) characteristics of the MOSFET [7].

(iv) Since $dV_{GS1}/dT < 0$ for $V_{GS1} < V_{CP}$ and $dV_{GS2}/dT > 0$ for $V_{GS2} > V_{CP}$, then reference voltage (V_{REF}) insensitive to temperature such that $V_{REF} = V_{GS1} + V_{GS2}$, $dV_{REF}/dT = 0$ can be realized [8].

(v) The reference current sources designed here are based on both circuit design and MOS device physics as well as s modeling technology, which are essential for designing analog circuits with small numbers of MOSFETs.

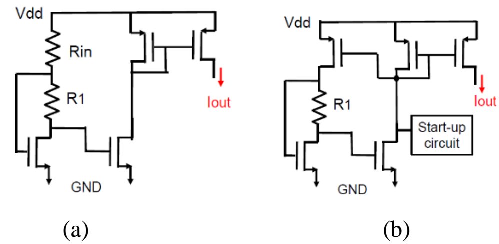


Fig. 25 Variations in MOS peaking current sources. (a) Output current is folded by PMOS current mirror. (b) Self-bias circuit with start-up.

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