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CMOS Reference Voltage Source Using Drain Current Temperature Characteristics

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Outline

- Research Objective
- Temperature Insensitivity
  - Reference Voltage Generator Core
- Supply Voltage Insensitivity
  - Bias Current Generator
- Whole Circuit
- Conclusion

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Research Background

Analog ICs require

Reference voltage source

Stable against PVT variation

P: Process
V: Supply voltage
T: Temperature

Bandgap reference circuit

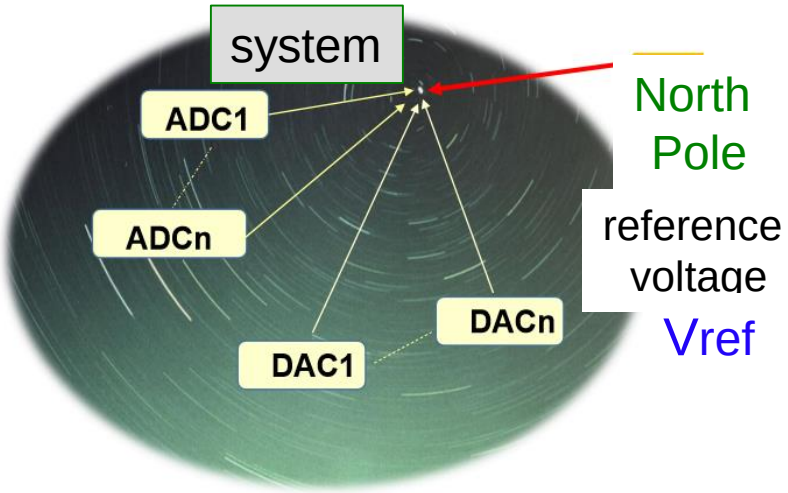
- Complicated
- Large chip area

Proposed voltage source

- Simple
- Insensitive to temperature, supply voltage

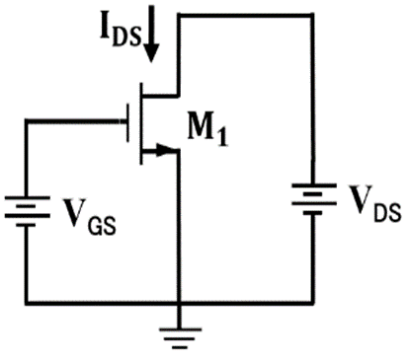
Research Objective

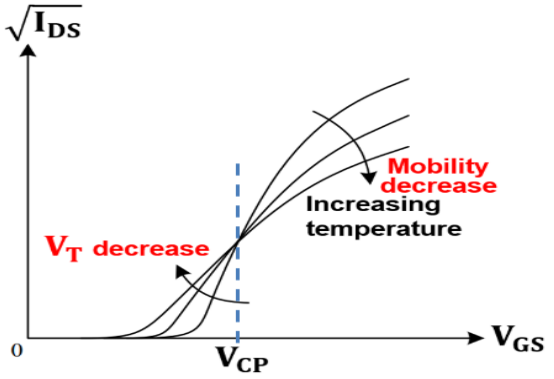
Development of reference voltage source insensitive to temperature and supply voltage with simple CMOS circuit.

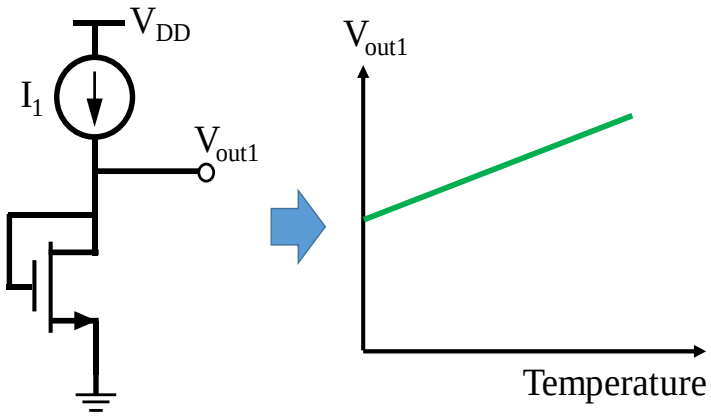


Our Approach: Temperature Insensitivity

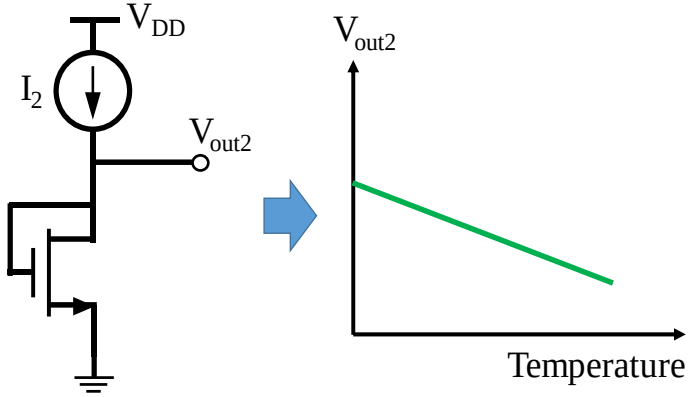
Utilize of
MOS drain current
temperature
characteristics







Vgs > Vcp → Positive TC

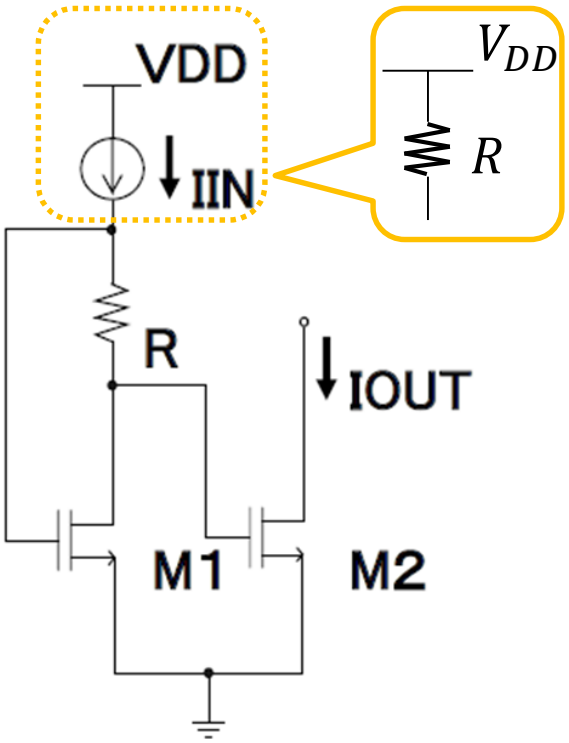


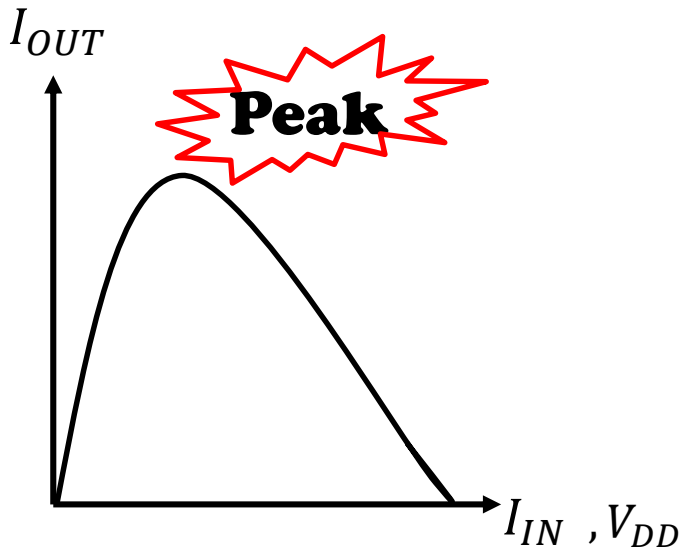
Vcp > Vgs → Negative TC

TC: Temperature Coefficient

Our Approach: Supply Voltage Insensitivity

Utilize of MOS Nagata Current Mirror Circuit





Peaking current characteristics

At peak vicinity

Small output current change
against input current change

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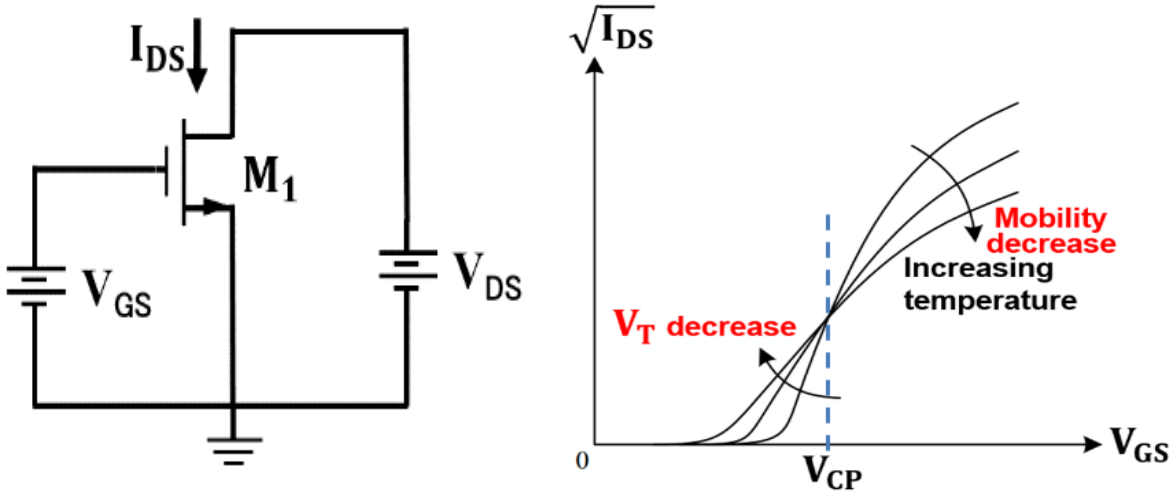
Drain Current Temperature Characteristics



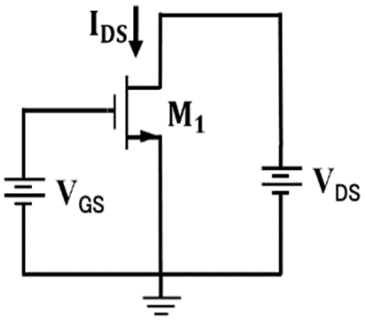
NMOS drain current temperature characteristics

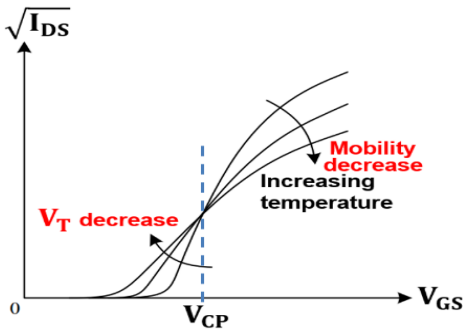
- For $V_{GS} = V_{CP}$, I_{DS} is insensitive to temperature.
  - At high temperature,

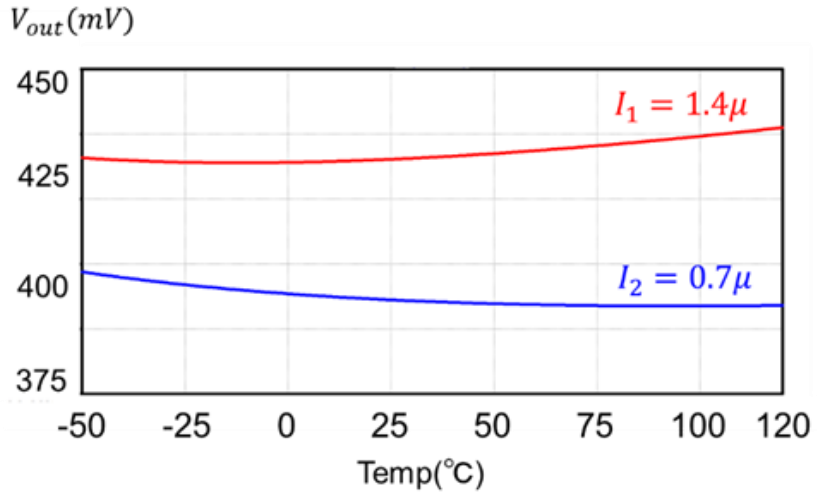
    For $V_{GS} < V_{CP}$, I_{DS} becomes larger

    For $V_{GS} > V_{CP}$, I_{DS} becomes smaller.

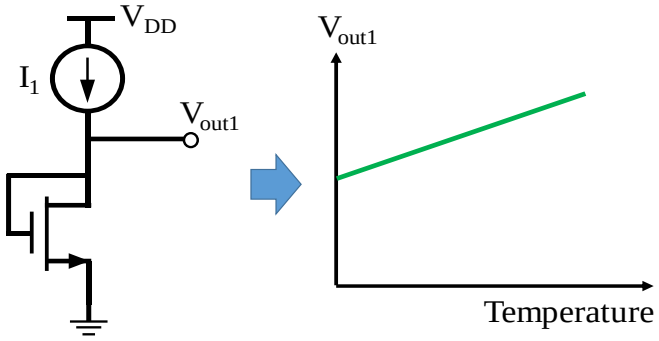
Voltage Source and Temperature



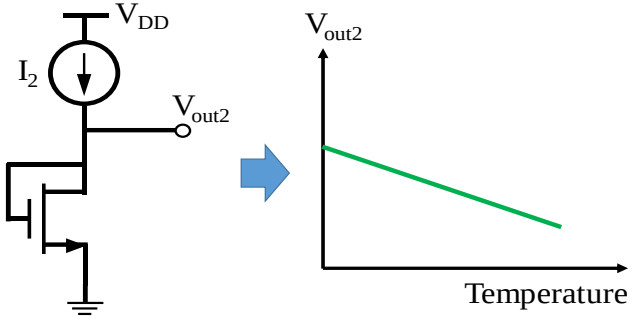




SPICE simulation result



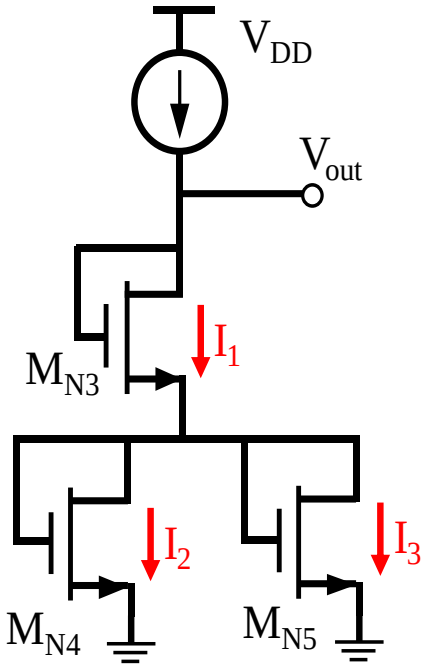
Vgs > Vcp → Positive TC

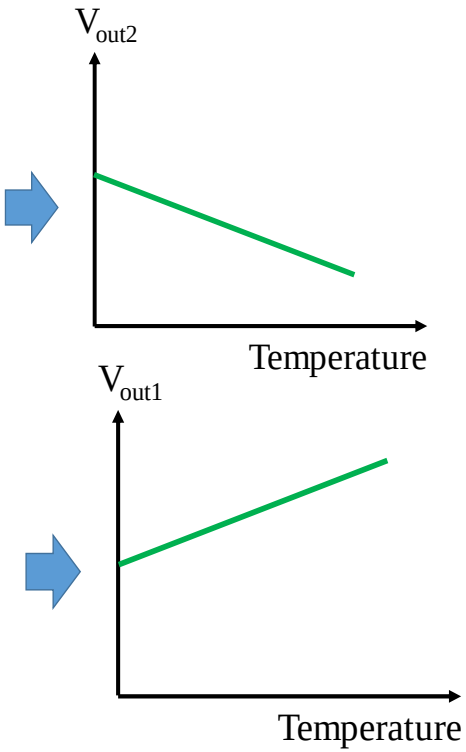


Vcp > Vgs → Negative TC

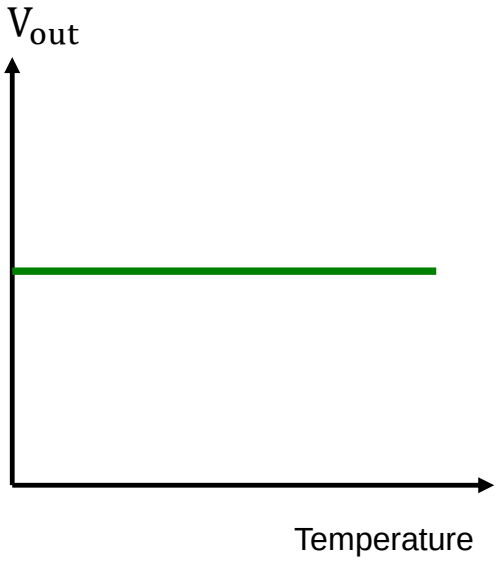
TC: Temperature Coefficient

Temperature Insensitive Voltage Source





$V_{out} = V_{out1} + V_{out2}$



Vgs3 > Vcp → Positive TC

Vcp > Vgs4=Vgs5 → Negative TC

$V_{out} = V_{out1} + V_{out2}$

Cancel temperature dependency

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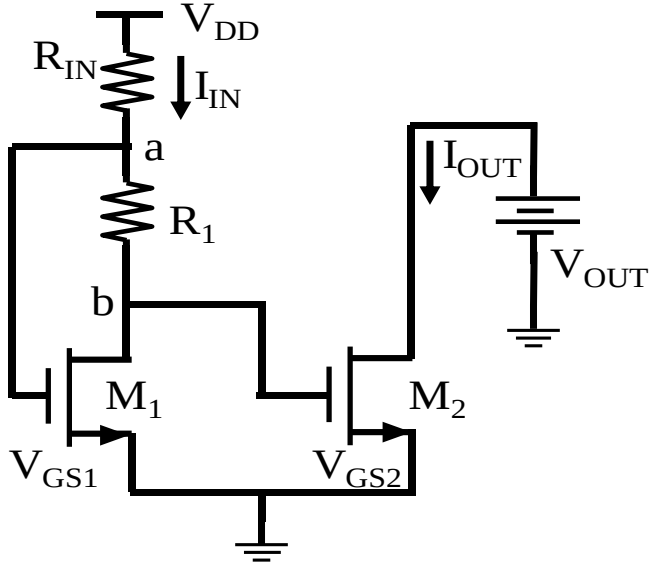
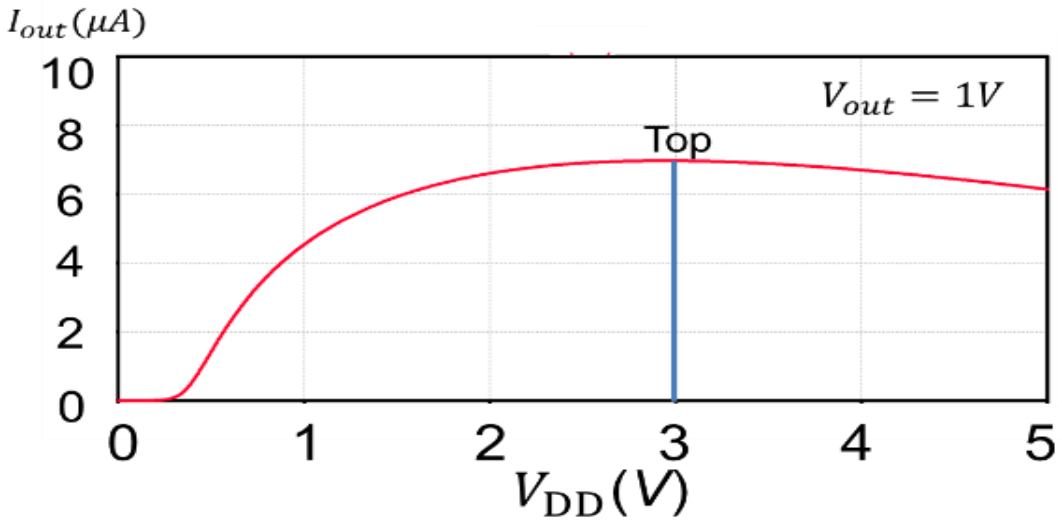
Nagata Current Source:
Supply Voltage Insensitivity

MOS Nagata Current Mirror Circuit

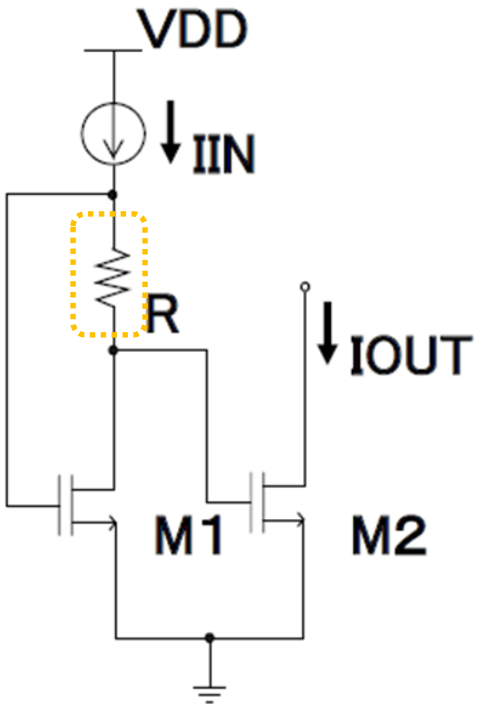


MOS Nagata Current Mirror



SPICE simulation result

Circuit Configuration and Operation(1)

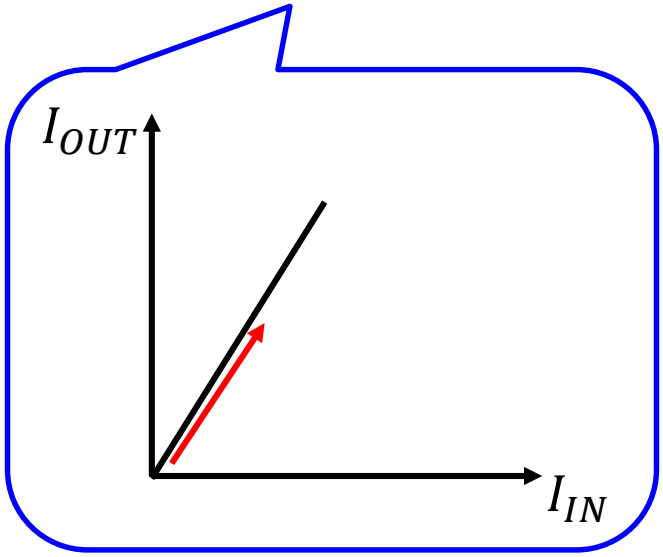


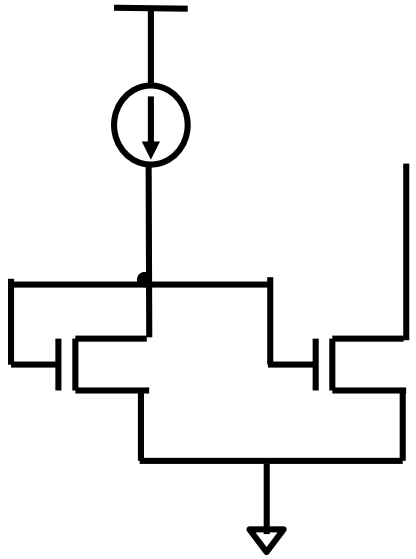
MOS Nagata
Current Mirror

I_{IN}: small

RI_{IN}: small

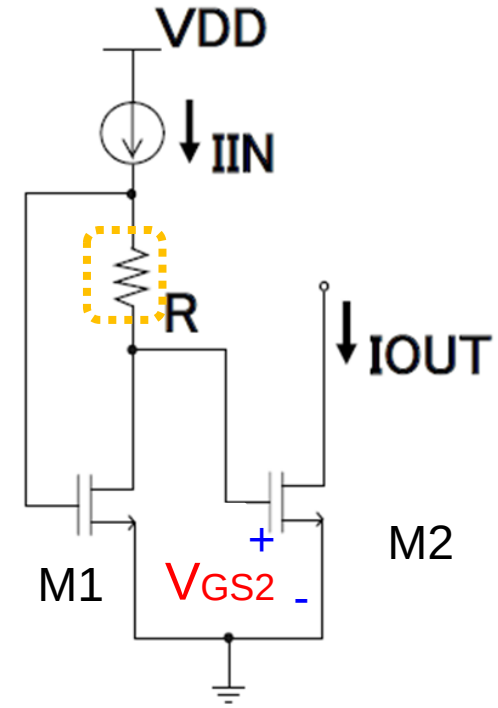
$I_{IN} = I_{OUT}$





Current Mirror

Circuit Configuration and Operation(2)

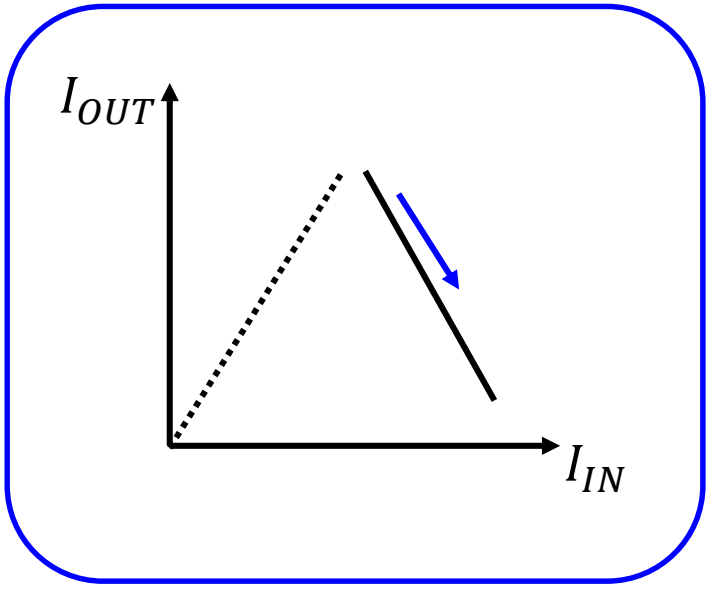


MOS Nagata
Current Mirror Circuit

➡ I_{IN}: $large$

➡ RI_{IN}: $large$

➡ V_{GS2} $becomes$ $smaller$



Temperature characteristics should be also considered.

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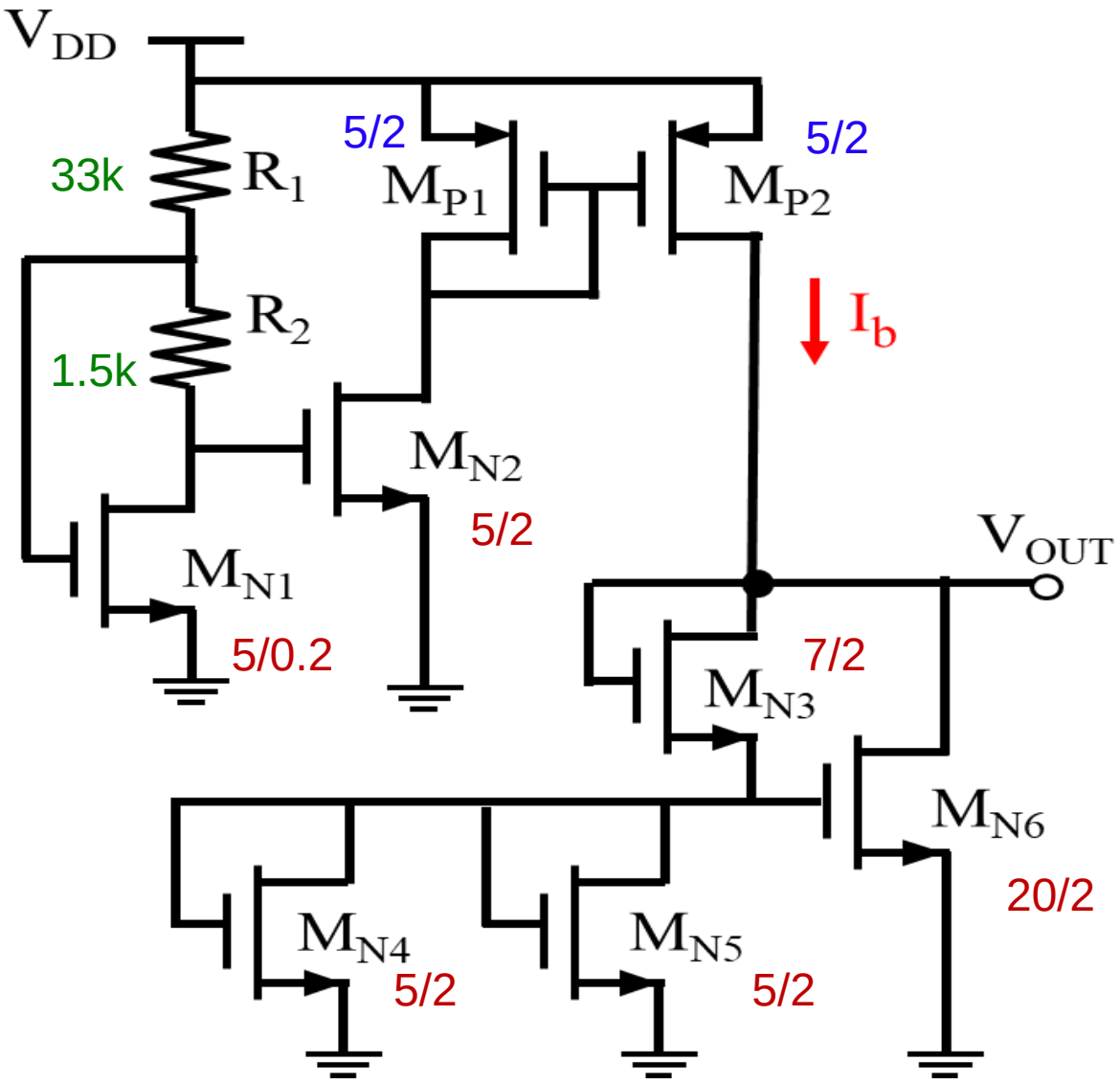
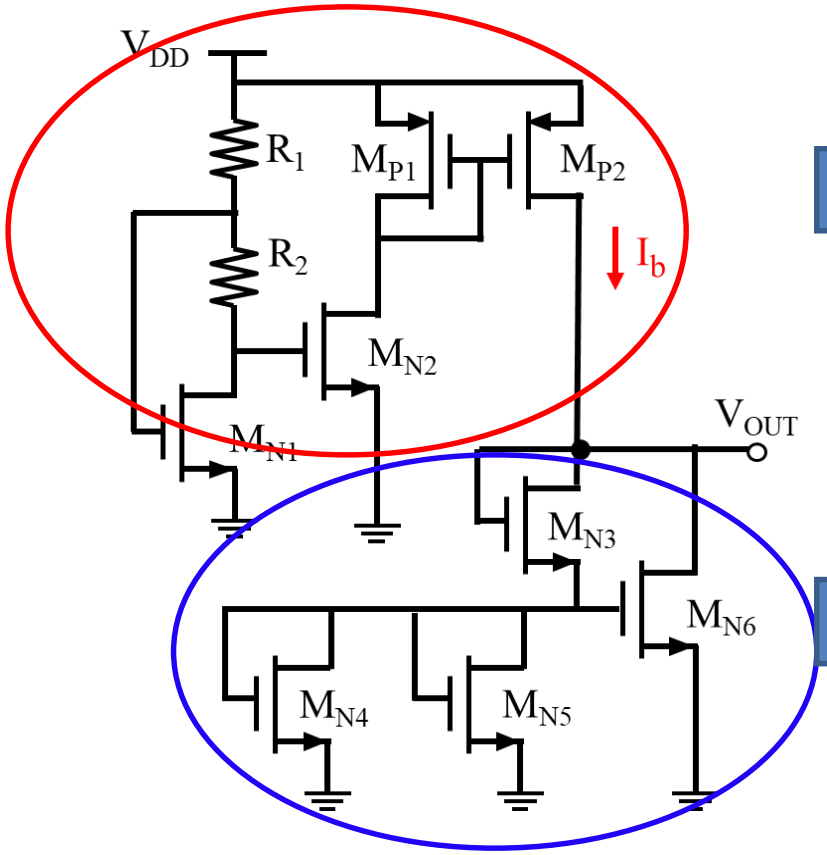
Proposed Voltage Reference



Voltage Reference Configuration



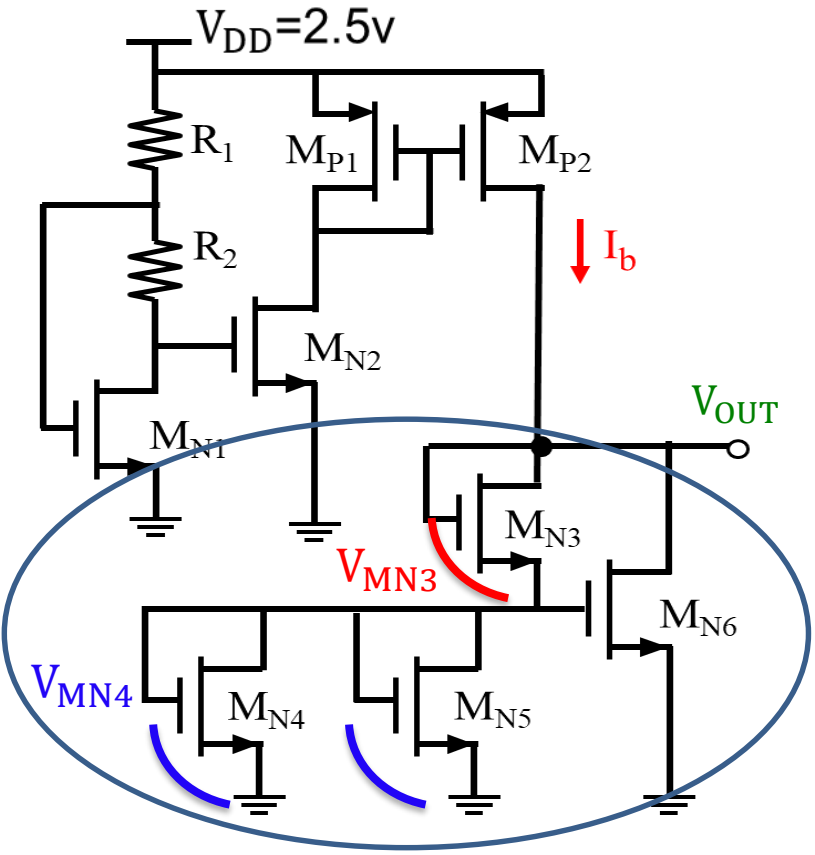
Supply voltage insensitive

Bias current generator

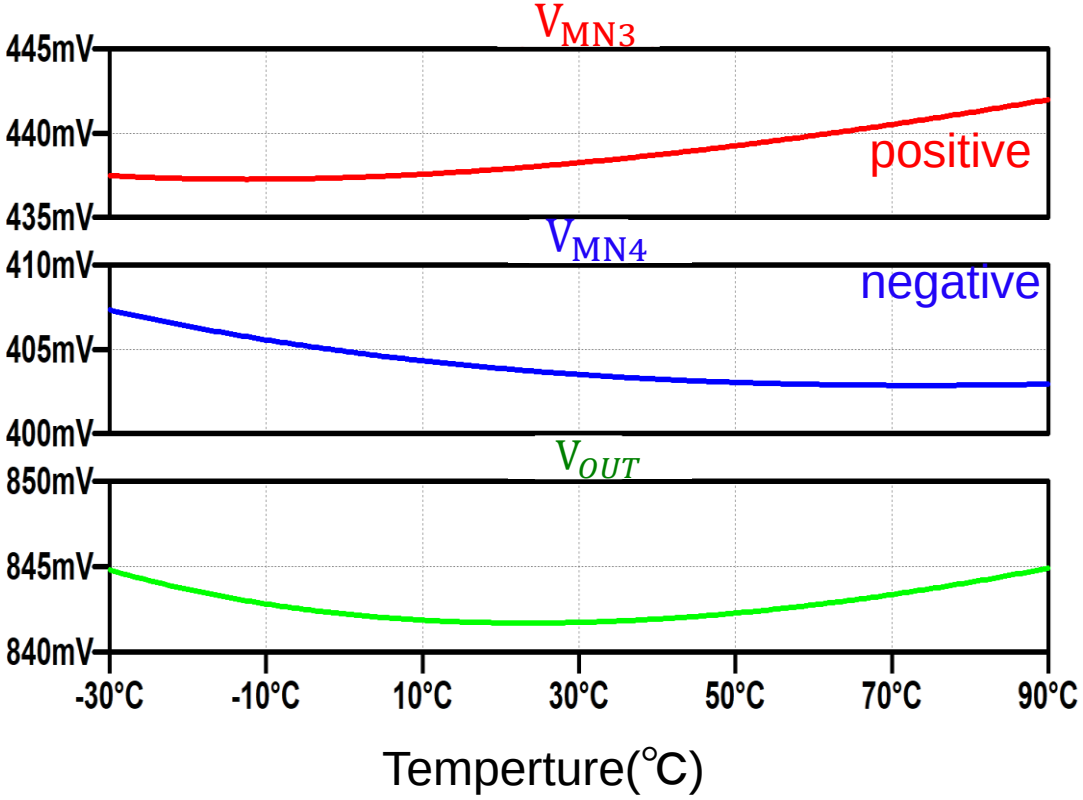
Temperature insensitive

Reference voltage core

Voltage Reference Core



Whole circuit

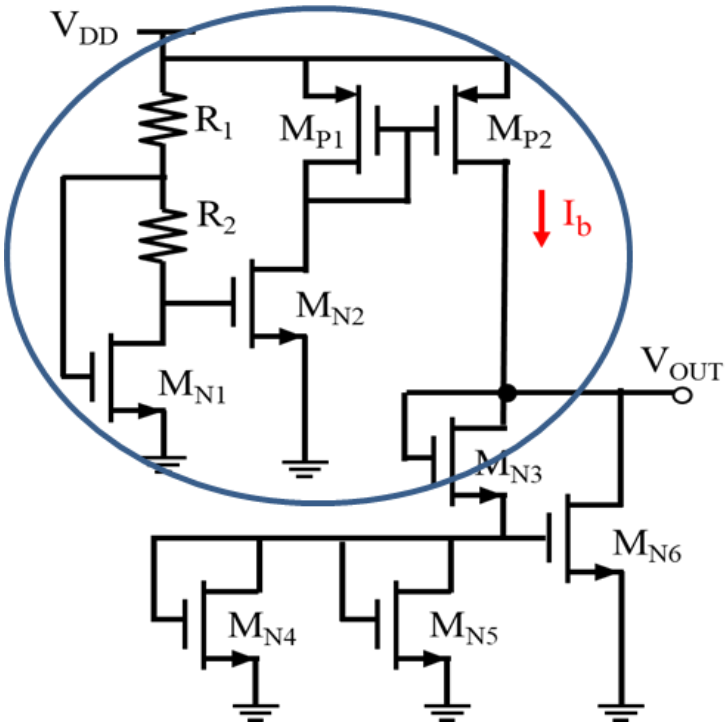


$V_{MN3} > V_{CP} > V_{MN4}$

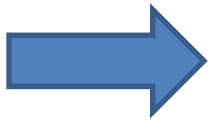
$Vout = V_{MN3} + V_{MN4}$

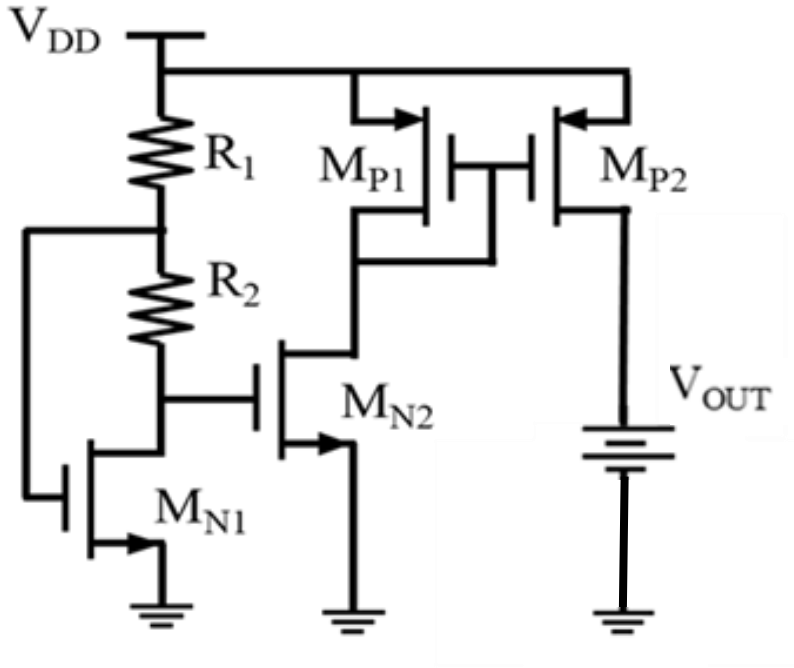
V_{OUT} ➡ Insensitive to temperature

Bias Current Generator



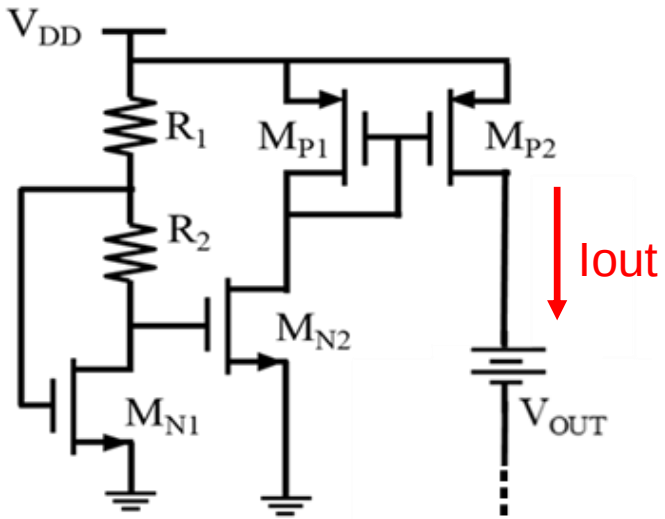
Whole circuit



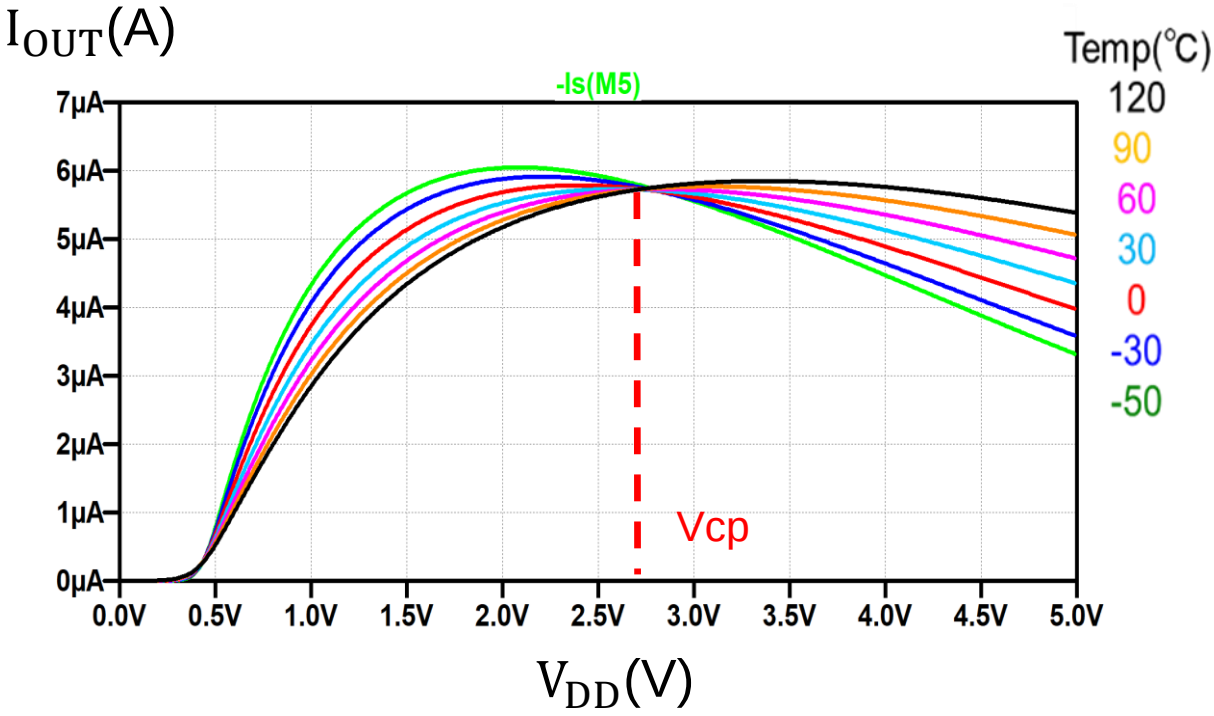


Nagata current mirror

Bias Current Generator:
Temperature Characteristics

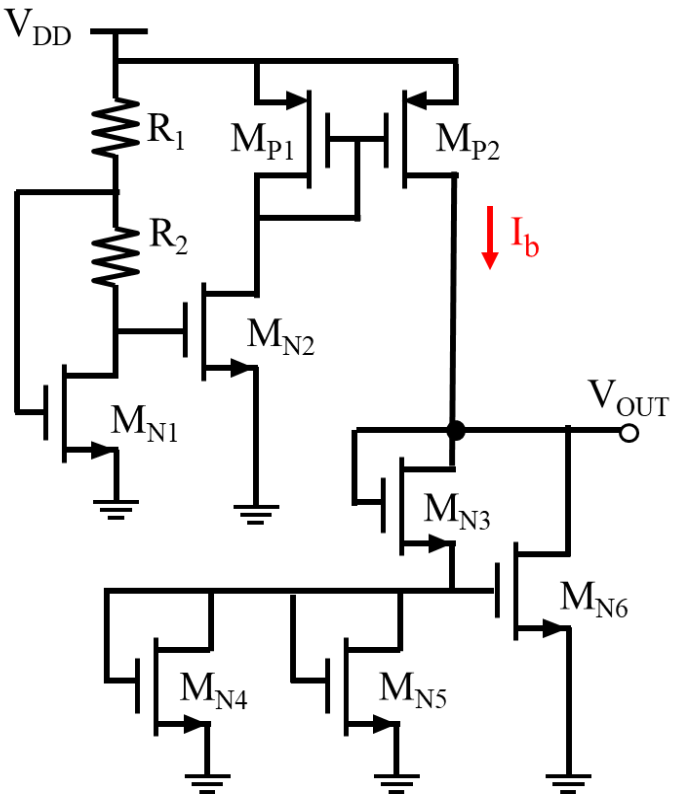


Nagata current mirror

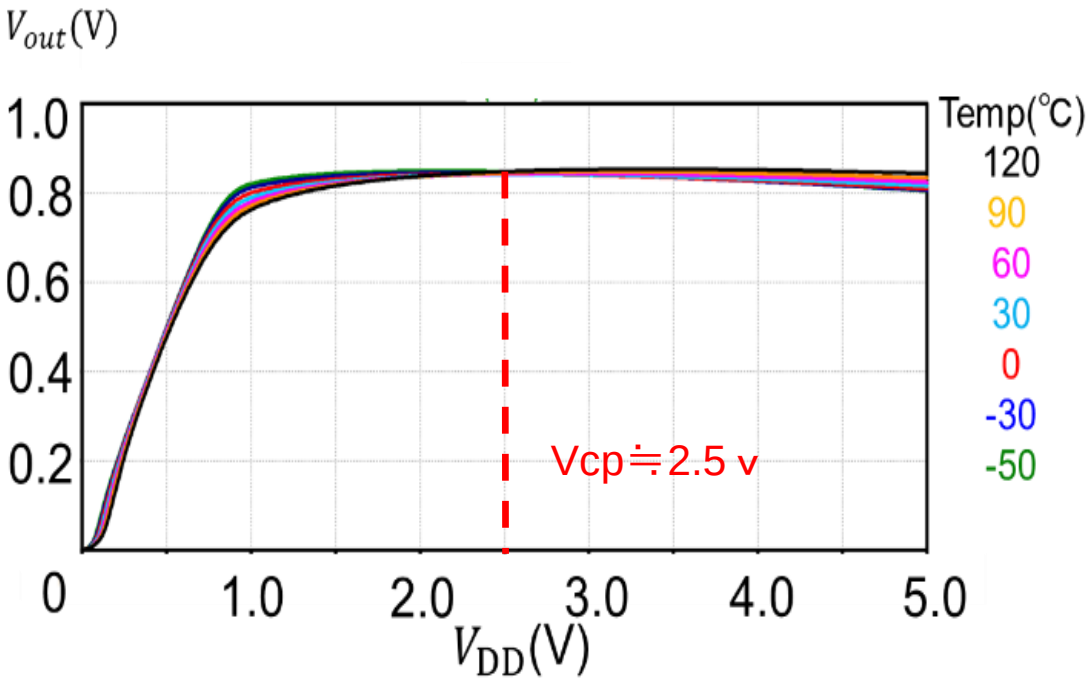


- Mountain shape with a peak point
- V_{CP} can be confirmed

Whole Circuit Simulation Result



Whole circuit

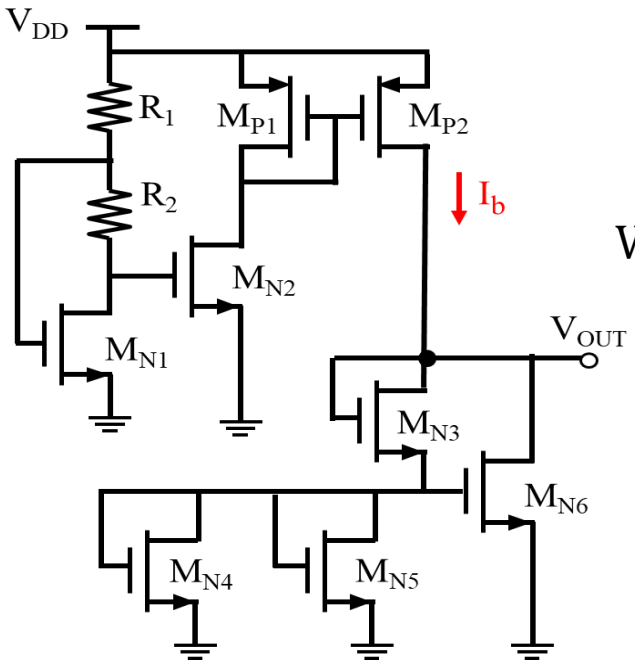


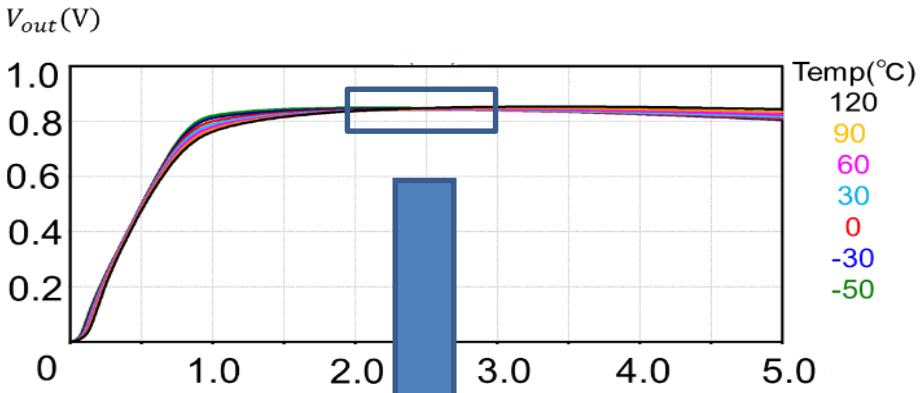
Output voltage VOUT

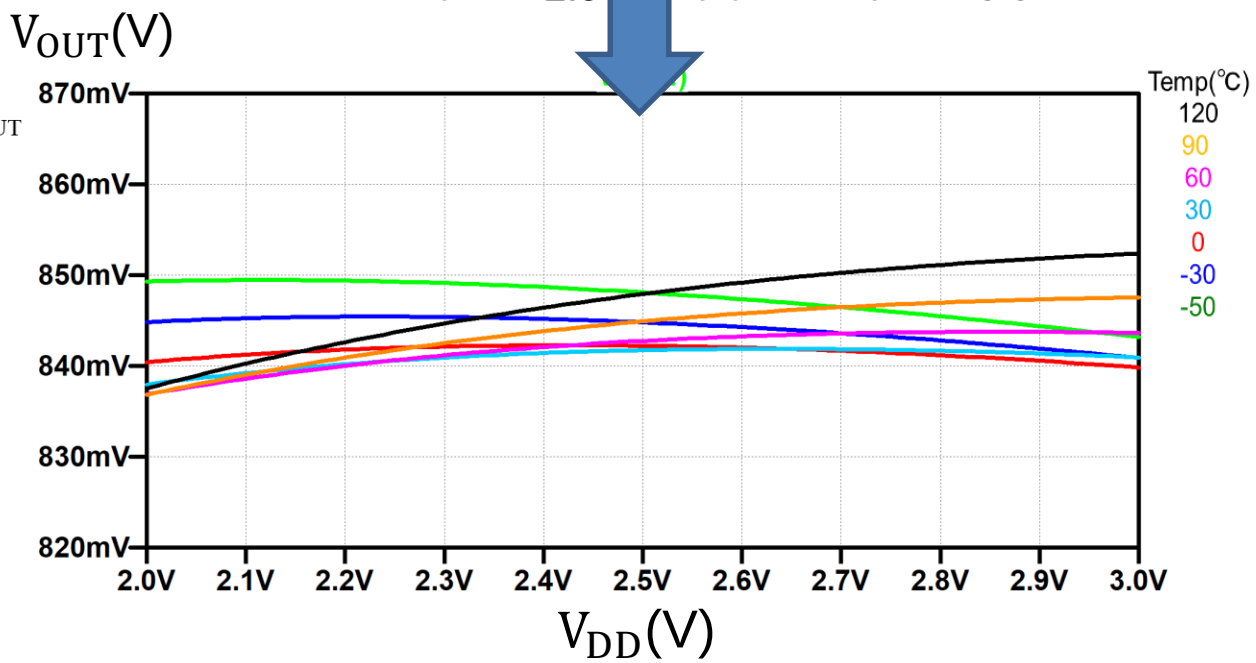
→ Constant over wide range of temperature

→ Constant over wide range of supply voltage

Whole Circuit Simulation Result (Enlarged)







Designed as

Supply voltage V_{DD} @2.5 V ⇒ Most stable

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Conclusion

Proposal of simple CMOS reference voltage source

- Voltage reference core
  Temperature insensitivity
- Bias current generator
  Supply voltage insensitivity
- Need for only standard CMOS
  TSMC 0.18um CMOS parameter
  SPICE simulation
- No need for start-up circuit
- Resistor temperature coefficient can be positive, zero or negative, if they are known a priori

Thank you very much

Reference and standard are important
to suppress manufacturing variation !

群馬大学
GUNMA UNIVERSITY

JEDAT®
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Kobayashi Laboratory