A Reference Current Source with Cascaded Nagata Current Mirrors Insensitive to Supply Voltage and Temperature

Tianrui Feng, Hiroshi Tanimoto, Takafumi Kamio,

Souma Yamamoto, Takashi Hosono, Shogo Katayama

Kakeru Ootomo, Anna Kuwana, Haruo Kobayashi

Gunma University

Kitami Institute of Technology

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- CMOS Reference Current Source with Cascaded Nagata Current Mirrors
- Temperature Insensitivity Design
- Conclusion

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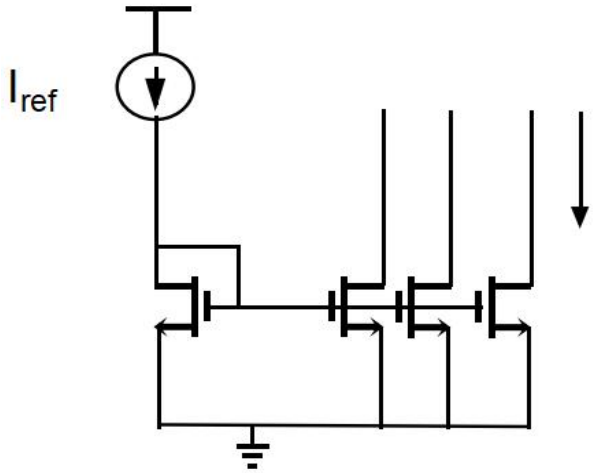
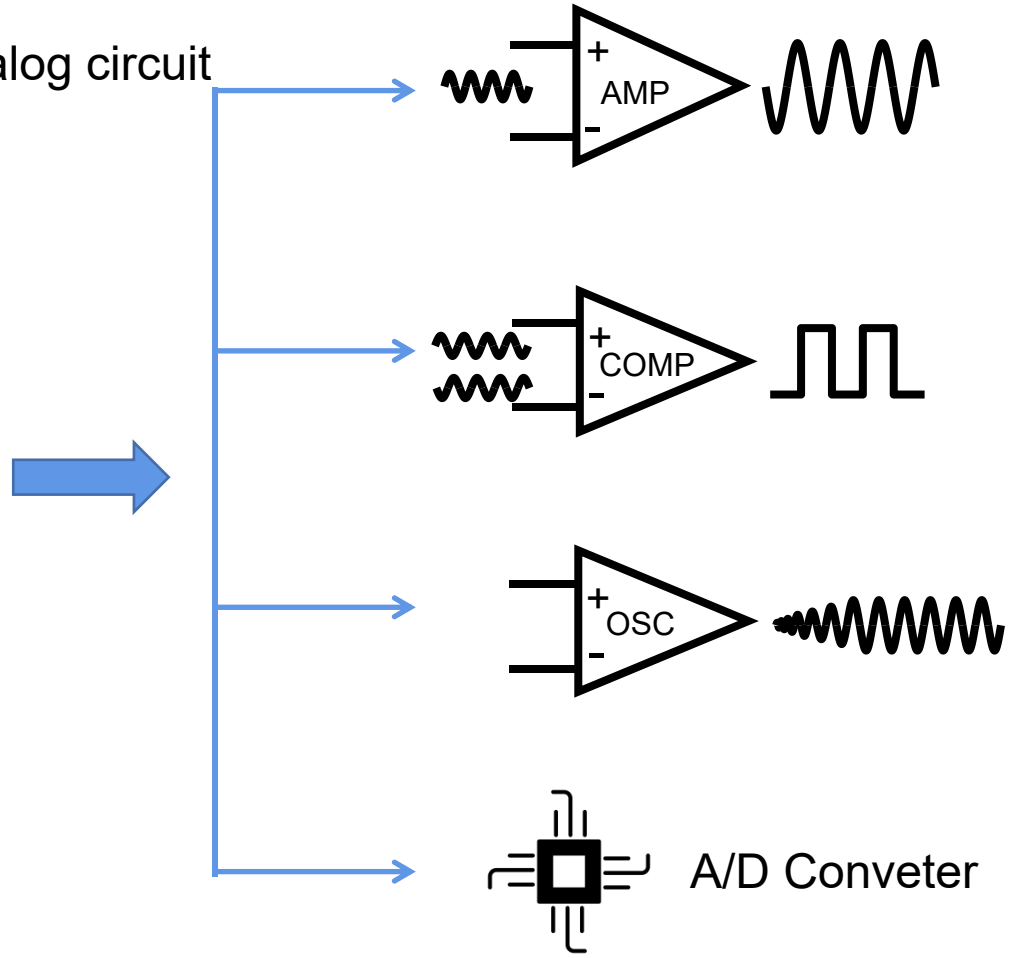
Research Background

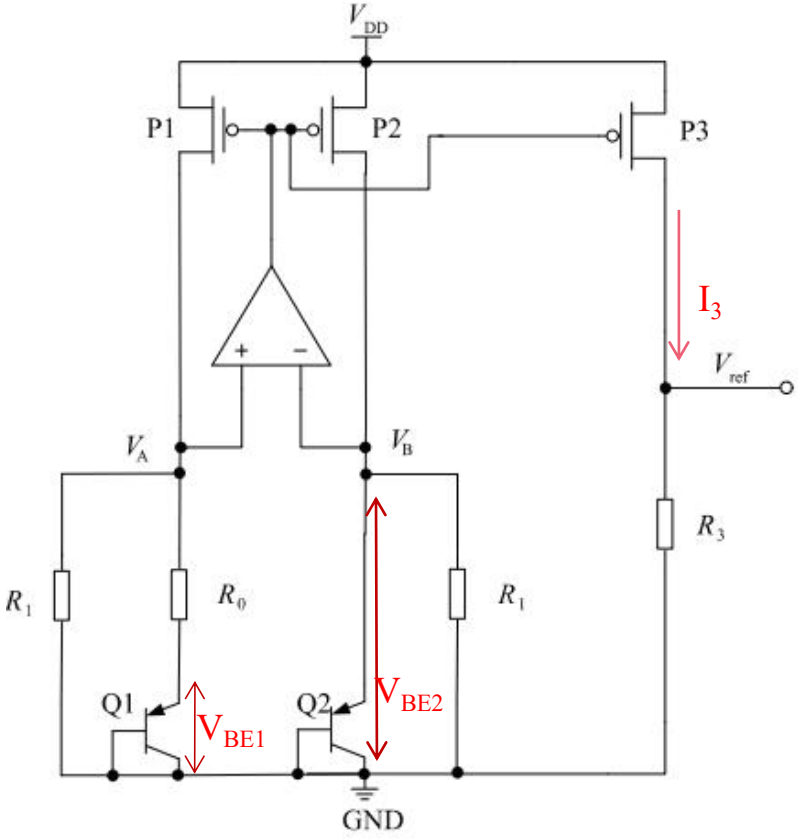
Reference current
→ Important building blocks in analog circuit

Supply stable current





Bandgap Reference Source



Ratio of emitter areas of bipolar transistors Q1 and Q2 is N:1
Aspect ratios of MOSFET P1,P2,P3 are the same

Operation amplifier makes V_A=V_B

$$\begin{aligned}\Delta V_{BE} &= V_{BE2} - V_{BE1} \\ &= V_T \ln\frac{I_0}{I_{S2}} - V_T \ln\frac{I_0}{NI_{S1}} \\ &= V_T \ln N\end{aligned}$$

$$I_3 = \frac{V_{BE2}}{R_1} + \frac{V_T \ln N}{R_0}$$

V_{BE2} negative temperature coefficient
V_T positive temperature coefficient

I_3 insensitive to temperature

Research Objective

Development of reference current source insensitive to temperature and supply voltage with simple CMOS circuit.

Bandgap reference circuit		Nagata current source
Complicated Large chip area		Simple Insensitive to supply voltage

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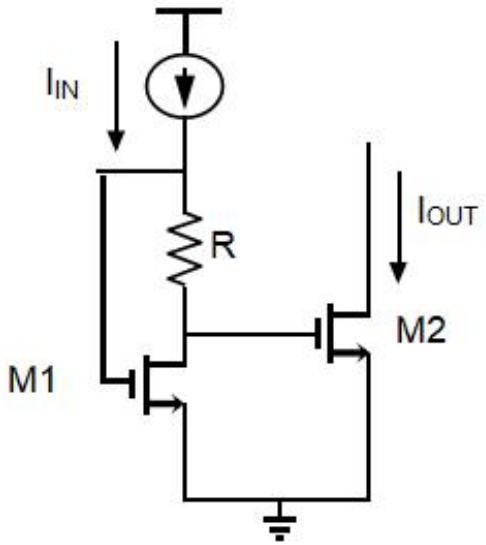
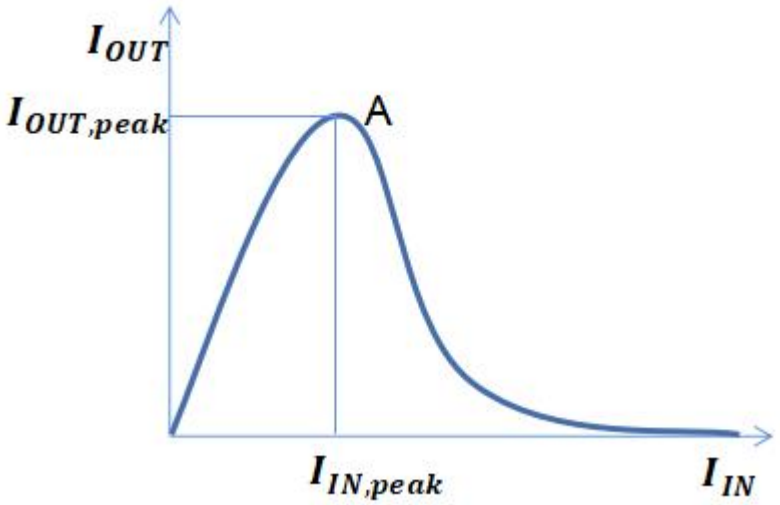
Nagata Current Mirror



NMOS Nagata current mirror



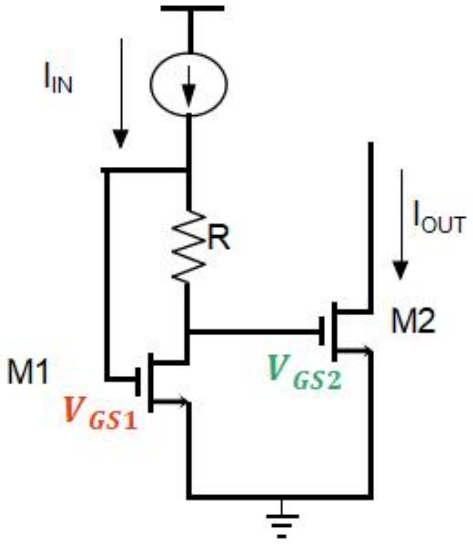
I-O current characteristics

Output current has a peak

$I_{IN} < I_{IN,peak}$, I_{OUT} monotonically increasing

$I_{IN} > I_{IN,peak}$, I_{OUT} monotonically decreasing

Analysis of Nagata Current Mirror



NMOS Nagata current mirror

Peak current value $I_{OUT,peak}$

$$V_{GS1} = V_{GS2} + I_{IN}R$$

$$①V_{GS1} = \sqrt{\frac{I_{IN}}{K_1}} + V_{th} \quad (K_1 = {}^1\!/_2\,\mu_n C_{ox}\frac{W_1}{L_1})$$

$$②V_{GS2} = \sqrt{\frac{I_{OUT}}{K_2}} + V_{th} \quad (K_2 = {}^1\!/_2\,\mu_n C_{ox}\frac{W_2}{L_2})$$

$$I_{OUT} = K_2R^2\left(\sqrt{\frac{I_{IN}}{K_1R^2}} - I_{IN}\right)^2$$

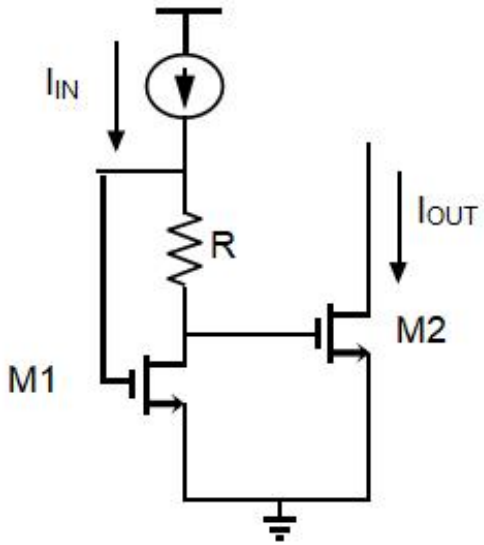
To find the maximal value, differentiate I_{OUT} with respect to I_{IN}

$$\frac{dI_{OUT}}{dI_{IN}} = 2K_2R^2\left(\sqrt{\frac{I_{IN}}{K_1R^2}} - I_{IN}\right)\left(\sqrt{\frac{1}{K_1R^2}} \times \sqrt{\frac{1}{4I_{IN}}} - 1\right)$$

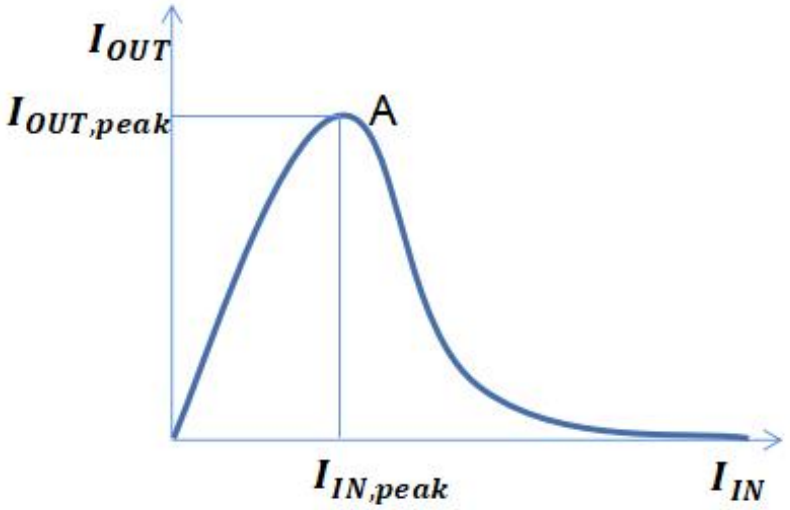
$$I_{IN,peak} = \frac{1}{4K_1R^2} \quad , \quad I_{OUT,peak} = \frac{1}{16K_1R^2} \times \frac{K_2}{K_1}$$

Output current I_{OUT} → function of R, K_1, K_2

Consideration of Cascaded Current Source



MOS Nagata current mirror



I-O current characteristics

Output current has a peak at point A

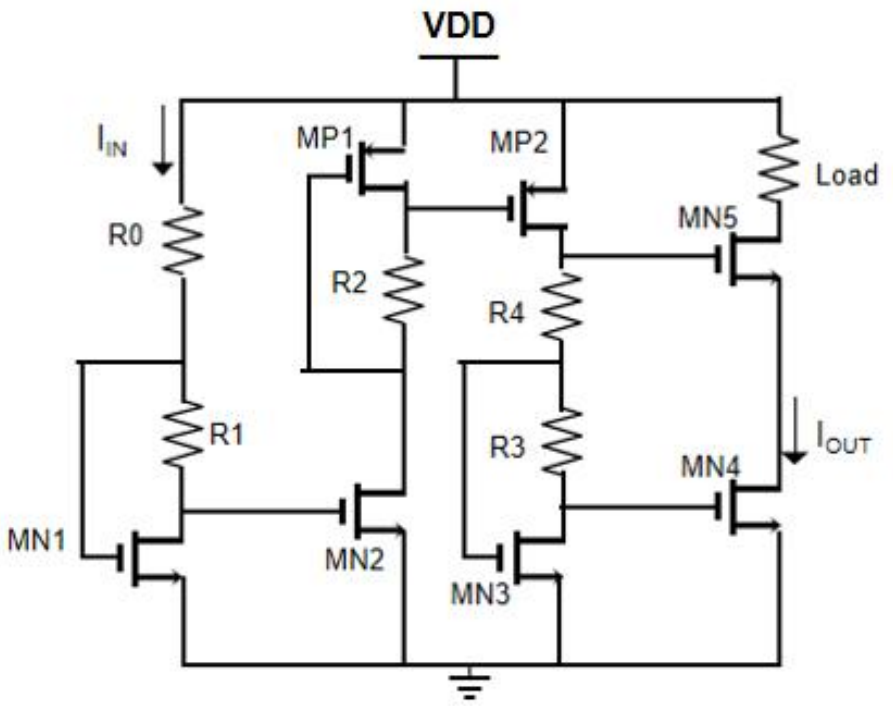
⇩

Near point A, derivative of output current is almost zero

⇩

If output current as input signal of next stage
the final output signal change more slowly.

Cascaded Reference Current Source



MN2,MP2,MN4 meets its peak at 1.8V

↓

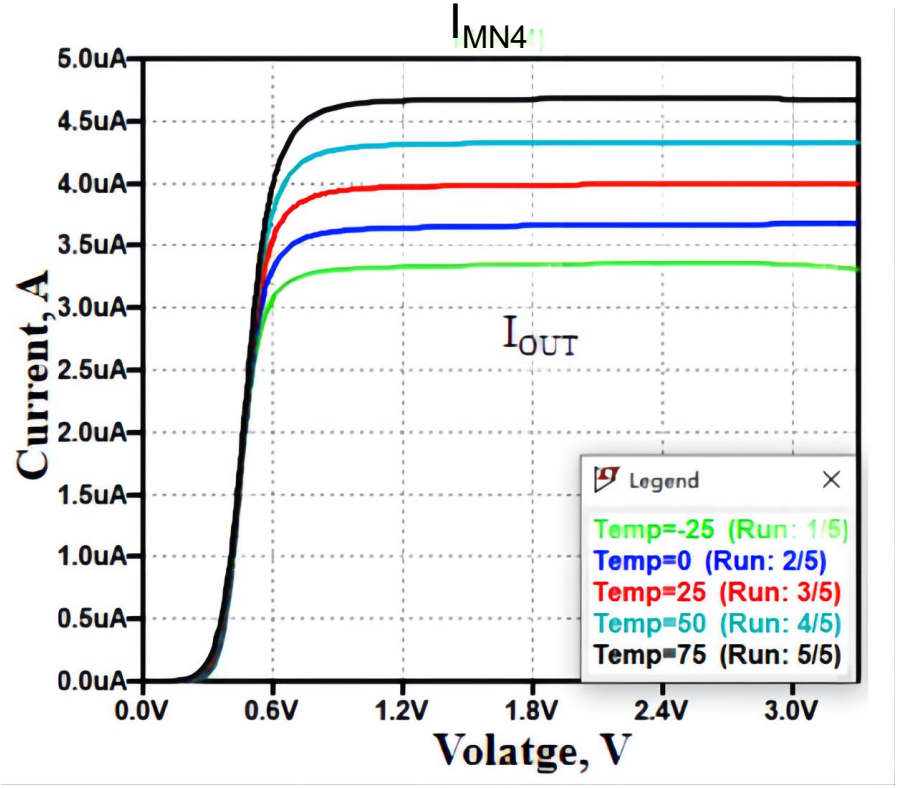
Gradient of I_{MN2} and I_{MP2} almost zero at 1.8V

↓

I_{MP2} insensitive to VDD (or I_{IN})

output current of MN4 becomes insensitive to supply voltage in wide range

Simulation Result of Supply Voltage Variation



Output current becomes insensitive to supply voltage

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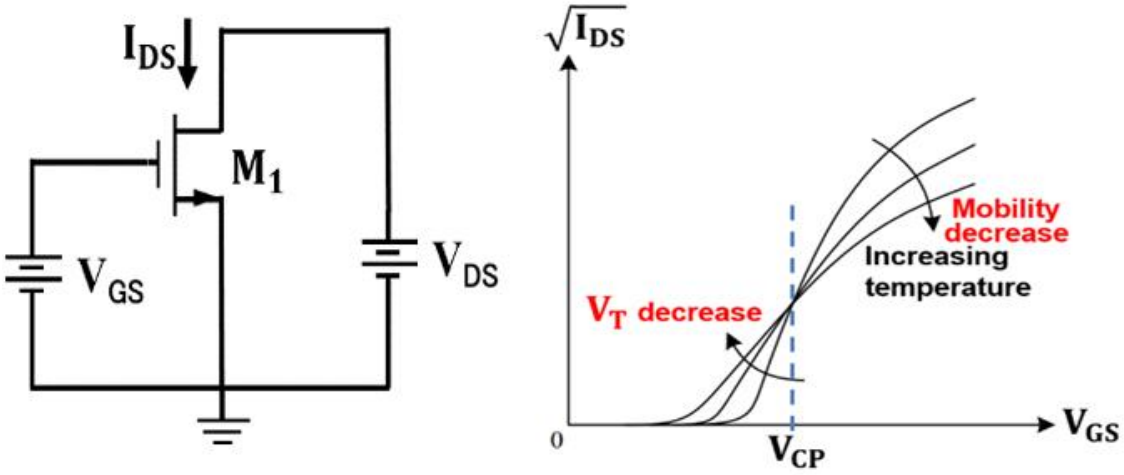
Temperature Characteristics of MOSFET Drain Current

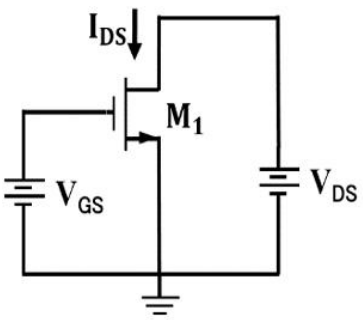


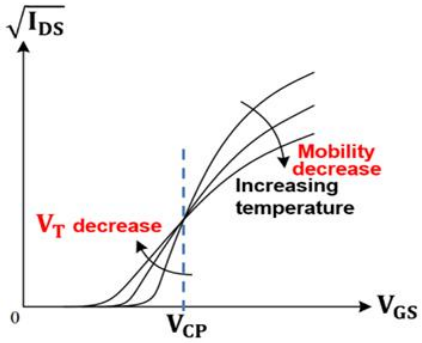
In saturation region $$I_D = \frac{W}{2L}\mu C_{ox}(V_{GS} - V_{th})^2$$

$$\frac{1}{I_D}\frac{dI_D}{dT} = \frac{1}{\mu}\frac{d\mu(T)}{dT} - \left[\frac{2}{V_{GS} - V_{th}(T)}\right]\frac{dV_{th}(T)}{dT}$$

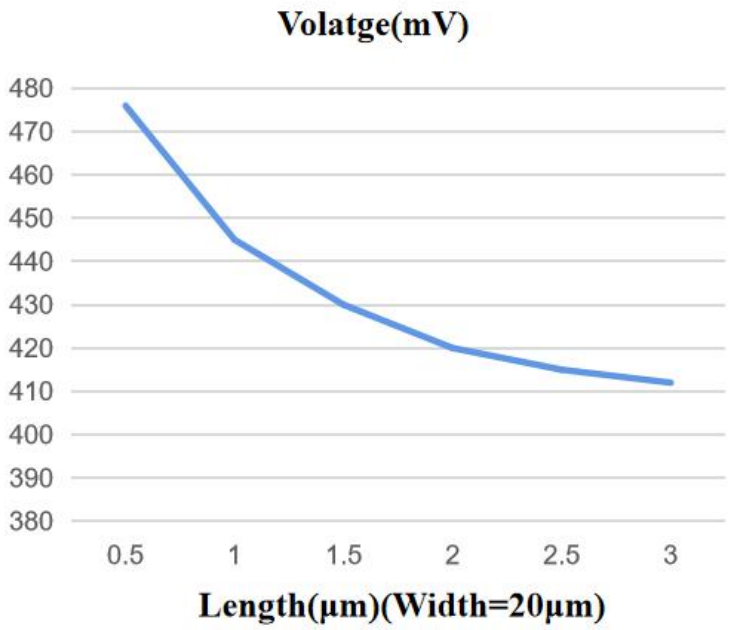
Drain current is constant at a certain biasing voltage (V_{CP})

Temperature Characteristics of MOSFET Drain Current



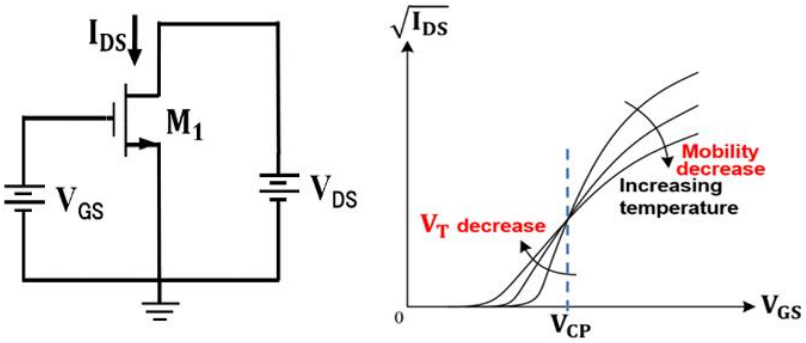


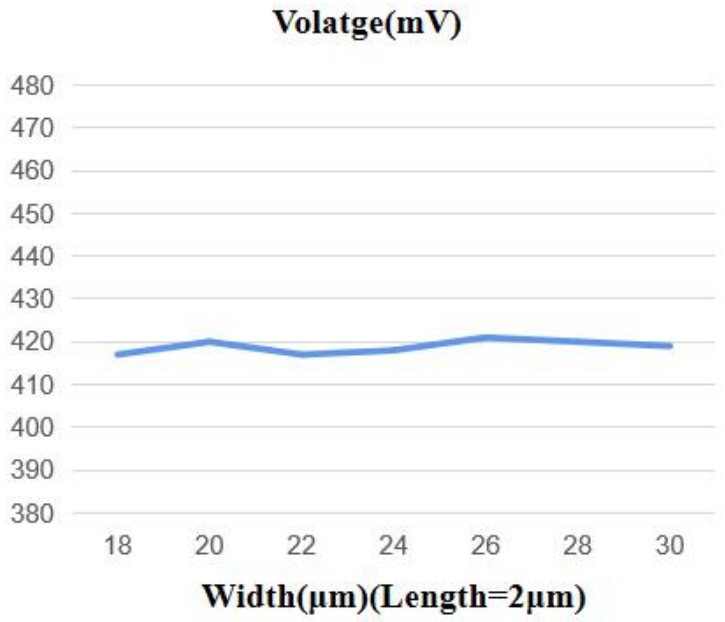
$$\frac{1}{I_D}\frac{dI_D}{dT} = \frac{1}{\mu}\frac{d\mu(T)}{dT} - \left[\frac{2}{V_{GS} - V_{th}(T)}\right]\frac{dV_{th}(T)}{dT}$$



As channel length L decreases, V_{CP} increases
due to the short channel effect that makes V_{th} decrease.

Temperature Characteristics of MOSFET Drain Current

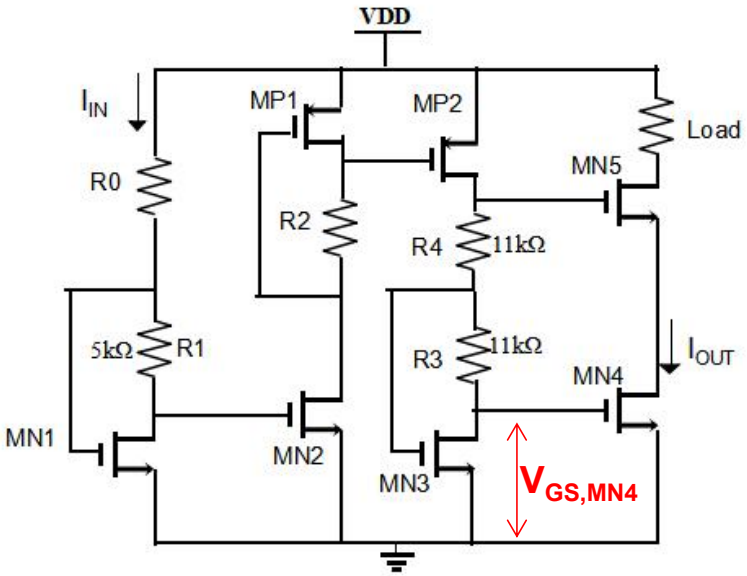




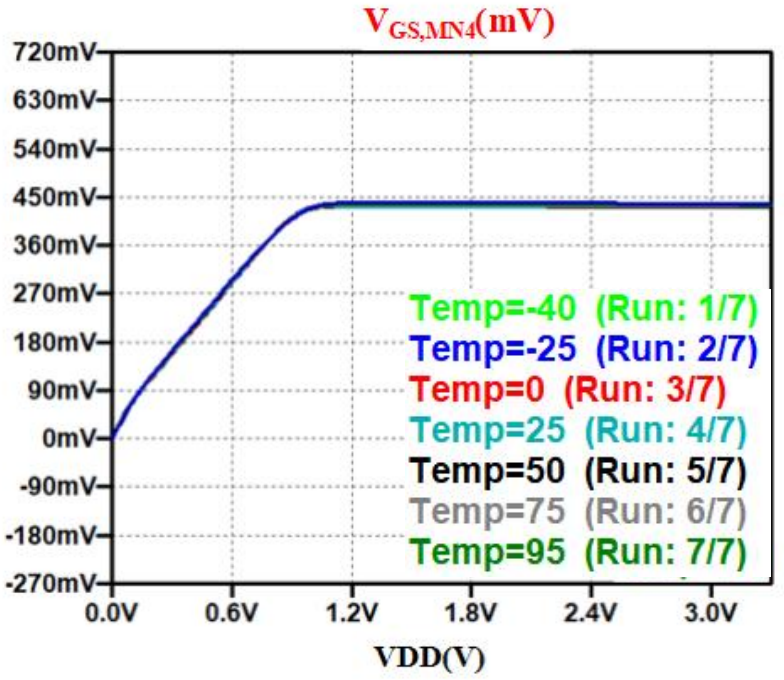
$$\frac{1}{I_D}\frac{dI_D}{dT} = \frac{1}{\mu}\frac{d\mu(T)}{dT} - \left[\frac{2}{V_{GS} - V_{th}(T)}\right]\frac{dV_{th}(T)}{dT}$$

In a large channel width,
V_{th} is almost constant even width changes,
hence the V_{CP} is almost constant.

Gate-Source Voltage of MN4



$$\frac{1}{I_D}\frac{dI_D}{dT} = \frac{1}{\mu}\frac{d\mu(T)}{dT} - \left[\frac{2}{V_{GS} - V_{th}(T)}\right]\frac{dV_{th}(T)}{dT}$$



Constant V_{GS} of MN4 by cascade structure

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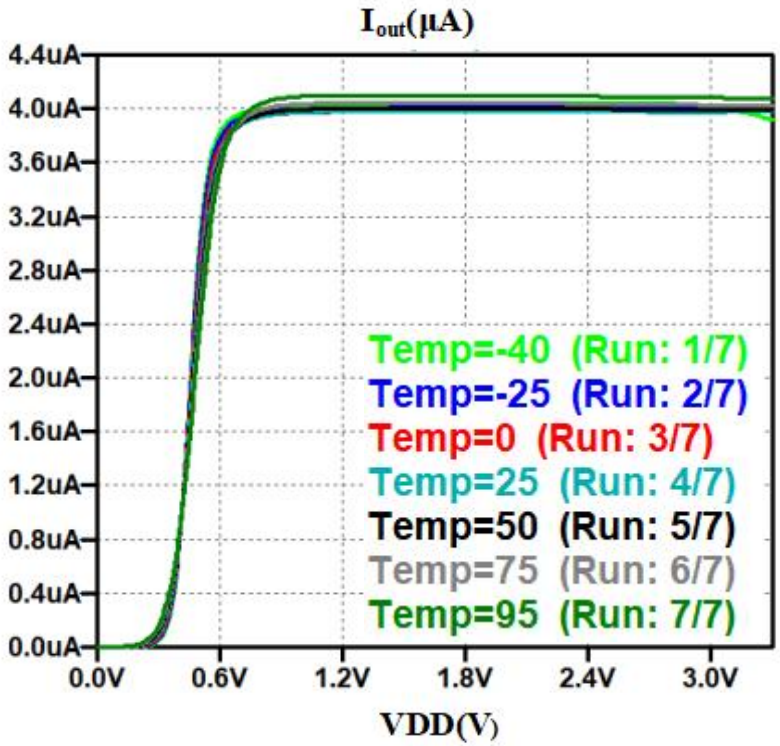
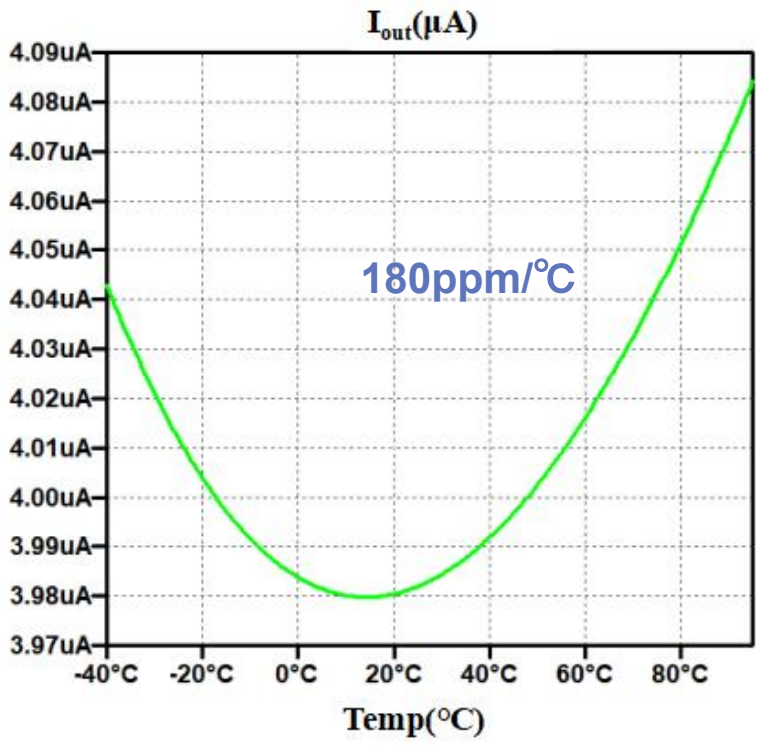
Biasing MN4 at ZTC point(V_{CP})

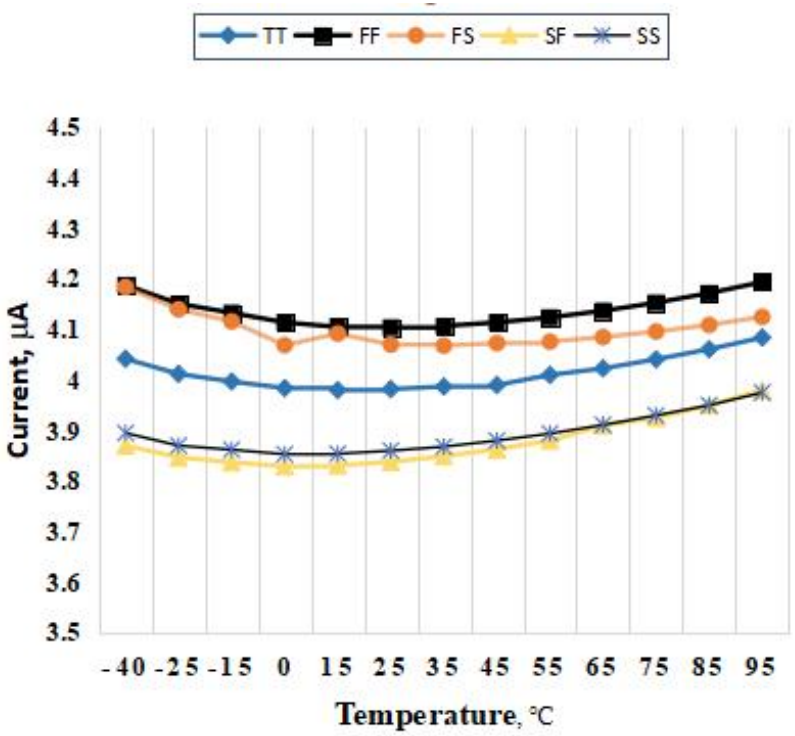
Simulation Result of Temperature Variation





Output current is almost constant with temperature variation

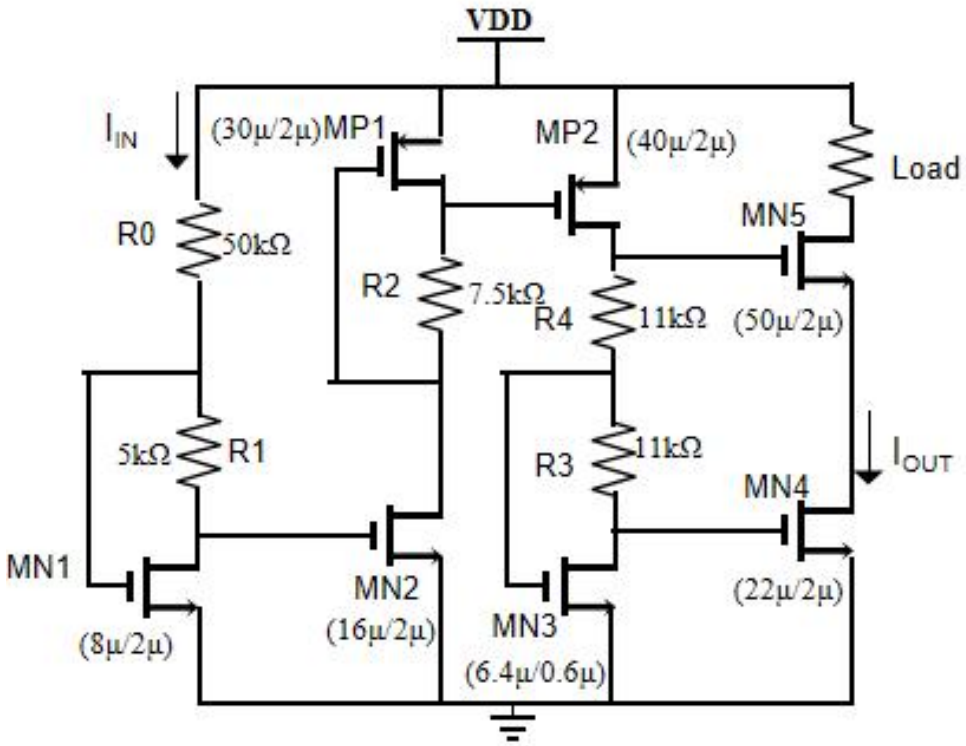
Simulation Result of Temperature Variation in 5 Corners



180ppm/℃
(TT condition)

Output current in each corner is almost constant for temperature change

Parameters of MOSFETs and resistors



(W/L): Aspect ratio of MOSFETs
W,L(μm)

Comparison with other designs

	Work	[1]	[2]	[3]	[4]	[5]
Technology	**180nm**	500nm	180nm	350nm	180nm	180nm
Supply Voltage(V)	**1.5~3.3**	1.8	2.4~3.0	1.8~3.0	1.25~1.8	1.8
Reference Current	**4μA**	7.25μA	10μA	96nA	92.3nA	120μA
Temp Co.(ppm/°C)	**180**	0.7	130	520	177	200
Temp Range (°C)	**-40~95**	-20~150	-40~80	0~80	-40~85	20~60
Power(μW)	**75(@1.8V)**	162	60 (@3.0V)	1 (@1.8V)	0.67 (@1.8V)	216

[1] Y. Lu, et. al.,"A 1.8-V 0.7 ppm/°C High Order Temperature Compensated CMOS Current Reference", Journal of Analog Integrated Circuits and Signal Processing (Jun. 2007).

[2] C. Wu, et. al., "A Low TC, Supply Independent, and Process Compensated Current Reference", IEEE Custom Integrated Circuits Conference, San Jose (Sept 2015).

[3] K. Ueno, et. al.,"A 1-μW, 600-ppm/°C Current Reference Circuit Consisting of Subthreshold CMOS Circuits," IEEE Trans. Circuits and Systems II: Express Briefs (Sept. 2010).

[4] S. S. Chouhan, et. al., " A 0.67μW, 177 ppm/◦C All MOS Current Reference Circuit in 0.18μm CMOS Technology," IEEE Trans. Circuits and Systems II: Express Briefs (Aug. 2016).

[5] T. Abe, et.al., "A Simple Current Reference with Low Sensitivity to Supply Voltage and Temperature," 24th International Conference on Mixed Design of Integrated Circuits and Systems (Aug. 2017).

Contents

Conclusion

1. Nagata Current Mirror
   a) I-O current characteristics of Nagata current mirror
   b) Peak value of output current and corresponding input current

2. Current Sources in Cascade Structure
   a) Output peak value widened by cascade structure
   b) Temperature independency realized by ZTC biasing technique
   c) Output reference current insensitive to supply voltage and temperature
   d) Working well without startup circuit

Thank you for your listening

Widely used Nagata current mirror wonderful

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