Low Switching Loss Dual RESURF 40 V N-LDMOS with Grounded Field Plate for DC-DC Converters

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OUTLINE

- Research Objective and Background
- Proposed LDMOS Structure and Operation
- Optimization Simulation Results
- Discussion
- Conclusion

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Research Objective

Development of LDMOS structure
for DC-DC converters handling 40V
in automotive applications

LDMOS: Lateral Double Diffused MOS

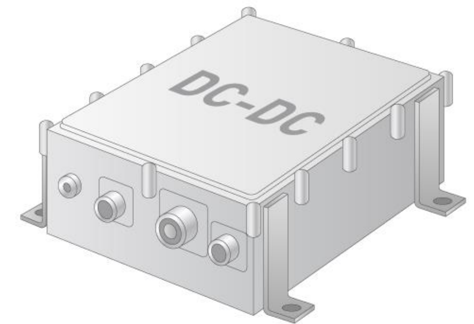
Research Background

DC-DC Converter for Automotive Application

- High efficiency
- High frequency
- High reliability

Requirements for its Switching Device

- Low specific on-resistance
- Low switching loss
- High hot carrier endurance
- Wide SOA



SOA: Safe Operating Area

Our Approach

LDMOS for 40V switching device

- Mature CMOS process usage
- One-chip integration with other circuits

Based on our Previous Proposed LDMOS

- Dual RESURF structure
- Field plate connected to gate

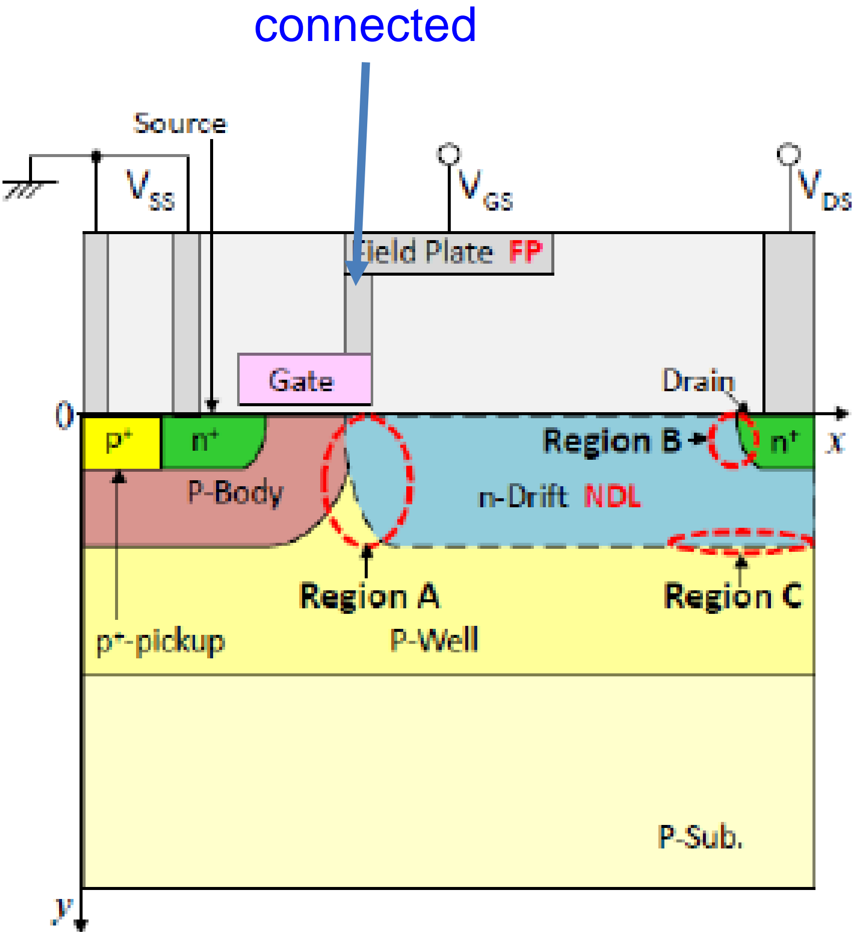
New Proposal

- Dual RESURF structure
- Field plate connected to ground
  - → Miller capacitance reduction

Investigation of Its optimal size and location

TCAD Simulation Verification

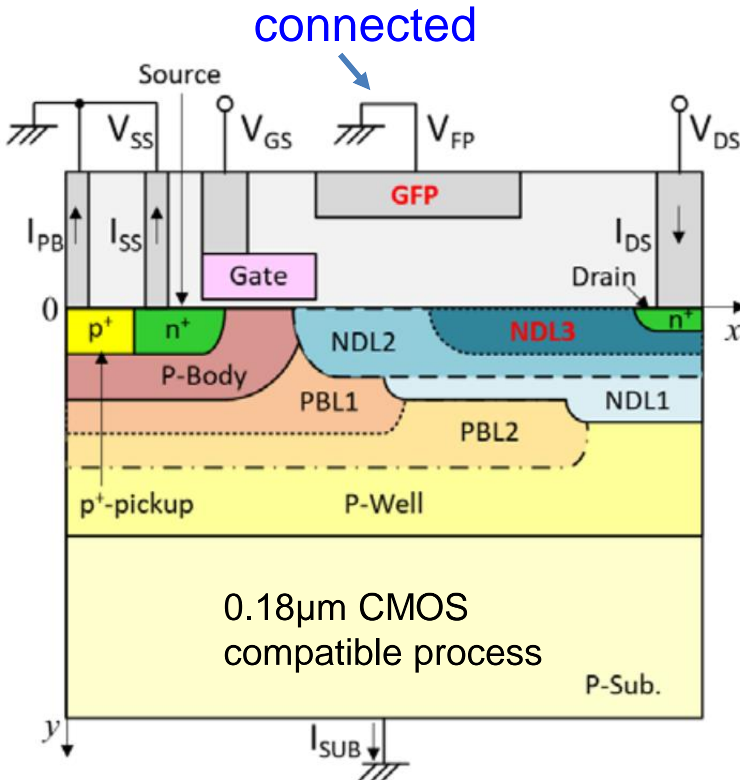
Conventional LDMOS Transistor Structure



Points to be improved

- Low hot carrier endurance
  by drain avalanche hot carriers
  high electric field in Region A
- Drain current expansion (CE)
  → narrow SOA
  by high electric field in Region B
  due to Kirk effect
- High specific on-resistance
  Low impurity concentration in n-drift region
- Premature breakdown
  by high electric field in Region C
  under the drain

Proposed LDMOS Transistor Structure



■P-buried Layers (Dual RESURF Structure)

- PBL1, 2

■N-drift Layers

- NDL1, 2
- NDL3:
  Specific on-resistance reduction
  CE (current expansion) suppression

■Grounded Field Plate (GFP)

- Complements RESURF effect in drift region
- Miller capacitance reduction
  → Low switching loss

Investigation of its optimal location, size

Research Overview

Our previous proposal:

0.18 μm CMOS compatible dual REduced SURface Field (RESURF)
40 V N-LDMOS transistor with grounded field plate

Our research here:

- Grounded field plate optimization
  by changing location, length of grounded field plate
- Its process feasibility investigation
  from mass production viewpoint
- Verification with TCAD simulation

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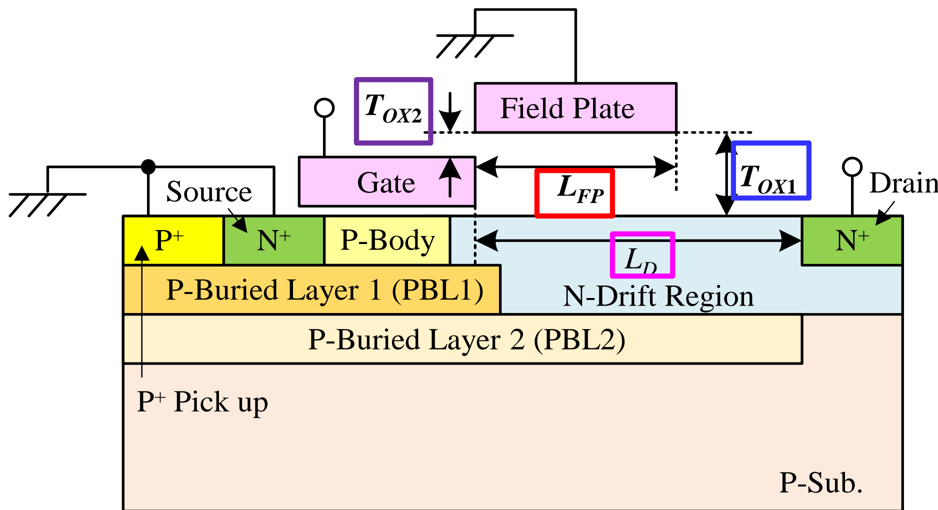
Proposed LDMOS Structure and Feature



Length of drift region L_D : 2650 nm

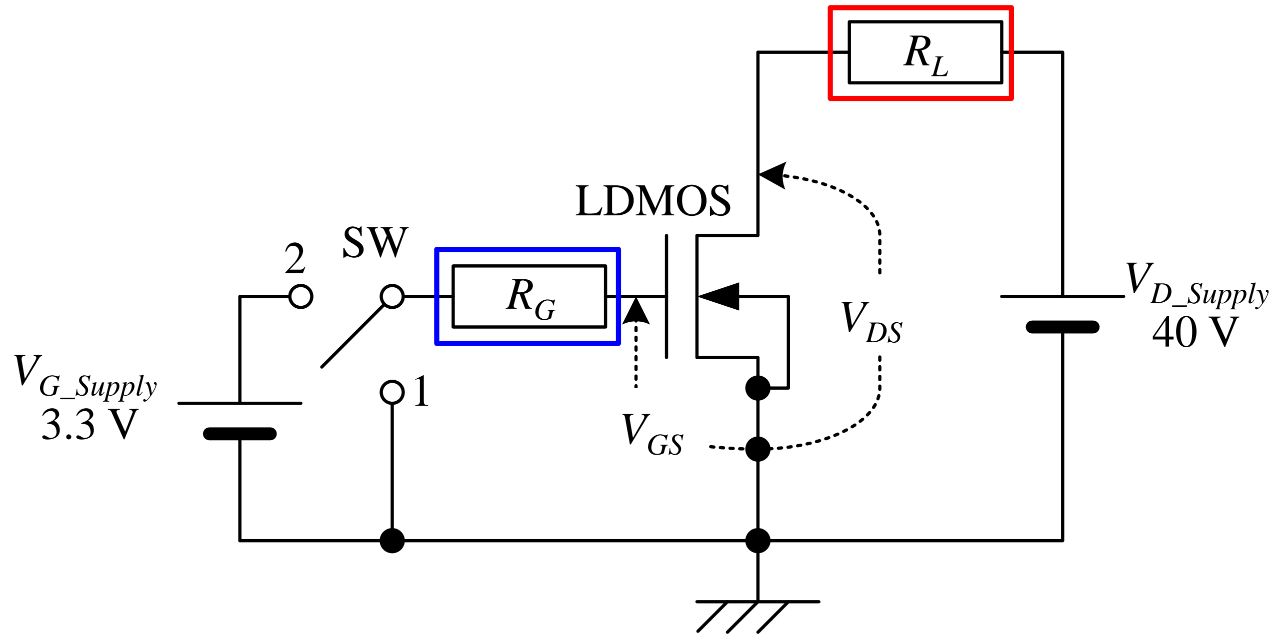
Field plate L_{FP}(standard $L_{FP\text{-}std}$) : 1625 nm

Thickness of oxide interlayer between field plate and drift region T_{OX1}(standard $T_{OX1\text{-}std}$): 308 nm

Oxide interlayer between field plate and the gate T_{OX2}(standard $T_{OX2\text{-}std}$): 100 nm

Breakdown voltage between drain and source BV_{DS} : 61 V

Simulation Circuit as Switching Device



Specific on-resistance: 40.8 mΩmm^2

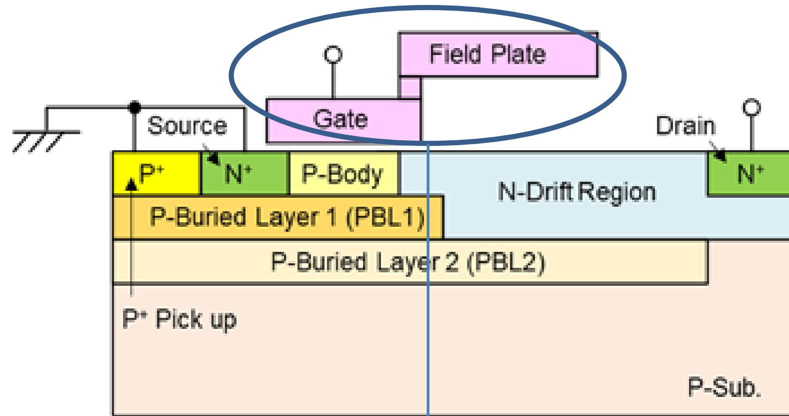
Load resistance R_L: 5.33Ωmm^2

Gate resistance R_G : 1.07Ωmm^2

Extrapolated threshold voltage: 1.05V

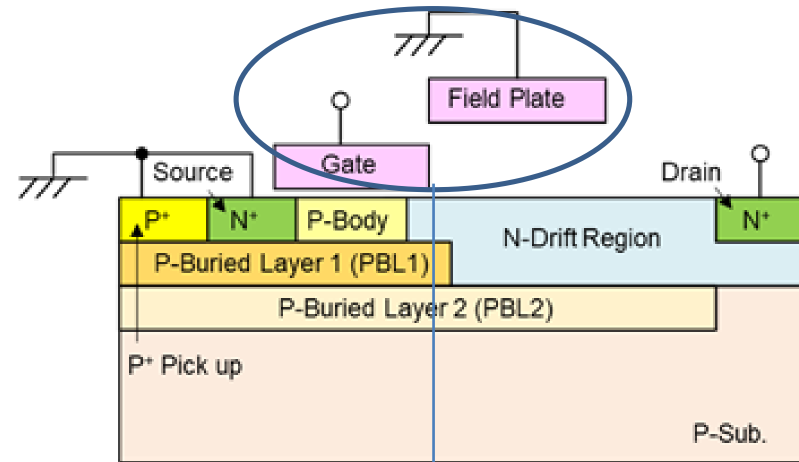
Device Structures and Features

Conventional device



(a) Conventional device

Proposed device [1, 2]



(b) Proposed device

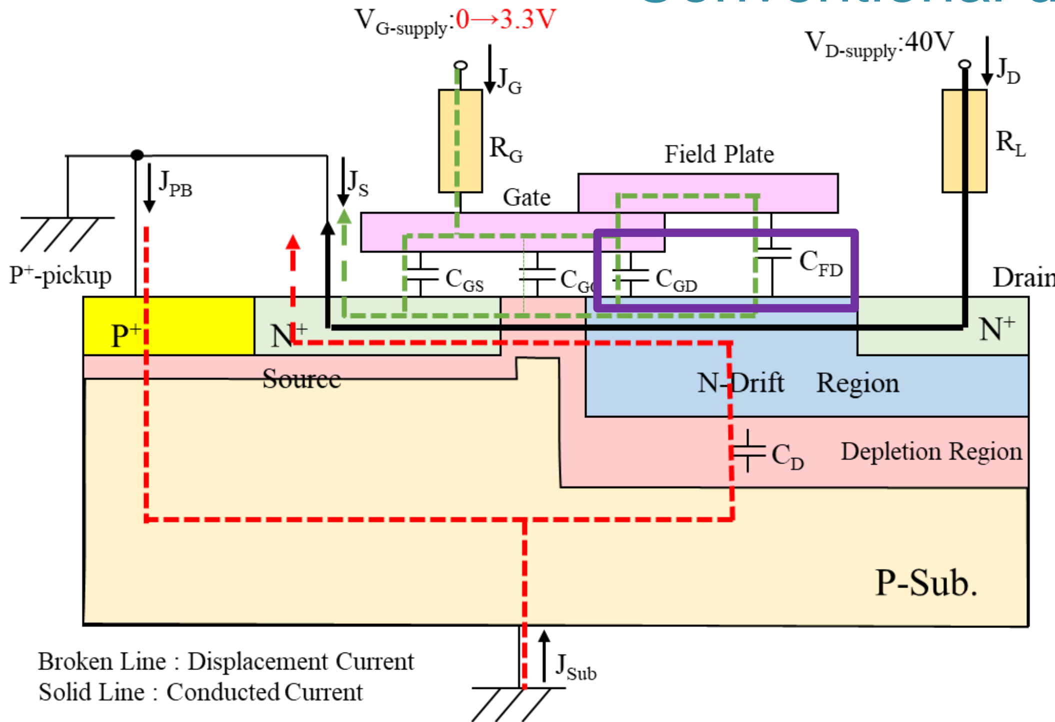
Field plate ➡ connected to gate

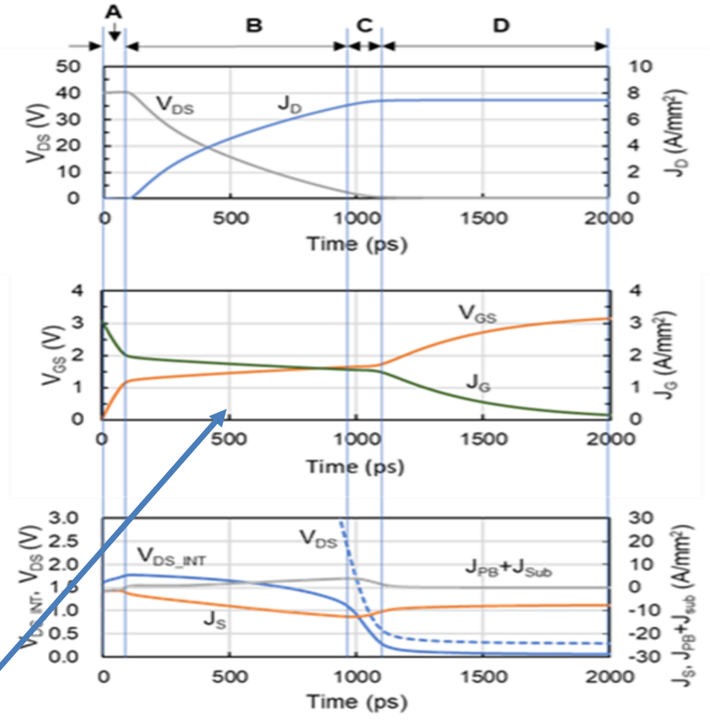
Field plate ➡ connected to ground

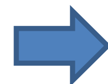
[1] J. Matsuda, et. al., "A Low Switching Loss 40 V Dual RESURF LDMOS Transistor with Low Specific On-Resistance", in *Proc. ICMEMIS*, Kiryu, 2017.
[2] J. Matsuda, et. al., "Low Switching Loss and Scalable 20-40 V LDMOS Transistors with Low Specific On-Resistance", in *Proc. ICTSS*, Kiryu, 2018.

Turn-On Simulation Results (Region B)

Conventional device







Region B

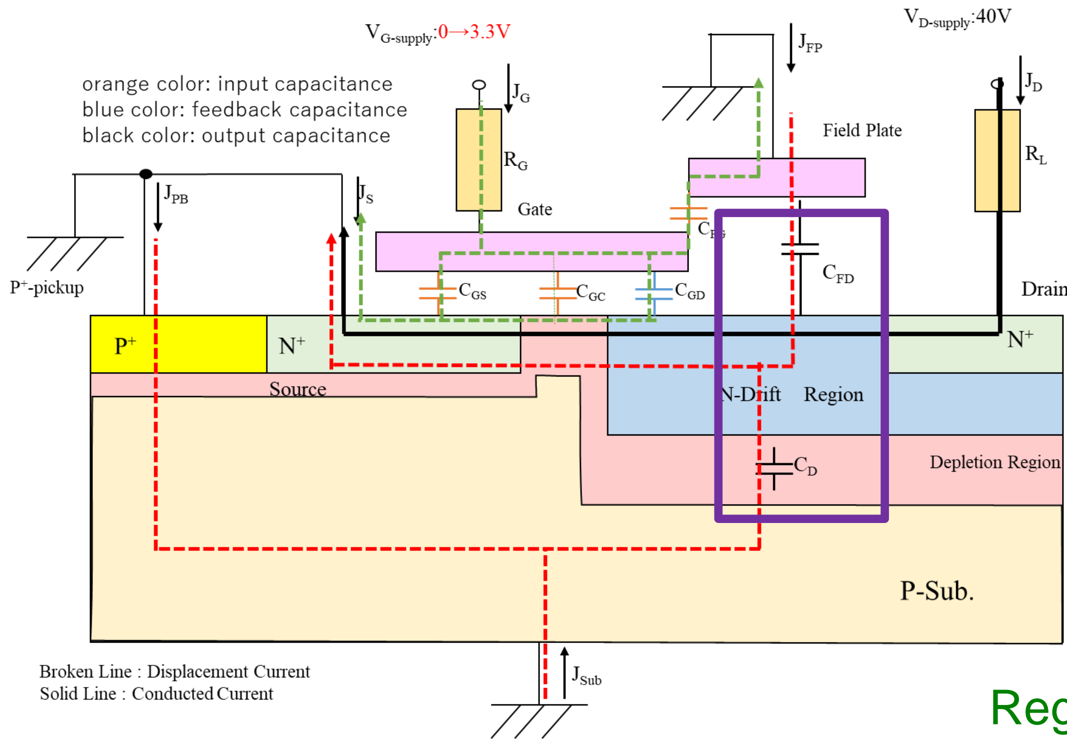
Charging feedback capacitance ($C_{GD}+C_{FD}$)

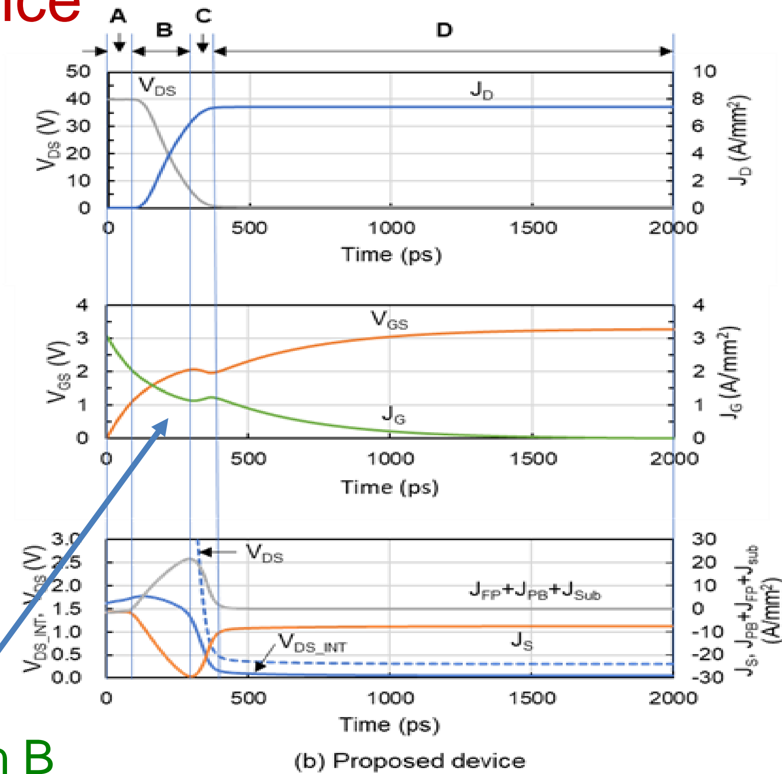
In gate plateau state
(**Long, intense Miller effect**) ☹

Discharging output capacitance(C_D)

Turn-On Simulation Results (Region B)

Proposed device





Region B

Discharging output capacitance(C_D+C_{FD})

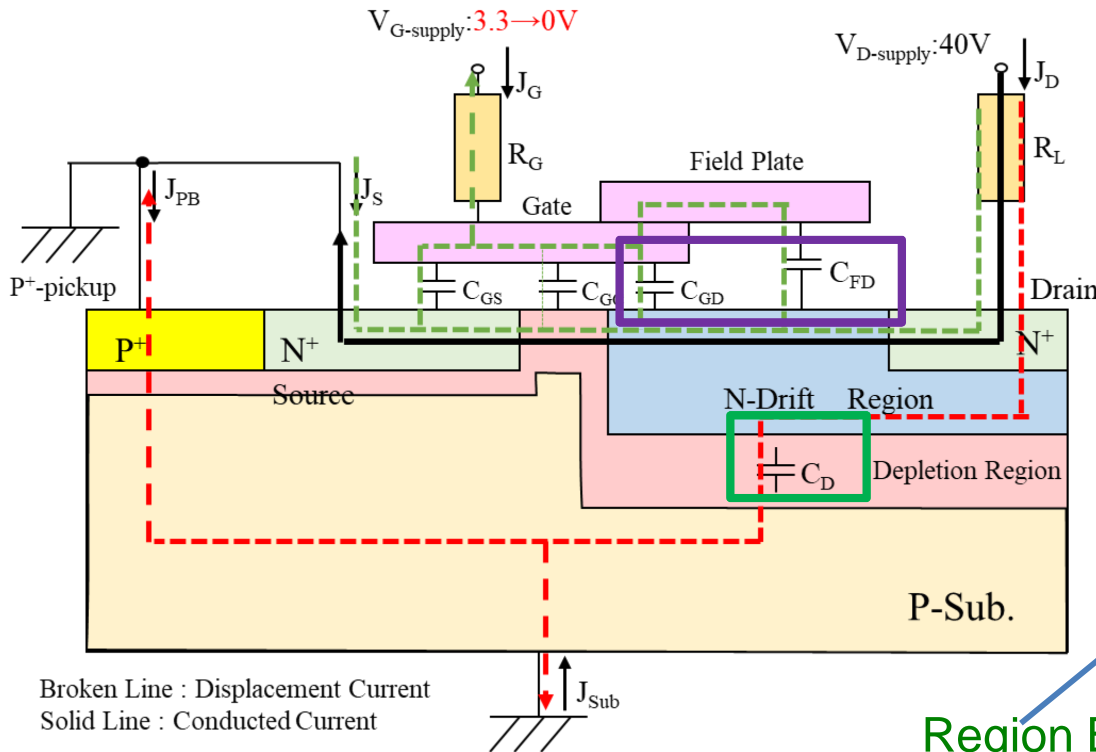
Increase in displacement current ($J_{FP}+J_{PB}+J_{Sub}$)

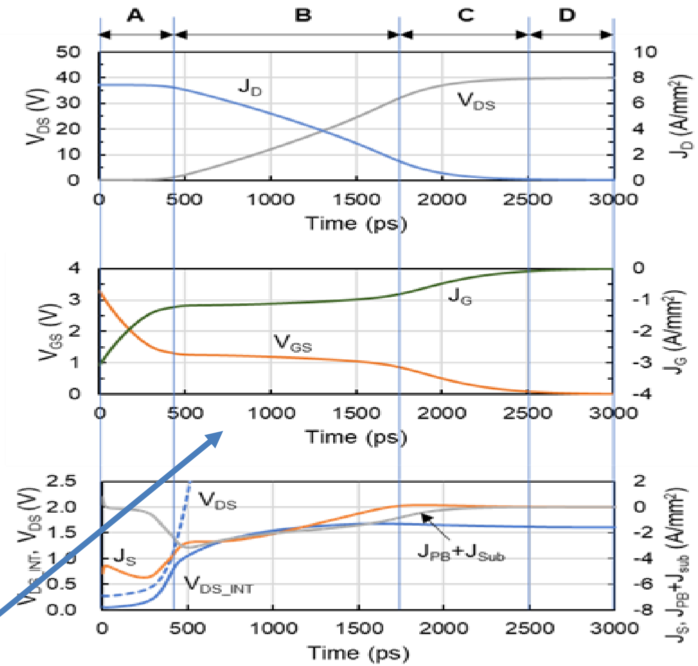
Gradual decrease in V_{DS_INT} ☺

(**Weak Miller effect**)

Turn-Off Simulation Results (Region B)

Conventional device





(a) Conventional device

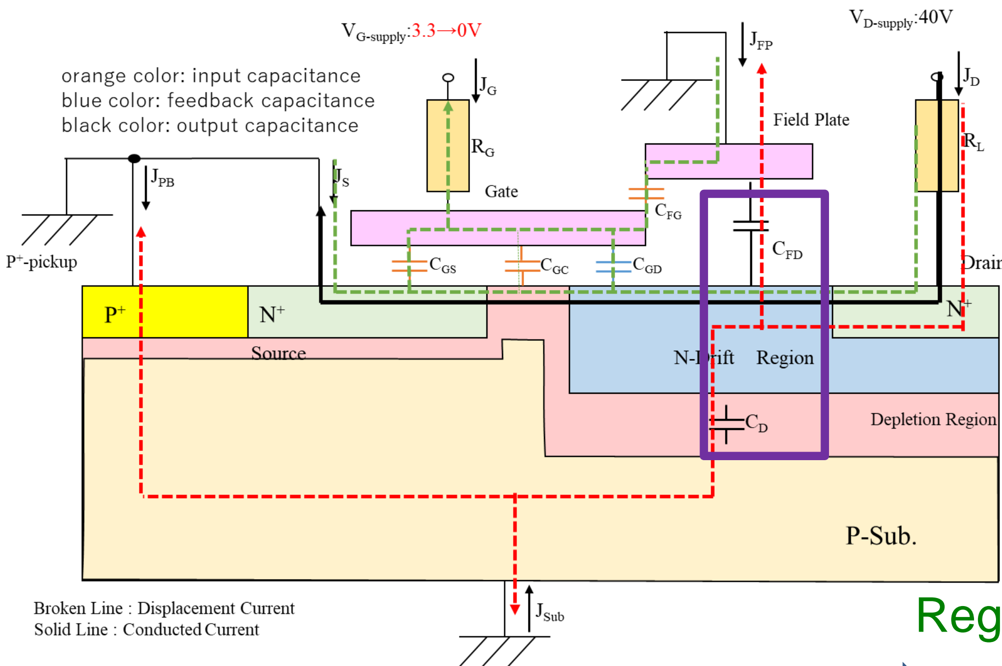
Region B

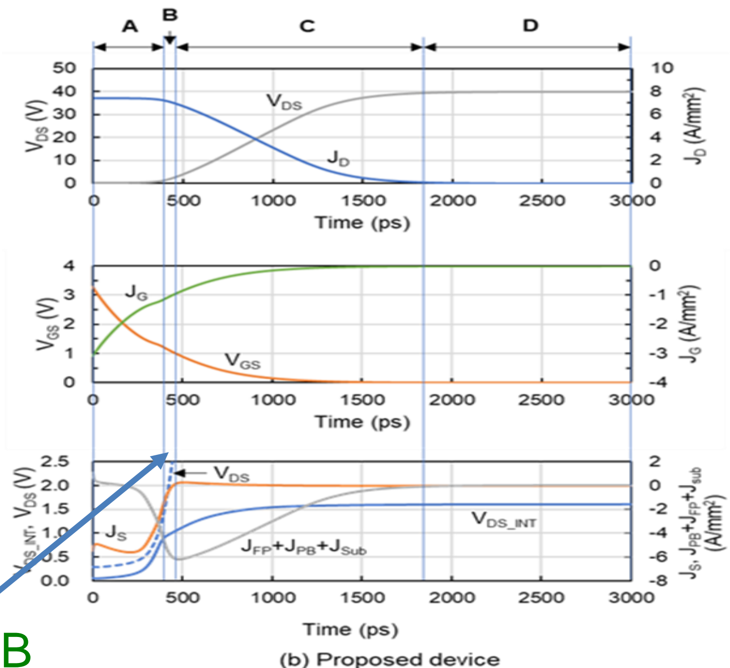
Charging output capacitance(C_D)
feedback capacitance(C_{GD}+C_{FD})

In gate plateau state
(**Long, intense Miller effect**) ☹

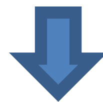
Turn-Off Simulation Results (Region B)

Proposed device

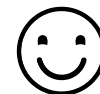




Region B

$V_{GS} \gtrsim V_T$  at beginning of turn-off

Slight increase in V_{DS_INT} Slight decrease in V_{GS}

Short, weak Miller effect (no gate plateau) 

Charging output capacitance (C_D+C_{FD})

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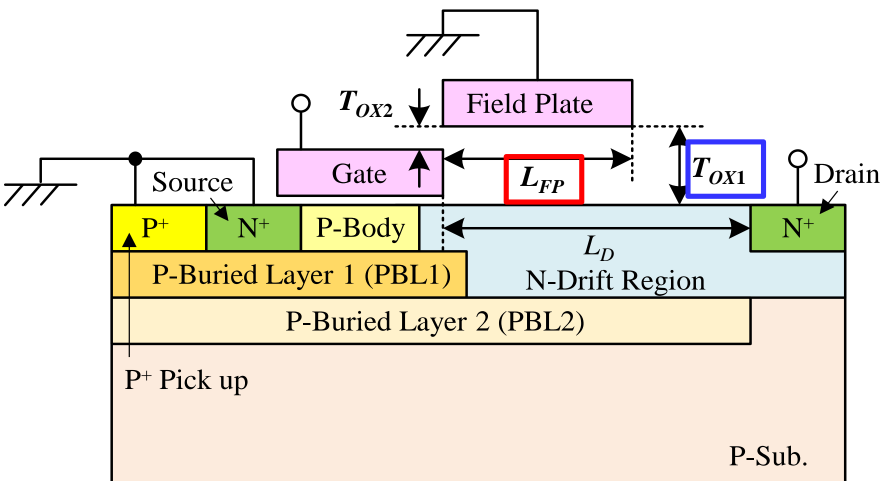
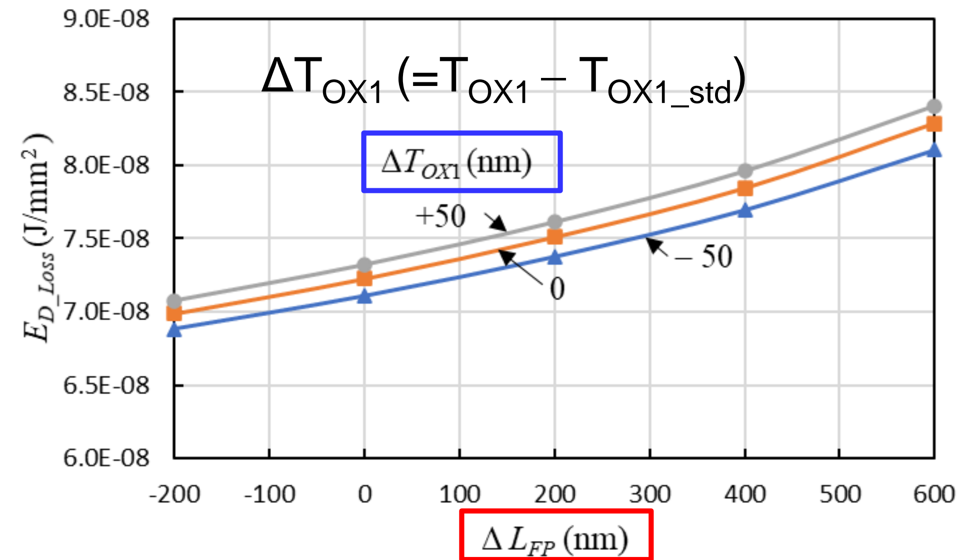
L_{FP} for Drain Loss E_{D_Loss}



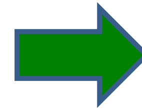


ΔL_{FP} (=$L_{FP} - L_{FP_std}$)

During turn-on/off :

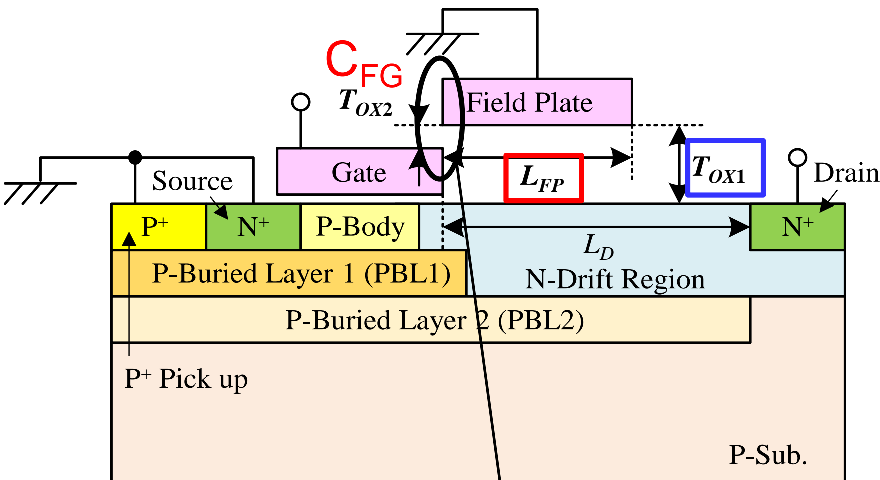
ΔL_{FP} increase or ΔT_{OX1} decrease

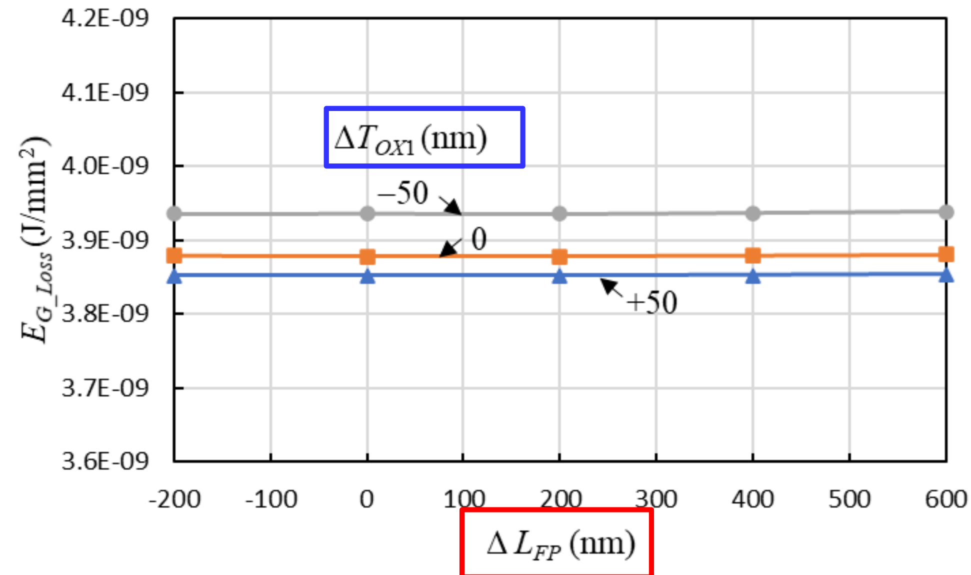
Displacement current increase



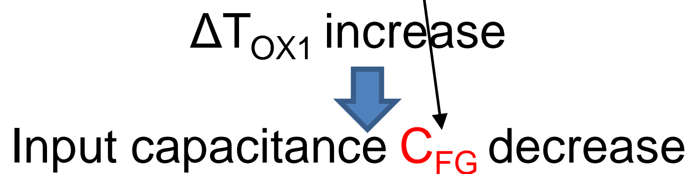
E_{D_Loss} increase

L_{FP} for Gate Loss E_{G_Loss}





ΔT_{OX1} increase

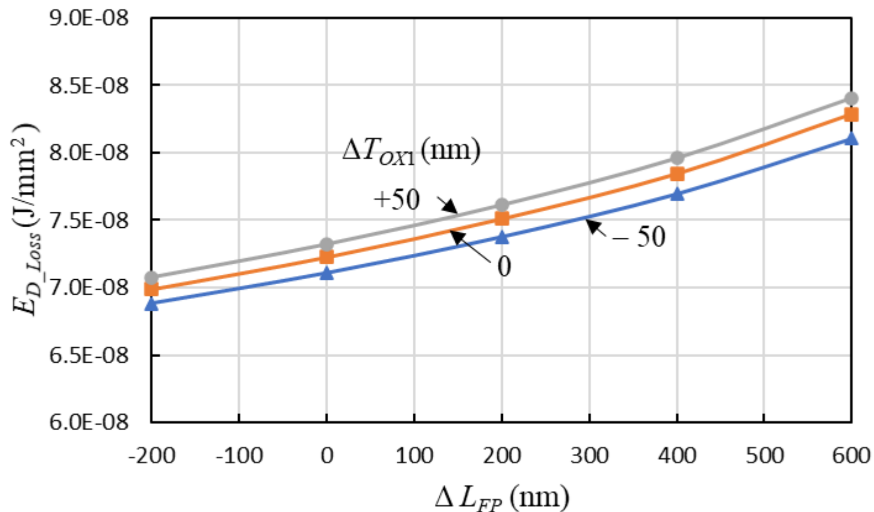


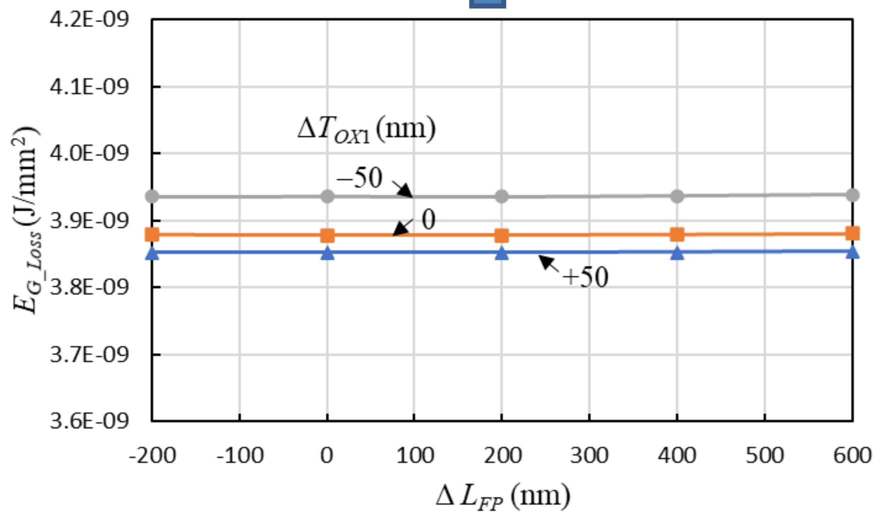
Input capacitance C_{FG} decrease

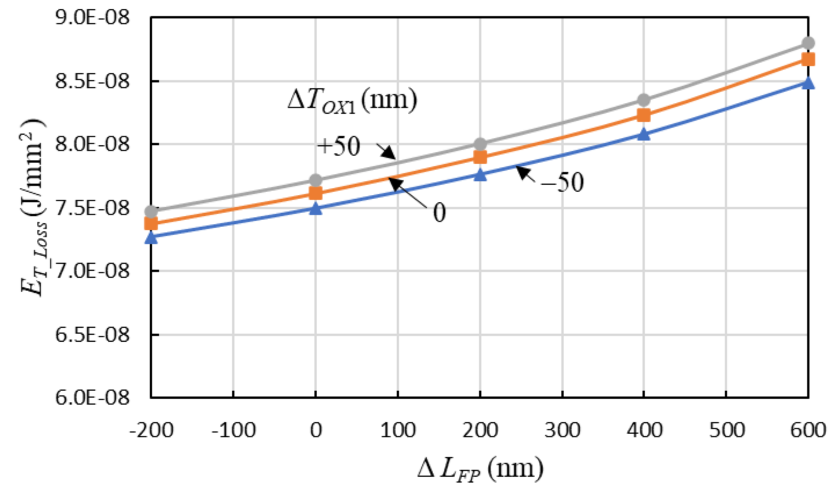
E_{G_Loss} :

- Independent of ΔL_{FP}
- Increase for ΔT_{OX1} decrease

L_{FP} for Switching Loss

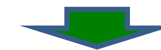






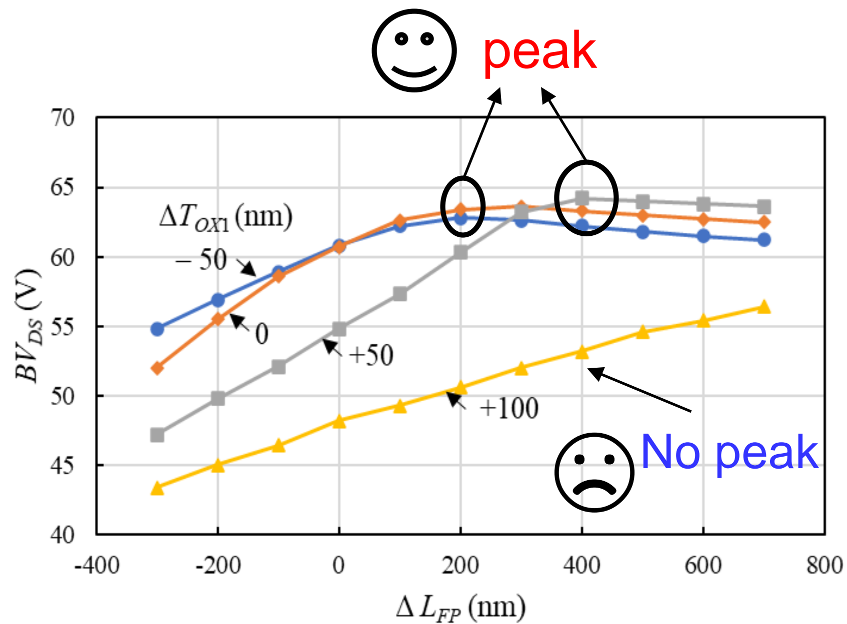
E_{G_Loss} is 1/20 lower than E_{D_Loss}

$$E_{T_Loss} = E_{D_Loss} + E_{G_Loss} \approx E_{D_Loss}$$



Increase for ΔL_{FP} → Increase E_{T_Loss}

L_{FP} for BV_{DS}



ΔT_{OX1} : -50 nm~+50 nm
Peak in BV_{DS}-ΔL_{FP}

ΔT_{OX1} : +100nm
No peak in BV_{DS}-ΔL_{FP}

For $BV_{DS} \geqq 60V$ (High reliability):

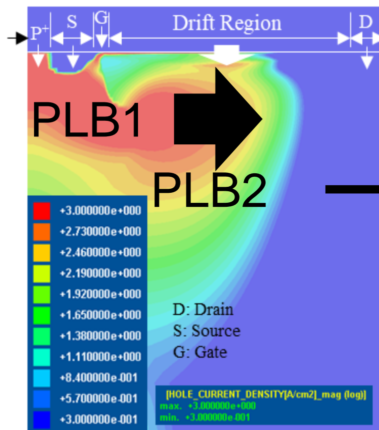
ΔT_{OX1}=100nm, $\Delta L_{FP} \geqq 200nm$

or

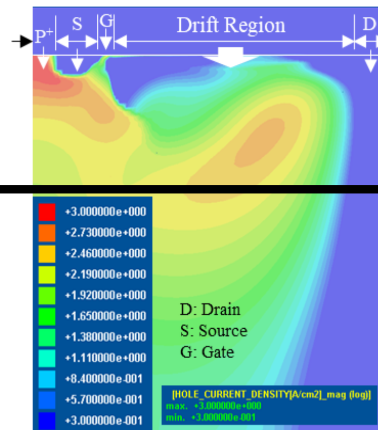
ΔT_{OX1}=50nm, $\Delta L_{FP} \geqq 200nm$

L_{FP} for BV_{DS}

Breakdown location



(a) $\Delta L_{FP} = -300$ nm

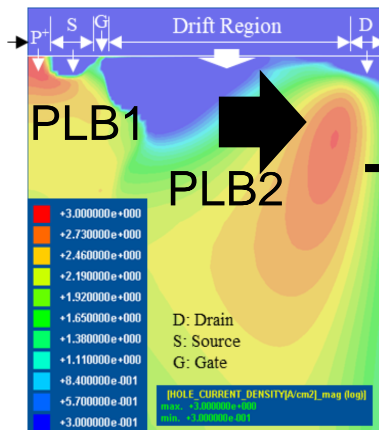


(b) $\Delta L_{FP} = 0$ nm

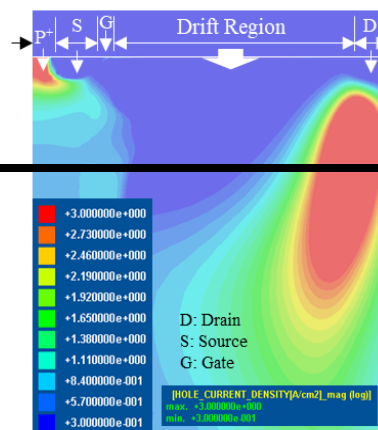
ΔL_{FP} =-300nm

- Insufficient RESURF
- BV near PBL1 end
- Current flow in drift region

Device destroyed
due to filamentation



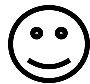
(c) $\Delta L_{FP} = +300$ nm



(d) $\Delta L_{FP} = +600$ nm

ΔL_{FP} =+300nm

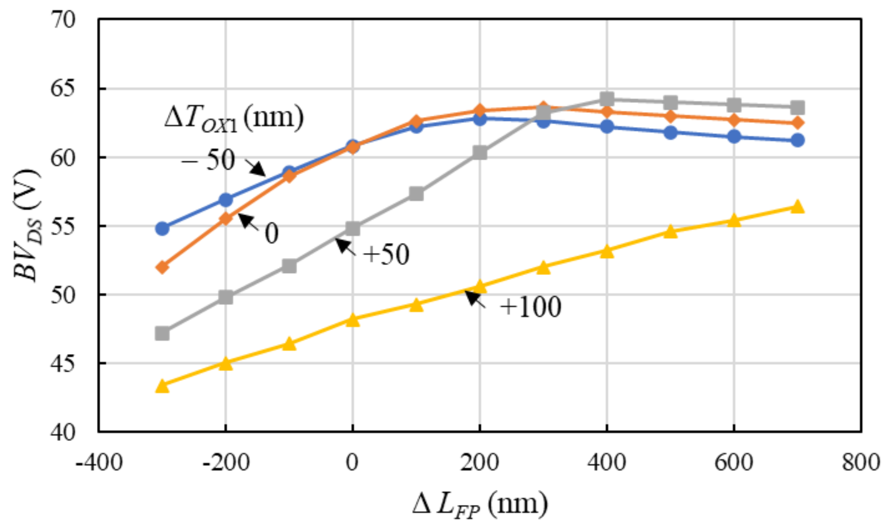
- Sufficient RESURF
- BV near PBL2 end
- Suppression of
  Current flow through drift region

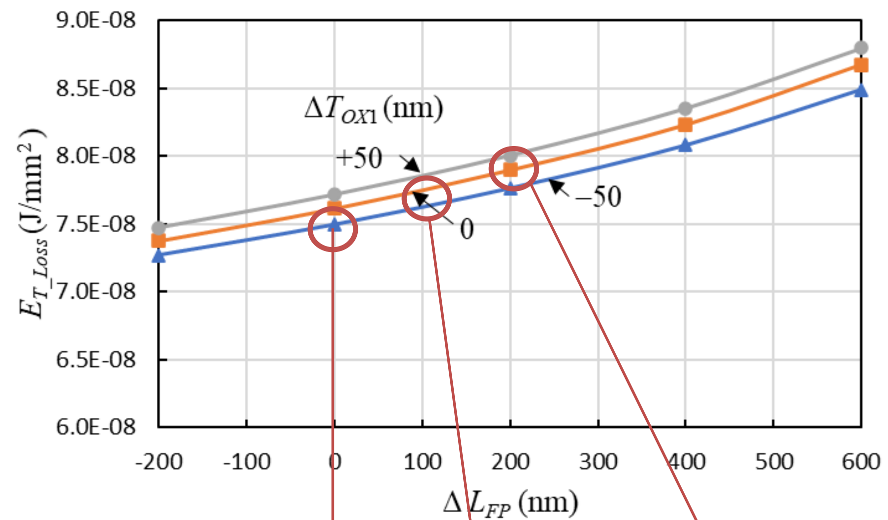


ESD resistance improvement

Drift region → breakdown

L_{FP} , T_{OX1} for Switching Loss





For BV_{DS} > 60 V	
ΔL_{FP} (nm)	ΔT_{OX1} (nm)
$0 \leq \Delta L_{FP} \leq 700$	$-50 \leq \Delta T_{OX1} \leq 0$
$200 \leq \Delta L_{FP} \leq 700$	$\Delta T_{OX1} = +50$

7.49×10^{-8} J/mm^2

7.90×10^{-8} J/mm^2

7.69×10^{-8} J/mm^2

E_{T_Loss} reduction by 53%
of LDMOS with
Field-Plate connected to gate
(ΔL_{FP}=0 nm, ΔT_{OX1}=0 nm)

Low switching loss

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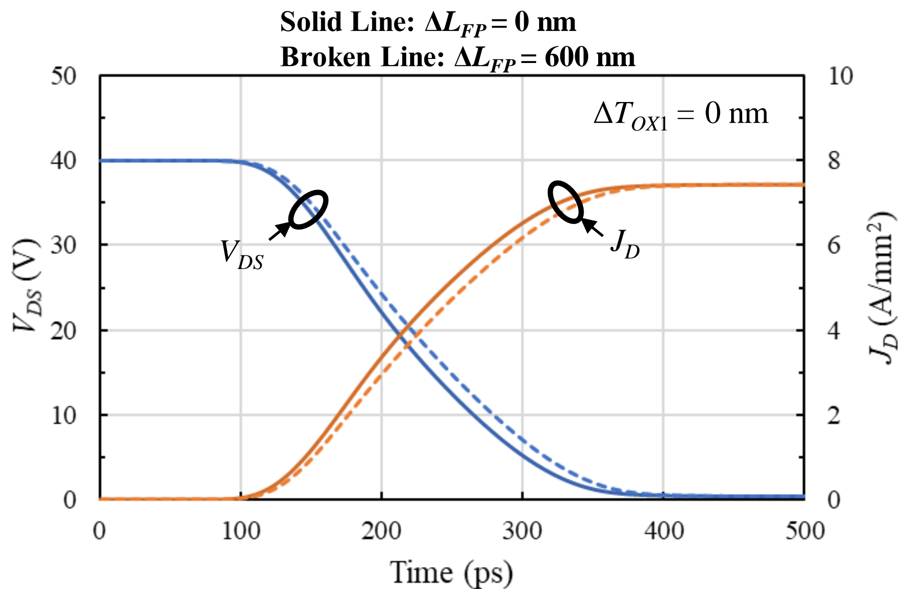
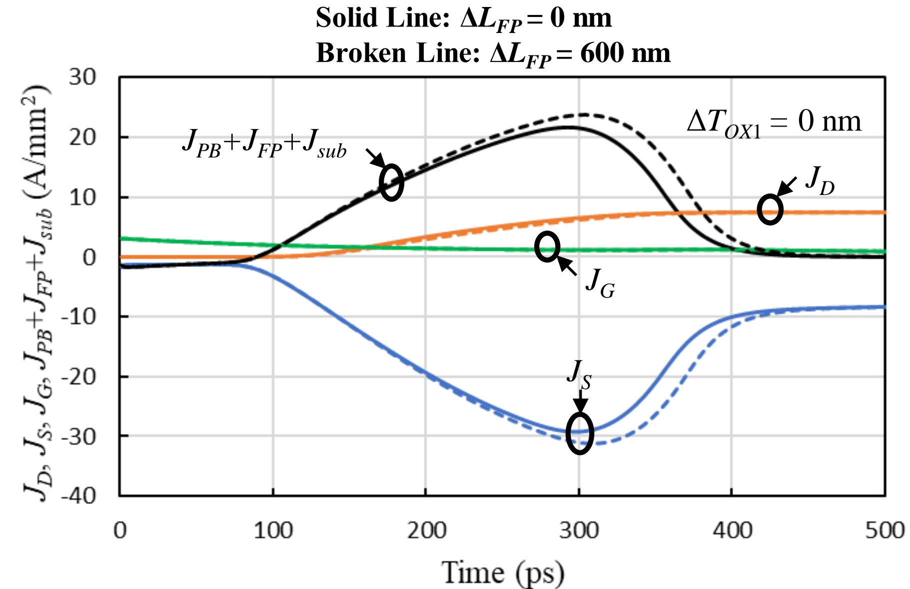
L_{FP} for Turn-on Characteristics





ΔL_{FP} $(=L_{FP} - L_{FP_std})$
ΔT_{OX1} $(=T_{OX1} - T_{OX1_std})$

L_{FP} increase ($\Delta L_{FP} = +600$ nm)

Drain current density (J_D) decrease

V_{DS} increase

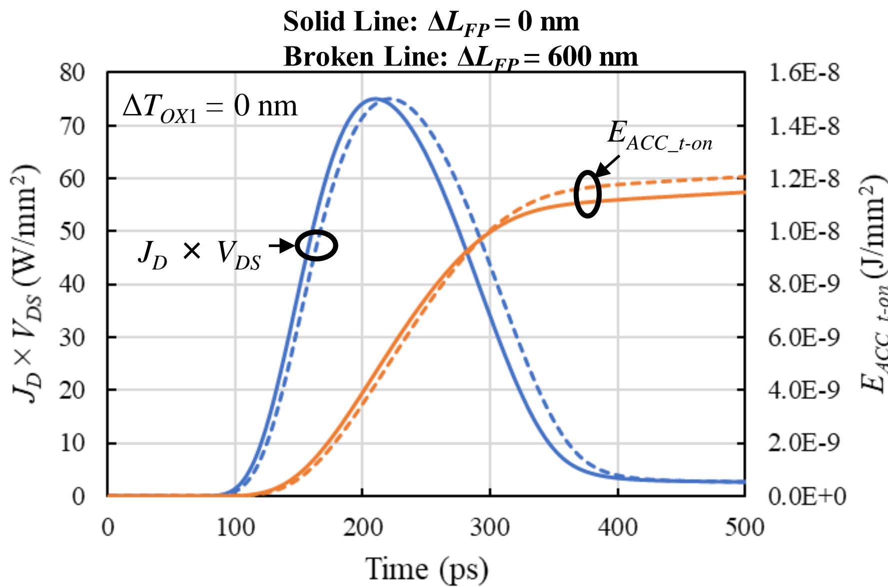
- Saturation state: 100 ps - 320 ps
- C_{FD} increase →

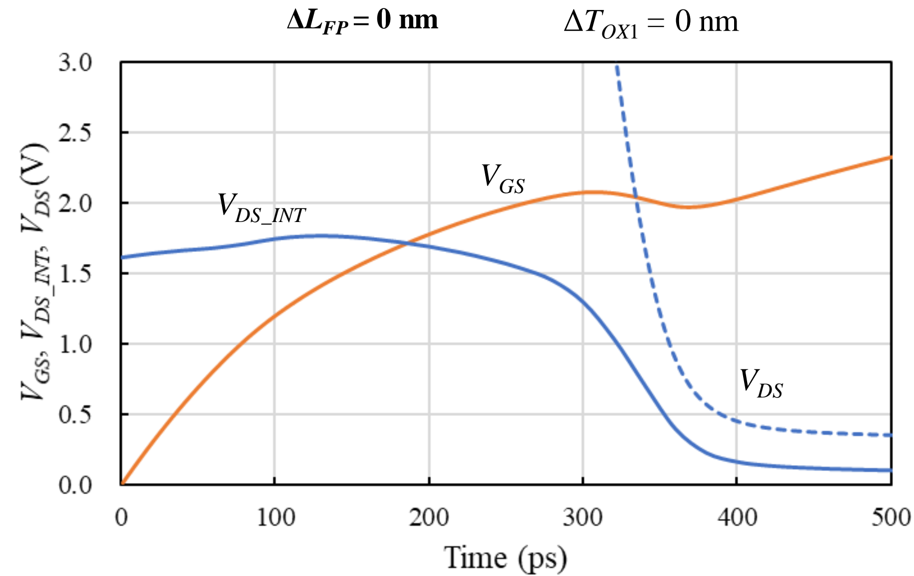
  $J_{PB}+J_{FP}+J_{Sub}$ increase, flow in drift region

  J_D decrease
- Voltage drop in drift region →

  Higher V_{DS}

L_{FP} for Turn-on Characteristics



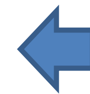


- At rising $P_{D_t\text{-}on}$

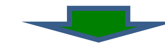
$P_{D_t\text{-}on}(\Delta L_{FP} = +600\ \text{nm}) < P_{D_t\text{-}on}(\Delta L_{FP} = 0\ \text{nm})$

- At falling $P_{D_t\text{-}on}$

$P_{D_t\text{-}on}(\Delta L_{FP} = +600\ \text{nm}) > P_{D_t\text{-}on}(\Delta L_{FP} = 0\ \text{nm})$



Voltage drop in drift region

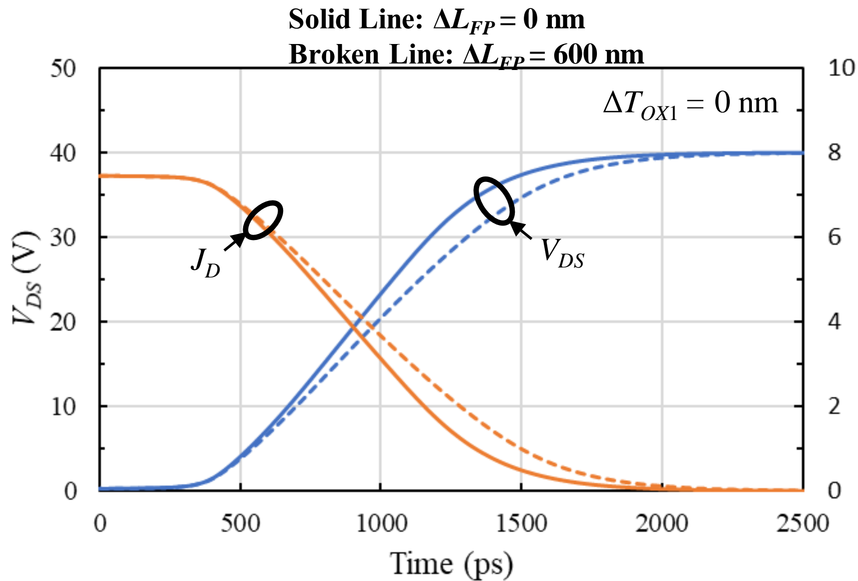


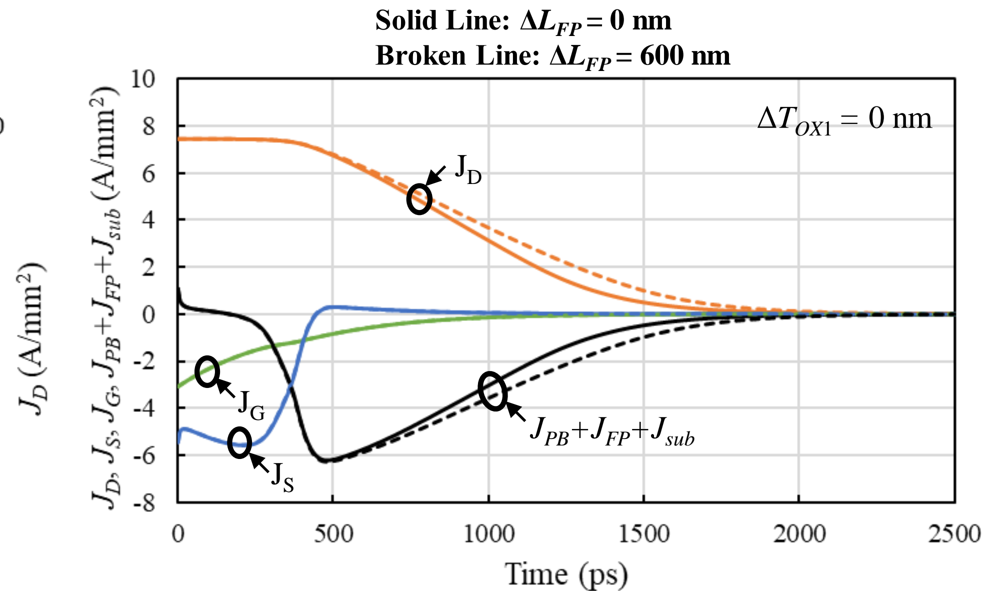
Higher V_{DS}

$P_{D_t\text{-}on}$ (= $J_D \times V_{DS}$) : Power dissipation density

$E_{ACC\ t\text{-}on}$: Accumulated energy dissipation density

L_{FP} for Turn-off Characteristics





- Saturation state: 320 ps - 2000 ps

L_{FP} increase (ΔL_{FP} = +600nm)

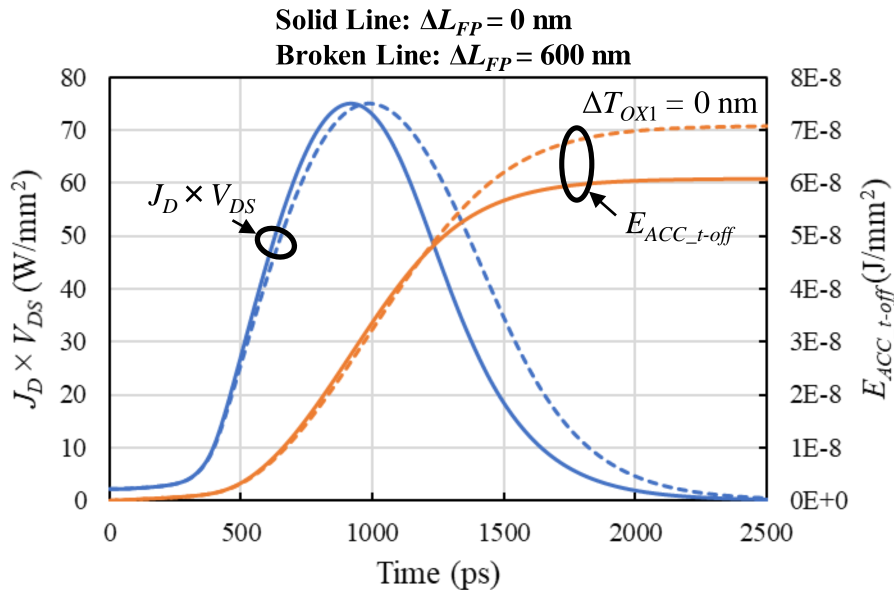
Drain current density (J_D) increase

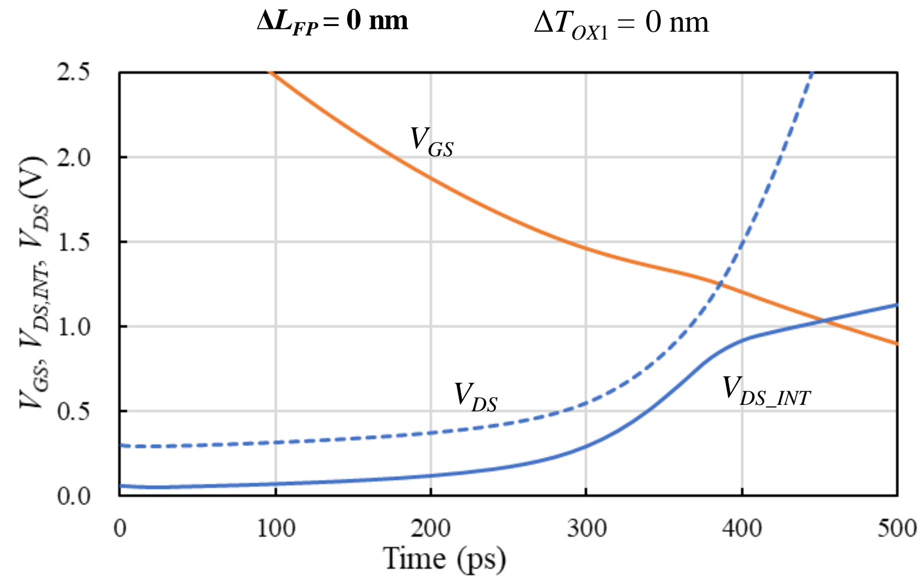
V_{DS} decrease

- C_{FD} increase →
  $J_{PB}+J_{FP}+J_{sub}$ →
  added to drain current density J_D
  → higher J_D

- Short current path decreases voltage drop in drift region → lower V_{DS}

L_{FP} for Turn-off Characteristics





- At rising $P_{D_t\text{-}on}$

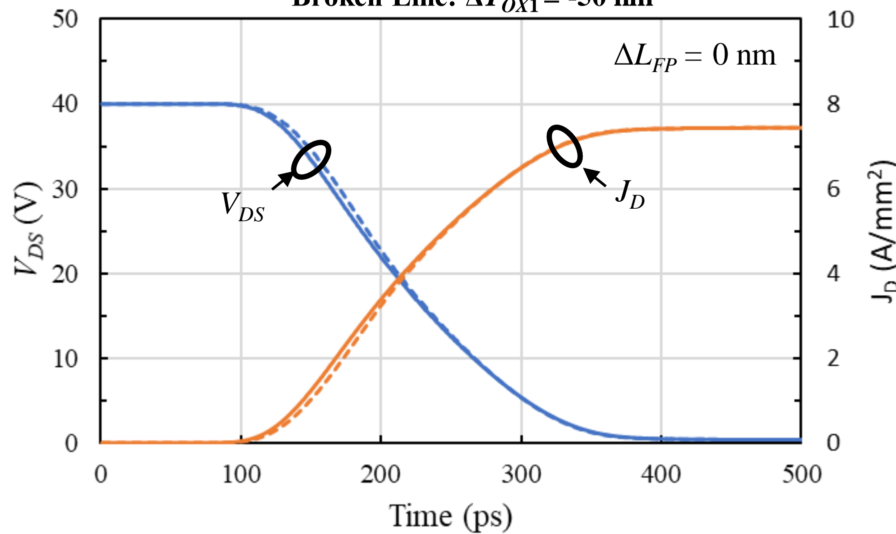
$P_{D_t\text{-}on}(\Delta L_{FP} = +600\text{ nm}) < P_{D_t\text{-}on}(\Delta L_{FP} = 0\text{ nm})$

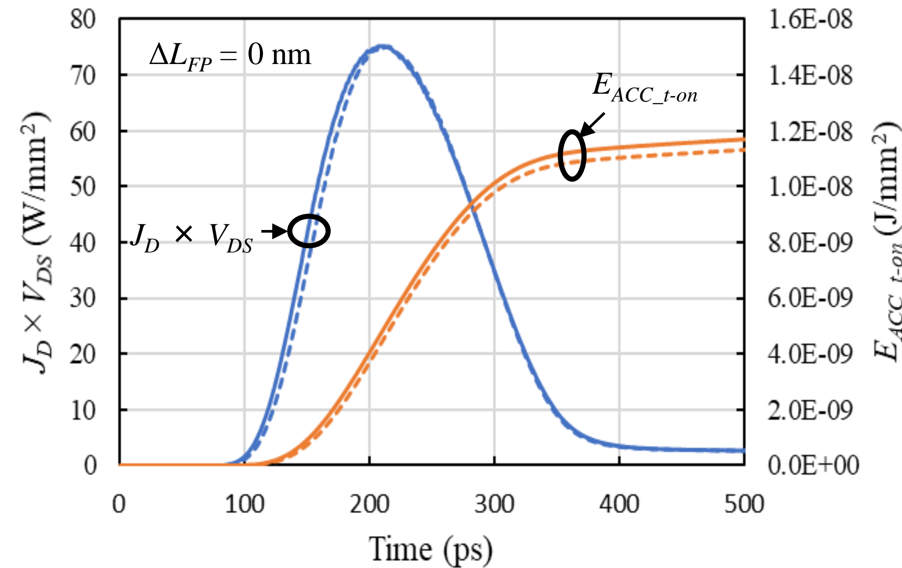
Higher J_D due to higher displacement current density $J_{PB}+J_{FP}+J_{sub}$ for $\Delta L_{FP} = +600$ nm

- At falling $P_{D_t\text{-}on}$

$P_{D_t\text{-}on}(\Delta L_{FP} = +600\text{ nm}) > P_{D_t\text{-}on}(\Delta L_{FP} = 0\text{ nm})$

T_{OX1} for Turn-on Characteristics





ΔL_{FP} (=L_{FP} – L_{FP_std})
ΔT_{OX1} (=T_{OX1} – T_{OX1_std})

T_{OX1} decrease (ΔT_{OX1} = -50 nm)

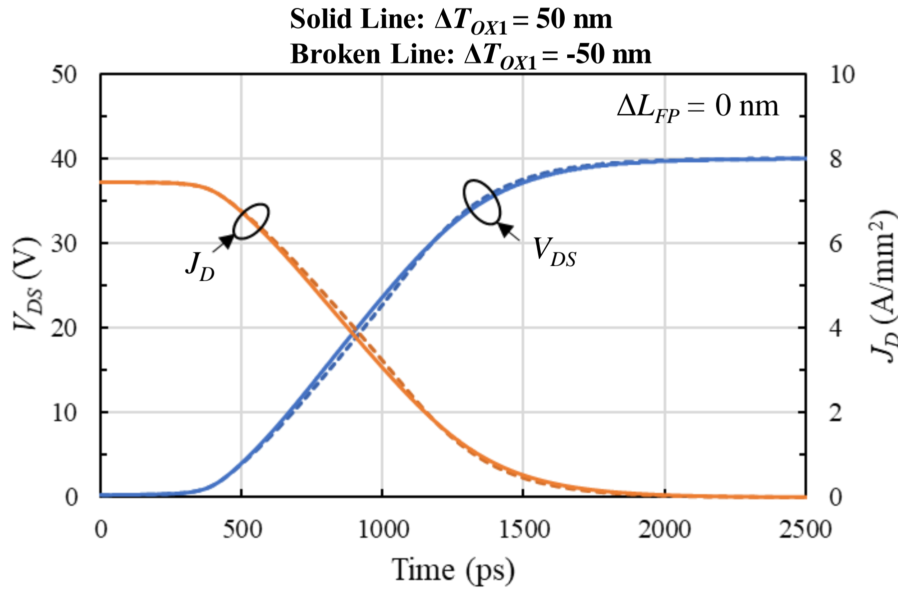
- Drain current density (J_D) decrease
- V_{DS} increase

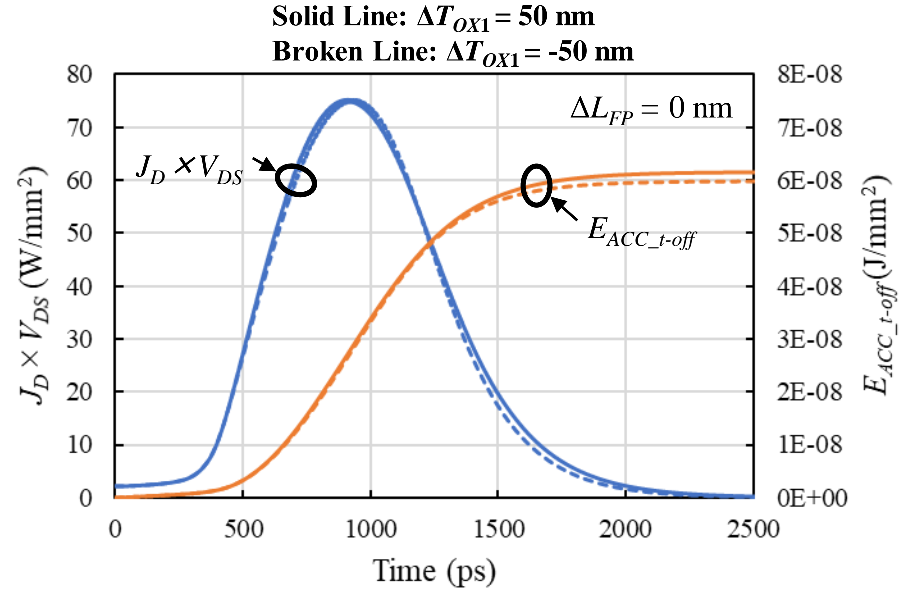
Higher J_{PB}+J_{FP}+J_{sub} ←Larger C_{FD} under intrinsic MOSFET saturation

J_D decrease → $P_{D_t\text{-}on}$ decrease

No change of L_{FP} → Lower $E_{ACC_t\text{-}on}$ for ΔT_{OX1} = -50 nm

T_{OX1} for Turn-off Characteristics





At turn-off rising:

T_{OX1} decrease (ΔT_{OX1} = -50 nm)

- Drain current density (J_D) increase
- V_{DS} decrease
- Higher $J_{PB}+J_{FP}+J_{sub}$ due to larger C_{FD} under intrinsic MOSFET saturation

At turn-off falling:

T_{OX1} decrease (ΔT_{OX1} = -50 nm)

- Drain current density (J_D) decrease
- V_{DS} increase
- Higher V_{DS} → Drift region resistance higher $E_{acc_t\text{-}off}$ decrease, Turn-off loss increase with T_{OX1} increase

OUTLINE

- Research Objective and Background
- Proposed LDMOS Structure and Operation
- Optimization Simulation Results
- Discussion
- Conclusion

Conclusion

LDMOS device design for 40V DC-DC converter

- Field Plate connected to ground
- Its size, location optimization of ΔL_{FP}, ΔT_{OX1}

For 0 nm $\leq \Delta L_{FP} \leq$ 200 nm, –50 nm $\leq \Delta T_{OX1} \leq$ 0 nm,

○ Switching loss reduction by 50 %

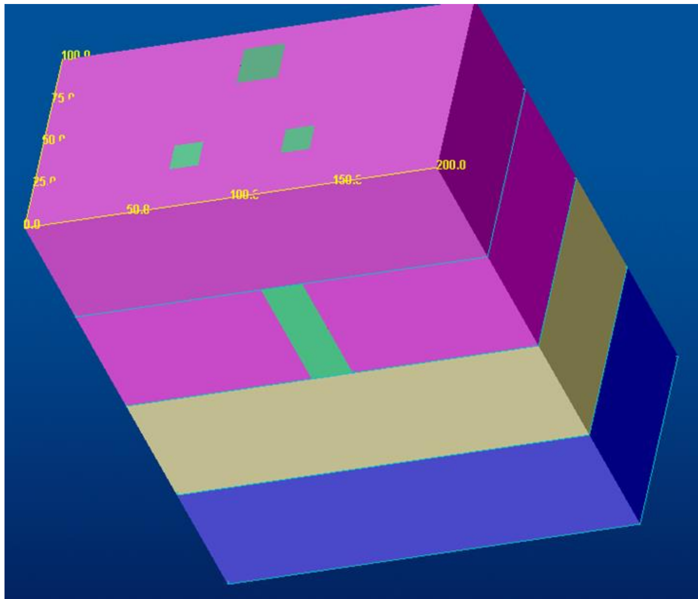
○ High ESD endurance

- Verified with TCAD simulation

Acknowledgments

- AdvanceSoft Corporation
  for providing 3D TCAD simulator.

- Japan Science and Technology Agency
  for assistance of this simulator development
  with A-STEP program.



Thank you for your listening