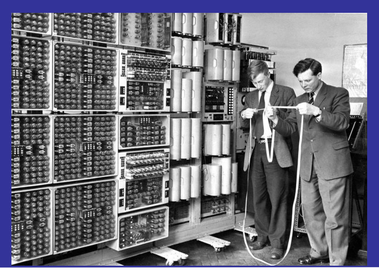
A-12 Efficient Hardware Architecture for Taylor-Series Expansion Calculation Using Distributed Arithmetic with Term Division



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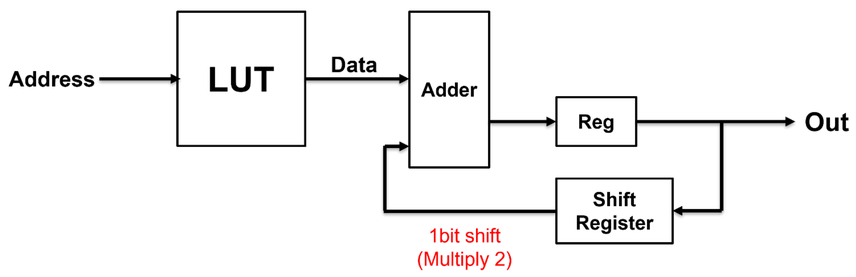
1. Background

Abstract

- Development of efficient DSP for Taylor-series expansion calculation
- Distributed Arithmetic usage
- Proposal of term division method for circuit reduction

Distributed Arithmetic (DA)



Multiply-accumulate operations without multipliers

Direct DA for Taylor-Series Expansion

$$f(x) = a_0 + a_1x + a_2x^2 + a_3x^3 + a_4x^4 + a_5x^5 + a_6x^6 + a_7x^7 + a_8x^8 + a_9x^9$$

Look Up Table

x^0	x^1	x^2	…	x^9	Output Data
0	0	0	…	0	0
1	0	0	…	0	a_0
0	1	0	…	0	a_1
…	…	…	…	…	…
1	1	1	…	1	$a_0 + a_1 + a_2 + \cdots + a_9$

2^{10} ↓ 1024 (rows) × 10 (columns)

Total LUT size:
1024 x 10 = 10,240 bits

$x^0, x^1, x^2, x^3, x^4, x^5, x^6, x^7, x^8, x^9$

8 multiplications

Need reduction of

- Number of multiplications

- Look Up Table (LUT) size

2. Research Objective

Development of efficient dedicated DSP architecture for Taylor-series expansion calculation

$$f(x) = f(\alpha) + \frac{f'(\alpha)}{1!}(x-\alpha) + \frac{f''(\alpha)}{2!}(x-\alpha)^2 + \frac{f'''(\alpha)}{3!}(x-\alpha)^3 + \cdots$$

Reduction of

- Number of multiplications

- Look Up Table (LUT) size

3. Distributed Arithmetic (DA)

$$y = h_0x_0 + h_1x_1 + h_2x_2$$

Bit-series operation in parallel

With LUT and adder, without multiplier

	x_0	x_1	x_2
MSB	1	0	1
	1	1	0
LSB	1	1	1

LUT

x_0	x_1	x_2	Sum
0	0	0	0
1	0	0	h_0
0	1	0	h_1
0	0	1	h_2
1	1	0	$h_0 + h_1$
1	0	1	$h_0 + h_2$
0	1	1	$h_1 + h_2$
1	1	1	$h_0 + h_1 + h_2$

$h_0 + h_1 + h_2$

	x_0	x_1	x_2
MSB	1	0	1
	1	1	0
LSB	1	1	1

LUT

x_0	x_1	x_2	Sum
0	0	0	0
1	0	0	h_0
0	1	0	h_1
0	0	1	h_2
1	1	0	$h_0 + h_1$
1	0	1	$h_0 + h_2$
0	1	1	$h_1 + h_2$
1	1	1	$h_0 + h_1 + h_2$

$$\left(\frac{1}{2} \times (h_0 + h_1 + h_2) + (h_0 + h_1)\right)$$

	x_0	x_1	x_2
MSB	1	0	1
	1	1	0
LSB	1	1	1

LUT

x_0	x_1	x_2	Sum
0	0	0	0
1	0	0	h_0
0	1	0	h_1
0	0	1	h_2
1	1	0	$h_0 + h_1$
1	0	1	$h_0 + h_2$
0	1	1	$h_1 + h_2$
1	1	1	$h_0 + h_1 + h_2$

$$\left(\frac{1}{2} \times \left(\frac{1}{2} \times (h_0 + h_1 + h_2) + (h_0 + h_1)\right) + (h_0 + h_2)\right)$$

	x_0	x_1	x_2
MSB	1	0	1
	1	1	0
LSB	1	1	1

2 bit (Integer part)

$$\left(\frac{1}{2} \times \left(\frac{1}{2} \times (h_0 + h_1 + h_2) + (h_0 + h_1)\right) + (h_0 + h_2)\right) \times 2^2$$

4. Our Approach: Term Division Method

Term division by 2

$$f(x) = \underbrace{(a_0 + a_2x^2 + a_4x^4 + a_6x^6 + a_8x^8)}_{\text{DA 1}} + x^1\underbrace{(a_1 + a_3x^2 + a_5x^4 + a_7x^6 + a_9x^8)}_{\text{DA 2}}$$

x^2, x^4, x^6, x^8

4 + 1 = 5 multiplications

Look Up Table 1

x^0	x^2	x^4	x^6	x^8	Output Data
0	0	0	0	0	0
1	0	0	0	0	a_0
0	1	0	0	0	a_2
…	…	…	…	…	…
1	1	1	1	1	$a_0 + a_2 + a_4 + a_6 + a_8$

2^5 ↓ 32 (rows) × 5 (columns)

Look Up Table 2

x^0	x^2	x^4	x^6	x^8	Output Data
0	0	0	0	0	0
1	0	0	0	0	a_1
0	1	0	0	0	a_3
…	…	…	…	…	…
1	1	1	1	1	$a_1 + a_3 + a_5 + a_7 + a_9$

Total LUT size: 32 x 5 x 2 = 320 bits

5. Verification of Term Division Method

Optimal number of term divisions for N-term Taylor series expansion → $\sqrt{N}$

	Division by	Number of multiplications	LUT size
16 terms	1	14	65536
	2	8	512
	4	6	64
	8	8	32
32 terms	1	30	4294967296
	2	16	131072
	4	10	1024
	8	10	128
	16	16	64
64 terms	1	62	1.84×10^{19}
	2	32	8589934592
	4	18	262144
	8	14	2048
	16	18	256
	32	32	128

Term division **by 2**

$$a_0 + a_2x^2 + a_4x^4 + a_6x^6 + a_8x^8 + a_{10}x^{10} + a_{12}x^{12} + a_{14}x^{14}$$
$$x \times (a_1 + a_3x^2 + a_5x^4 + a_7x^6 + a_9x^8 + a_{11}x^{10} + a_{13}x^{12} + a_{15}x^{14})$$

Term division **by 4**

$$a_0 + a_4x^4 + a_8x^8 + a_{12}x^{12} + x \times \left[(a_1 + a_5x^4 + a_9x^8 + a_{13}x^{12}) + x \times \left[(a_2 + a_6x^4 + a_{10}x^8 + a_{14}x^{12}) + x \times (a_3 + a_7x^4 + a_{11}x^8 + a_{15}x^{12})\right]\right]$$

Term division **by 8**

$$(a_0 + a_8x^8) + x \times \left[(a_1 + a_9x^8) + x \times \left[(a_2 + a_{10}x^8) + x \times \left[(a_3 + a_{11}x^8) + x \times \left[(a_4 + a_{12}x^8) + x \times \left[(a_5 + a_{13}x^8) + x \times \left[(a_6 + a_{14}x^8) + x \times (a_7 + a_{15}x^8)\right]\right]\right]\right]\right]$$

6. Conclusion

- **Distributed arithmetic & Division of terms to Taylor-series expansion calculation**

  ⇒ Reduction of LUT memory size $10240 \Rightarrow 320$

  ⇒ Reduction of x^n calculation by Multiplier $8 \Rightarrow 5$

- **Future Work**

  Evaluation with FPGA