Efficient Hardware Architecture for Taylor-Series Expansion Calculation Using Distributed Arithmetic with Term Division

Xaybandith Hemthavy
J. Wei, S. Katayama, A. Kuwana, H. Kobayashi, K. Kubo
Gunma University, Oyama National College of Technology

Summary

Development of efficient dedicated DSP architecture for Taylor-series expansion calculation

Distributed Arithmetic (multiply-accumulate without multipliers)

Proposed term division method

Speed improvement & circuit reduction

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● Research Objective

Development of efficient dedicated DSP architecture for Taylor-series expansion calculation

$$f(x) = a_0 + a_1x + a_2x^2 + a_3x^3 + a_4x^4 + a_5x^5 + a_6x^6 + a_7x^7 + a_8x^8 + a_9x^9$$

● Problems for Distributed Arithmetic (DA)

Need for reduction of

- Number of multiplications
- Look Up Table (LUT) size

$x^0, x^1, x^2, x^3, x^4, x^5, x^6, x^7, x^8, x^9$

8 multiplications

Look Up Table

x^0	x^1	x^2	…	x^9	Output Data
0	0	0	…	0	0
1	0	0	…	0	a_0
0	1	0	…	0	a_1
…	…	…	…	…	…
1	1	1	…	1	$a_0 + a_1 + a_2 + \cdots + a_9$

2^{10} ↓ 1024

10

Total LUT size:
1024 x 10 = 10,240 bits

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● Our Approach : Term Division Method

$$f(x) = (a_0 + a_2x^2 + a_4x^4 + a_6x^6 + a_8x^8) + x^1(a_1 + a_3x^2 + a_5x^4 + a_7x^6 + a_9x^8)$$

x^2, x^4, x^6, x^8

4 + 1 = 5 multiplications

Look Up Table 1

x^0	x^2	x^4	x^6	x^8	Output Data
0	0	0	0	0	0
1	0	0	0	0	a_0
0	1	0	0	0	a_2
…	…	…	…	…	…
1	1	1	1	1	$a_0 + a_2 + a_4 + a_6 + a_8$

2^5 ↓ 32

5

Look Up Table 2

x^0	x^2	x^4	x^6	x^8	Output Data
0	0	0	0	0	0
1	0	0	0	0	a_1
0	1	0	0	0	a_3
…	…	…	…	…	…
1	1	1	1	1	$a_1 + a_3 + a_5 + a_7 + a_9$

Total LUT size: 32 x 5 x 2 = 320 bits

Distributed Arithmetic (DA) : Multiply-Accumulate calculation
Bit-serial operation in parallel
with LUT + adder
without multiplier