A-7

Segmented DAC Linearity Improvement Algorithm Using Unit Cell Sorted Alternately with Digital Method

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Background and Objective

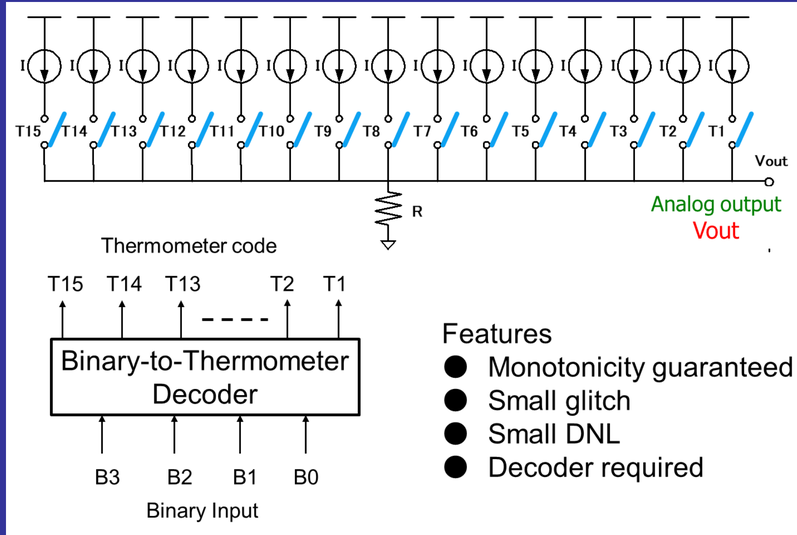
Digital-to-Analog Converter (DAC)

- Key component in modern transmitter circuits.
- High linearity is required.

Nano-CMOS implementation of DAC
- Device mismatch is large
- DAC linearity deteriorates
- Digital circuit can be implemented with small chip area

Objective:
Development of digital calibration method for DAC non-linearity.
Digitally-assisted analog technology.

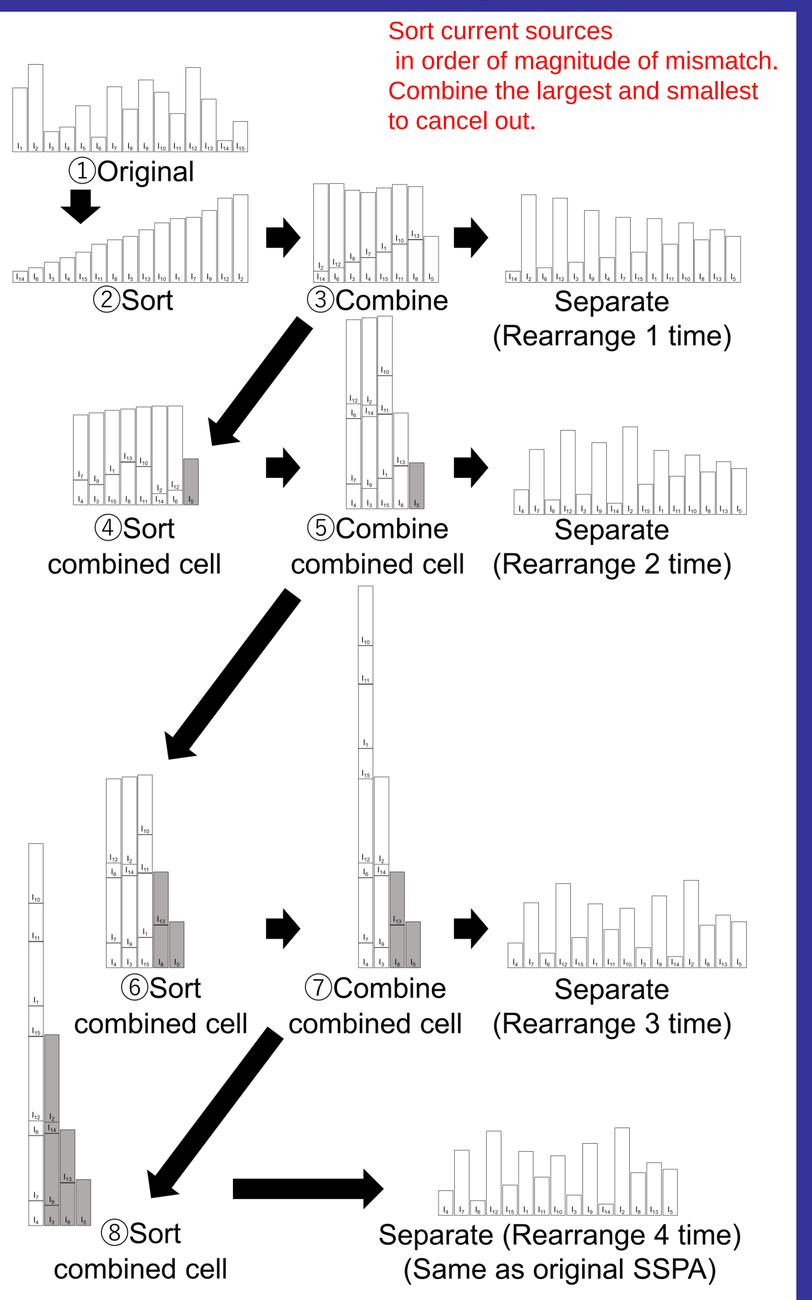
Segmented DAC Configuration: 4-bit case



Features
- Monotonicity guaranteed
- Small glitch
- Small DNL
- Decoder required

Current sources magnitude are not equal because of mismatch.
Mismatch causes DAC non-linearity.

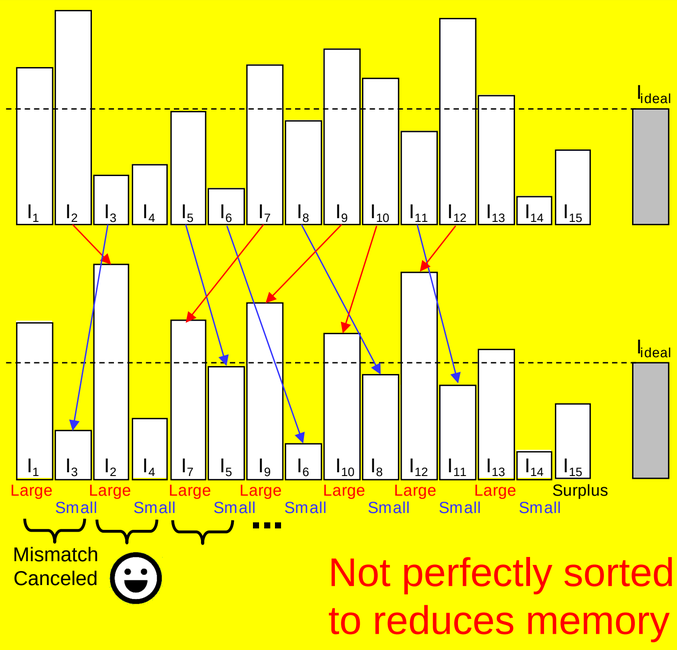
"SSPA[1]" and "Rearrange[2]" Calibration Algorithm



[1] T. Chen, et. al. , “A 14-bit 200-MHz Current-Steering DAC with Switching Sequence Post-Adjustment Calibration”, IEEE Asian Solid-State Circuits Conference, Hangzhou, China (Nov. 2006).

[2] Y. Liu, et. al. “Optimization of Segmented DAC Linearity Improvement Algorithm Using Unit Cell Sorting with Digital Method”, The 31st International Workshop on Post-Binary ULSI Systems (ULSIWS), (May 2022)

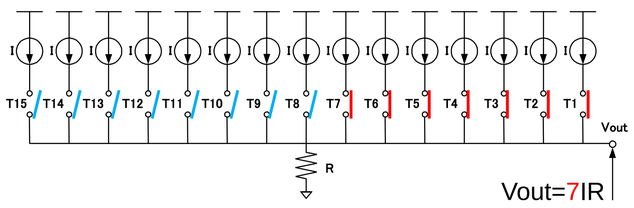
Proposed "Alternate" Calibration Algorithm



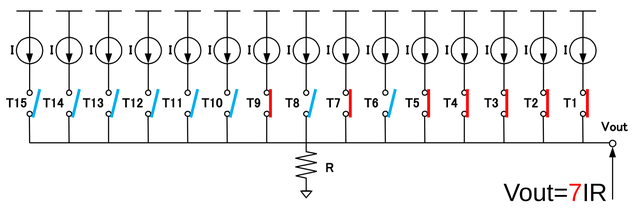
Not perfectly sorted
to reduces memory space
and number of comparisons.

Operation example: Digital Input = 7

① Original order

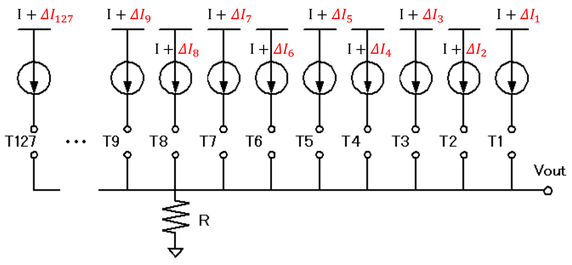


② Calibrated order by "Alternate" algorithm



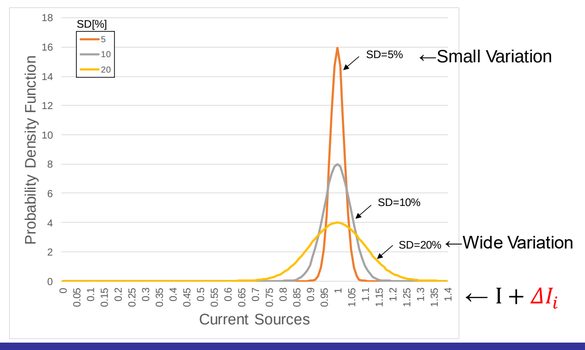
Simulation Conditions

Assuming 7-bit DAC, 127 current sources are used.
The current sources have mismatches. (ΔI_i)



Mismatches vary within the range of SD [%].

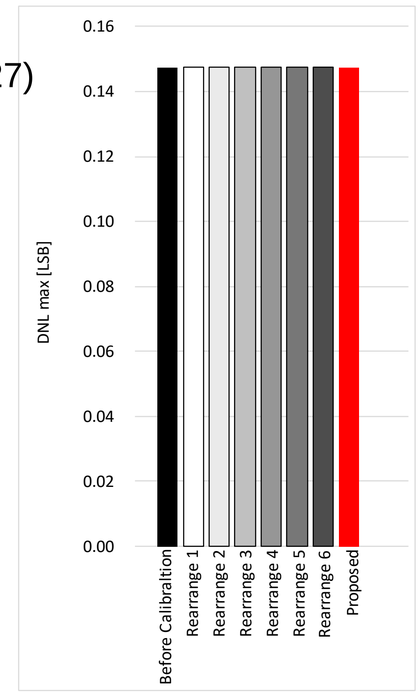
SD=10
in this poster.



Simulation Result (DNL)

DNLmax=
maximum(DNL1: DNL127)

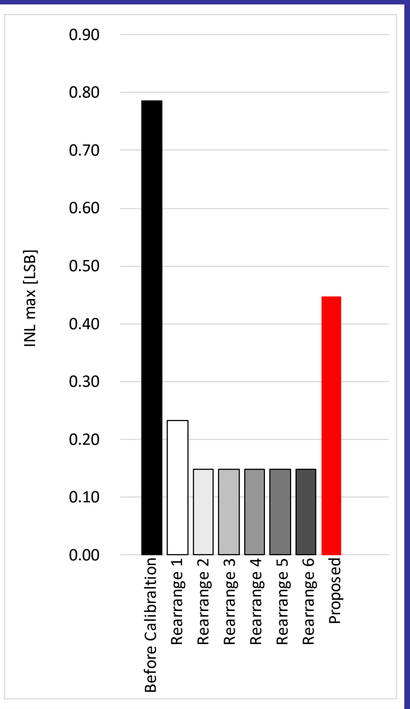
DNL does not change by both of Rearrange and proposed method.



Simulation Result (INL)

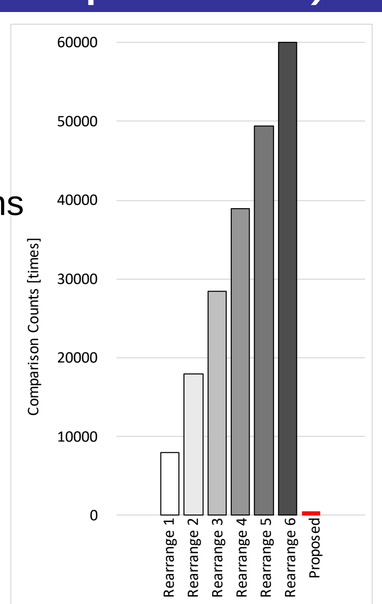
INLmax=
maximum(INL1: INL127)

INL is sufficiently small in Rearrange 2.
The proposed method cannot reduce INL as much as Rearrange, but INL is reduced to about 0.56 if the INL of before calibration is 1.0.



Simulation Result (Number of comparisons)

Proposed method significantly reduces the number of comparisons to less than one-tenth that of Rearrange 1

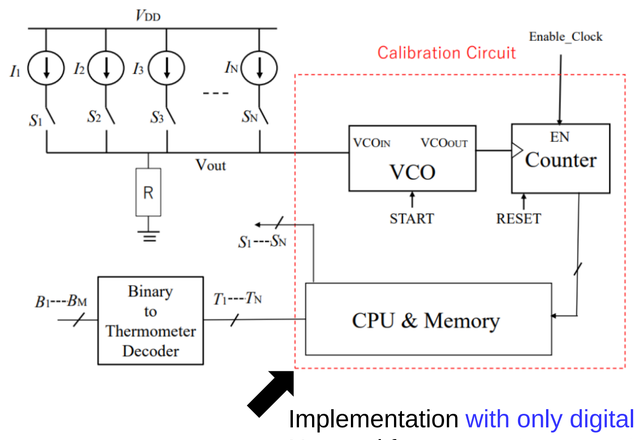


DAC Architecture

Current comparator is used in conventional SSPA.

T. Chen, G. Gielen (KU Leuven), “A 14-bit 200-MHz Current-Steering DAC with Switching Sequence Post-Adjustment Calibration”, IEEE ASSCC (Nov. 2006)

Our proposal is VCO instead of comparator.



Implementation with only digital circuit.
No need for a current comparator.

Conclusion

- Segmented current-steering DAC linearity improvement algorithm is investigated.
- Proposed “Alternate” method can...
  - ✓ reduces INL to about 0.4 – 0.6 if INL of before calibration is 1.0.
  - ✓ significantly reduces the number of comparisons during calibration.
  - ✓ reduce required memory space.
    If N current sources & M-bit DAC input,
    - "SSPA" and "Rearrange": $N \times 2^M$
    - Proposed "Alternate" requires: N