Segmented DAC Linearity Improvement Algorithm Using Unit Cell Sorted Alternately with Digital Method

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Abstract - This paper describes a self-calibration method for a current-steering Digital-to-Analog Converter (DAC) with a voltage-controlled oscillator (VCO). It is a digital method and does not require high precision analog circuits; the VCO needs only monotonic characteristics but it does not need linearity. Mismatches among the unit current sources in the current-steering segmented DAC cause the overall DAC nonlinearity, and the VCO measures the order of each current source value. The measured information is stored in memory, and based on it, each current source is sorted to reduce the DAC nonlinearity. Especially we have investigated with simulations whether the comparison algorithms can improve the DAC Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) with several mismatch conditions. We present its principle and simulation results.

I. Introduction

Digital-to-Analog Converter (DAC) is a key component for modern transmitter circuits, and there its high linearity is required. For its nano-CMOS implementation, the device mismatch is large and hence the analog circuit characteristics may be deteriorated. However, there, digital circuit can be implemented with small chip area and hence so-called the digitally-assisted analog technology is attractive.

This paper investigates the DAC linearity improvement algorithm and circuit; the DAC under investigation employs the current-steering segmented architecture for high-speed and low glitch applications as shown in Fig. 1.

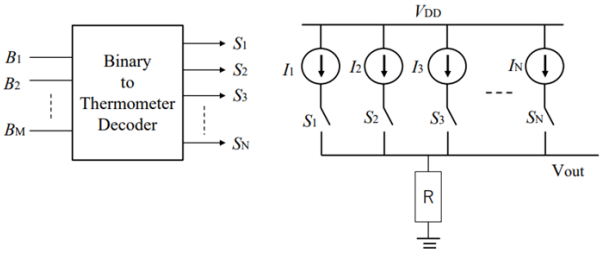


Fig. 1. Segmented current-steering DAC configuration.

The switching sequence post adjustment (SSPA) is one of the DAC linearity improvement algorithms and circuits [1]. It is based on the idea that INL can be reduced by canceling current source mismatches. It is proposed that using VCOs to compare current sources simplifies the circuit by eliminating the need for linearity (only monotonically decreasing linearity is needed) to determine the size of the current sources [2]. Notice that here the sorting algorithm is based on the unit current cell value measurement results. However, in another research in [3], the measurement is not performed but the sorting is based on the systematic error tendency depending on the unit cell layout position. In comparison, the SSPA method is expected to accurately estimate the reducing ratio of DNL and INL.

Furthermore, we have studied in detail the difference in the effect of SSPA on DNL and INL when the variation of current sources is large and when the variation of current sources is small [4]. We also devised a method called “Rearrange” to optimize the SSPA steps to reduce the calibration time and circuit size [5]. This time, we developed the “Alternate” method to further reduce calibration time and circuit size.

II. Problem Formulation

Consider the segmented current-steering DAC in Fig. 1. Ideally the designed current sources satisfy the following:

$$I_1 = I_2 = I_3 = \ldots = I_N \quad (1)$$

However, in reality, due to device mismatches, they are not identical and expressed as follows:

$$\begin{aligned} I_1 &= I + \Delta I_1, \\ I_2 &= I + \Delta I_2, \\ I_3 &= I + \Delta I_3, \ldots, \\ I_N &= I + \Delta I_N \end{aligned} \quad (2)$$

Here I is defined as their average of I_1, I_2, I_3,…and I_N:

$$I = \frac{1}{N}\left[I_1 + I_2 + I_3 + \ldots + I_N\right] \quad (3)$$

ΔI_1, ΔI_2, ΔI_3,…, and ΔI_N can be positive, zero or negative. The sum of the mismatches can be obtained from Eqs. (2) and (3) as follows:

$$\Delta I_1 + \Delta I_2 + \Delta I_3 + \ldots + \Delta I_N = 0 \quad (4)$$

The DAC operation in Fig. 1 is as follows: For the DAC input of zero, all switches are off, and the analog output of $V_{OUT} = 0$. For the DAC input of one, the switch of S1 is on and $V_{OUT} = RI_1 = R\ (I + \Delta I_1)$. For the DAC input of two, S1 and S2 are on and $V_{OUT} = R\ (I_1 + I_2) = \mathrm{R}\ (2\ I + \Delta I_1 + \Delta I_2)$. Similarly, for the DAC input of k, $V_{OUT} = R\ (I_1 + I_2 + \ldots + I_k) = \mathrm{R}\ (\mathrm{k}\ I + \Delta I_1 + \Delta I_2 + \ldots + \Delta I_k)$.

We see that non-zero values of ΔI_1, ΔI_2, ΔI_3,…, and ΔI_N can cause the DAC nonlinearity. Let us consider to select n1-th, n2-th,.. and nk-th, current sources for DAC input of k, as follows:

$$\begin{aligned} V_{OUT} &= R\ (I_{n1} + I_{n2} + \ldots + I_{nk}) \\ &= R\ (\mathrm{k}\ I + \Delta I_{n1} + \Delta I_{n2} + \ldots + \Delta I_{nk}) \end{aligned} \quad (5)$$

If the following is satisfied

$$|\Delta I_{n1} + \Delta I_{n2} + \ldots + \Delta I_{nk}| < |\Delta I_1 + \Delta I_2 + \ldots + \Delta I_k| \quad (6)$$

Then the integral nonlinearity at the input k can be reduced. In this paper, we investigate the unit cell selection algorithm which minimizes $|\Delta I_{n1} + \Delta I_{n2} + \ldots + \Delta I_{nk}|$ as much as possible.

III. Unit Current Cell Sorting Algorithm

A. *Conventional Algorithm (SSPA)*

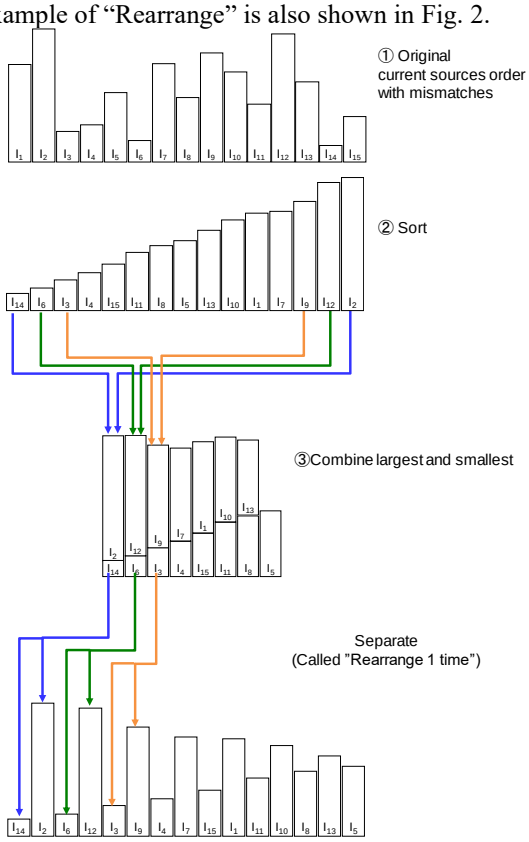
The switching sequence post adjustment (SSPA) algorithm [1] is a calibration method that can change the switching sequence of current cells especially after fabrication process, and a very good integral linearity of the DAC can be obtained. Its algorithm is as follows (Fig. 2):

1) The values of the unit current cells are measured with the VCO though it is not linear, but monotonicity is kept, and they are sorted in the memory from the lowest to the highest order.
2) Then, the sorted unit current cells are rearranged by arranging small unit current cells between two large cells, using the CPU.
3) After that, each two neighboring unit current cells are summed.
4) Then summed unit current cells are again measured and sorted as 1).
5) They are rearranged as 2).
6) Finally, the final sequence is obtained.

Remark:
(i) Current summation can be done simply with their connection in parallel, obeying the Kirchhoff current law.
(ii) We can have redundant unit current cells. For example, we have N+2 unit current cells and discard two cells with the largest and the smallest unit current cells, and we perform the same method to the remaining N unit current cells as described above.

B. *Conventional Algorithm (Rearrange)*

When there are N=2^n current sources, SSPA takes long time because "combine, sort, and rearrange" must be performed n times. "Rearrange" is based on the idea that SSPA can be stopped midway and the number of rearrangements optimized. An example of "Rearrange" is also shown in Fig. 2.



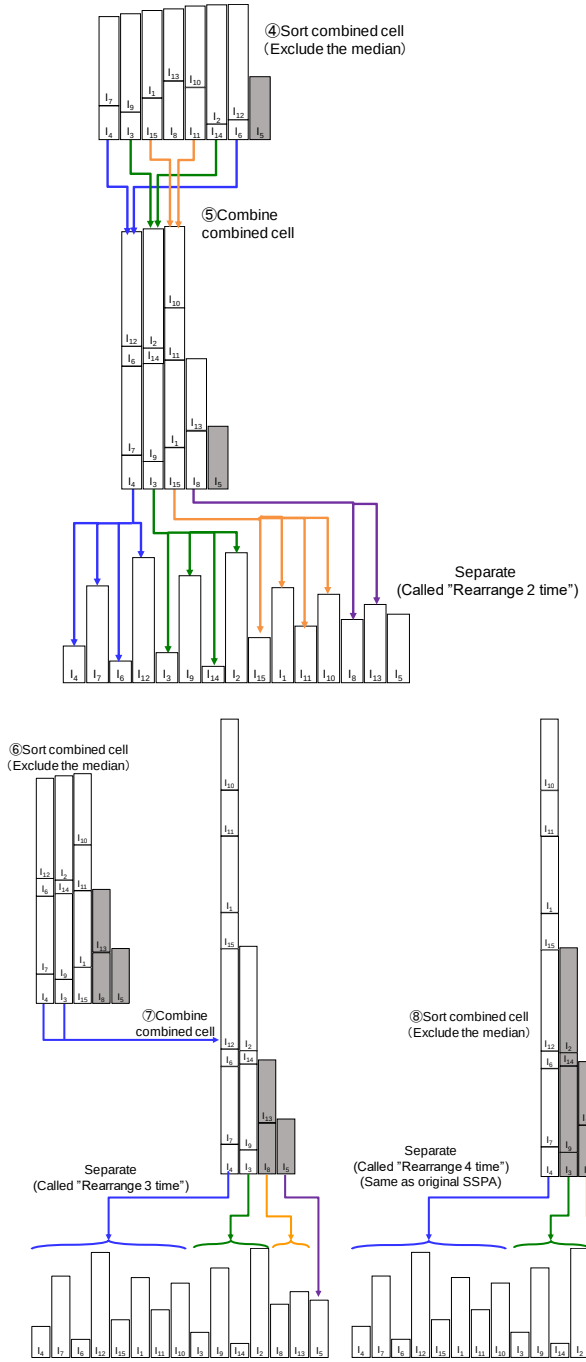


Fig. 2. Explanation of SSPA and "Rearrange" algorithm with 15 current sources example.

C. *Proposed Algorithm (Alternate)*

SSPA and Rearrange require all current sources to be completely sorted in ascending order. As described later, our proposal algorithm repeatedly compares the magnitudes of two current sources using VCO for current source comparison. A large number of comparisons are required for sorting. Therefore, to reduce the number of comparisons, we propose the following algorithm: compare I_{ideal} with each current source I_i and sort them alternately as greater than I_{ideal}, less than I_{ideal}, and so on. In the example in Fig. 3, the initial conditions are larger, larger, smaller, smaller, smaller, smaller, larger, smaller, larger, larger, smaller, larger, larger, smaller, smaller. After calibration, they become larger, smaller, larger, smaller, larger, smaller, larger, smaller, larger, smaller, larger, smaller, larger, smaller, and finally, the surplus (smaller). This algorithm is named "Alternate" and is expected to reduce the number of comparisons compared to conventional SSPA and Rearrange.

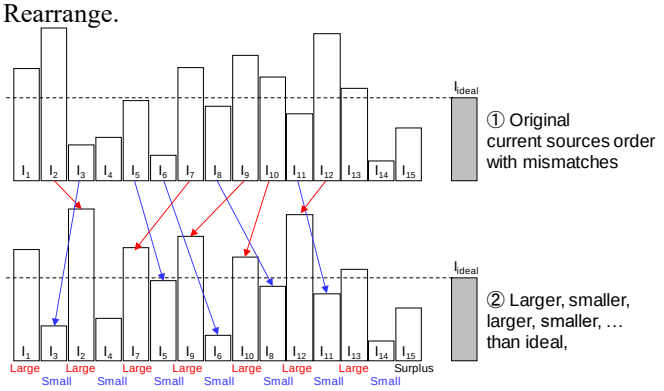
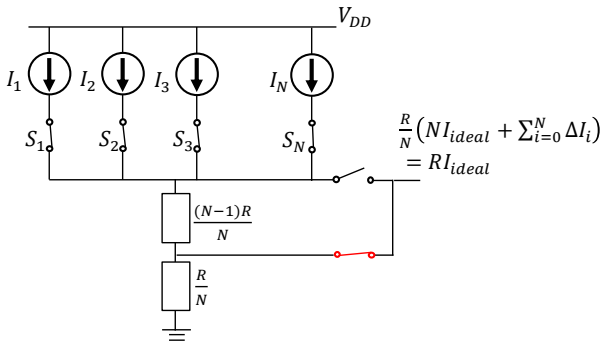
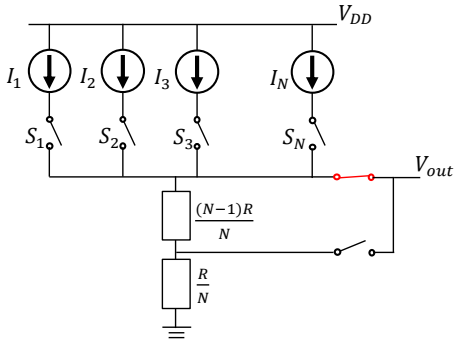


Fig. 3. Proposed "Alternate" calibration algorithm with 15 current sources example.

I_{ideal} is the same as I in Eq. (3). It is measured using resistor divider as shown in Fig. 4(a). $\sum_{i=0}^{N} \Delta I_i$ is 0 according to Eq (4); I_{ideal} can be obtained as the average of N currents. Furthermore, by switching the switch as shown in Fig. 4(b), the DAC can be used without changing the circuit. As the value of I_{ideal} varied depending on the variation of ΔI, a resistor driver as shown in Fig. 4 was used.



(a) Measurement of I_{ideal}.



(b) Use as a DAC.

Fig. 4. Circuit to measure I_{ideal} and switch to use as DAC.

IV. Simulation Results

A. *Simulation settings and 7-bit DAC as example*

Assuming a 7-bit DAC, 127 current sources are used in the first simulation. The current sources have mismatches as shown in Eq. (2). In this study, the current source was assumed to vary in a normal distribution with standard deviation σ (defined as SD/2) around the mean value I defined by Eq. (3). It means that it varies within the range of SD [%] concerning the magnitude I of the current source. An example for I=1.0 and SD=5, 10, and 20 are shown in Fig. 5. The larger the SD, the larger the mismatches. The simulation was performed by varying the degree of mismatches from 1% to 20% as parameter SD.

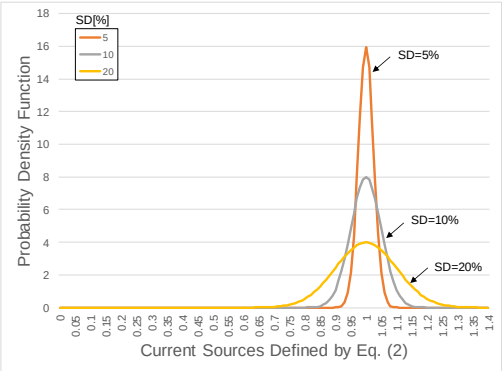


Fig. 5. Example of the current sources mismatches.

The mismatches are calculated using the standard rand function of C language, using the current time as the seed of the rand function. Since each run produced a different value, we ran the simulation 10 times. For each simulation, INLmax and DNLmax were calculated according to Eqs (7) and (8). In other words, we obtained INLmax and DNLmax for 10 times. 10 INLmax and DNLmax were arithmetically averaged, respectively.

$$\mathrm{INLmax}=\mathrm{maximum}(\mathrm{INL}_1:\mathrm{INL}_{127}) \quad (7)$$

$$\mathrm{DNLmax}=\mathrm{maximum}(\mathrm{DNL}_1:\mathrm{DNL}_{127}) \quad (8)$$

The maximum values of DNL and INL are shown in Figs. 6 and 7. Only the case of a variation of current sources mismatches SD=10 is shown as an example. Without calibration, with current sources rearranged with the proposed algorithm in the previous study (called Rearrange), and the proposed algorithm in this study are compared respectively. DNL does not change by both of Rearrange and proposed method. INL is sufficiently small in Rearrange 2, as previously clarified. The proposed method cannot reduce INL as much as Rearrange, but INL is reduced to about 0.56 if the INL of before calibration is 1.0.

Furthermore, the number of comparisons is shown in Fig. 8. the proposed method significantly reduces the number of comparisons to less than one-tenth that of Rearrange 1.

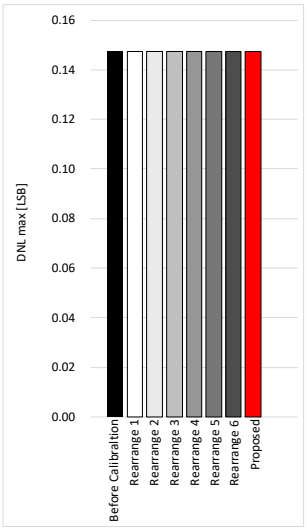


Fig. 6. The maximum value of DNL.

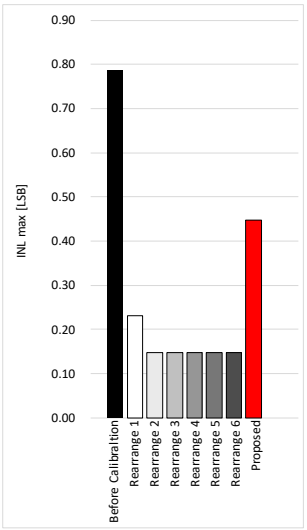


Fig. 7. The maximum value of INL.

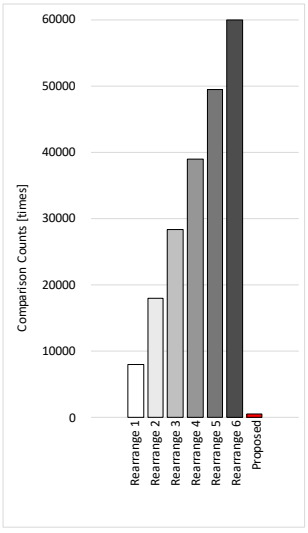
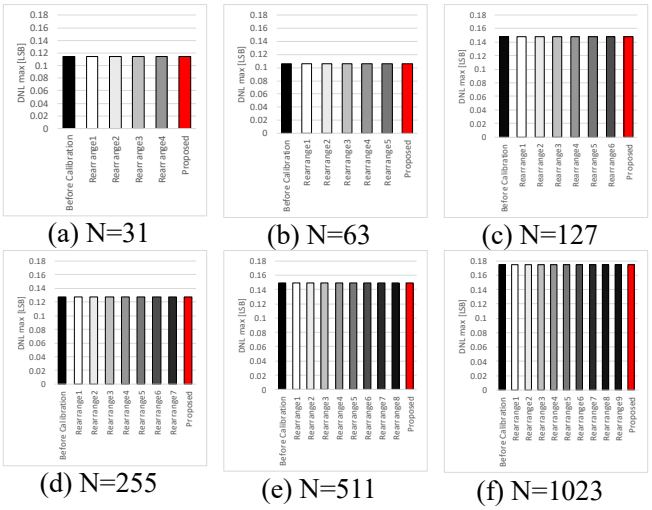


Fig. 8. Number of comparisons performed to sort current sources.

B. *Comparison of different number of current sources*

Assuming 5-bit, 6-bit, ..., 10-bit DACs, that is, 63, 127, 255, 511,1023, 2047 current sources are used in the simulation respectively. SD = 10 in all cases.

The maximum value of DNL, calculated in the same way as in Fig. 6, is shown in Fig. 9. The reason for the different number of graphs is that the number of Rearrange increases with the number of current sources as shown in Fig. 2. The more current sources there are, the larger the DNL tends to be. However, it is also considered to depend on the variation of the current sources with mismatches. As explained in chapter IV, section A, the simulations were run 10 times and averaged. It is considered that running the simulation a greater number of times and taking the average would provide a more accurate measure of trends, it will be one of the future works.

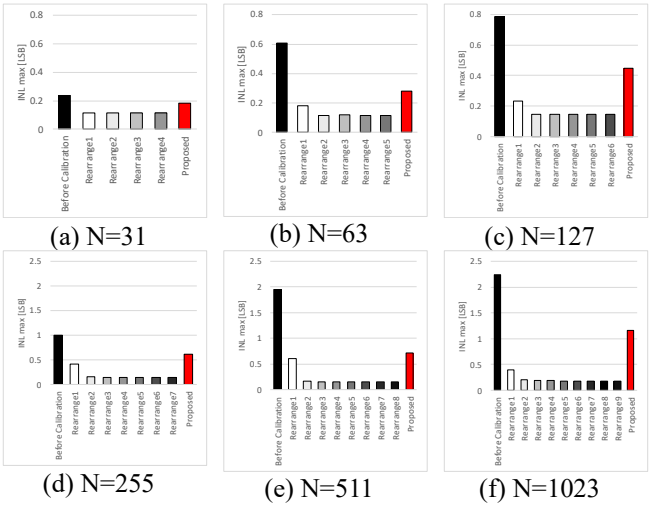


(a) N=31 (b) N=63 (c) N=127

(d) N=255 (e) N=511 (f) N=1023

Fig. 9. The maximum value of DNL.

Figure 10 shows the INL calculated in the same way as in Fig. 7. When the INL of before calibration was 1.0, Fig. 11 shows what value INL was reduced by Rearrange1 and the proposed method, respectively (as noted in Section A, this is reduced to 0.56 when there are 127 current sources). When N is 63 or more, Rearrange1 can reduce to between 0.2 and 0.4, and proposed to between 0.4 and 0.6. This is also likely to depend on the variability of the mismatches and will be studied in more detail in the future.



(a) N=31 (b) N=63 (c) N=127

(d) N=255 (e) N=511 (f) N=1023

Fig. 10. The maximum value of INL.

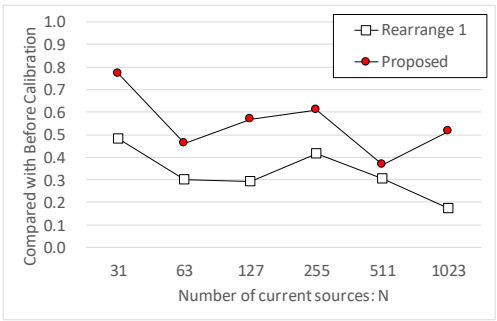
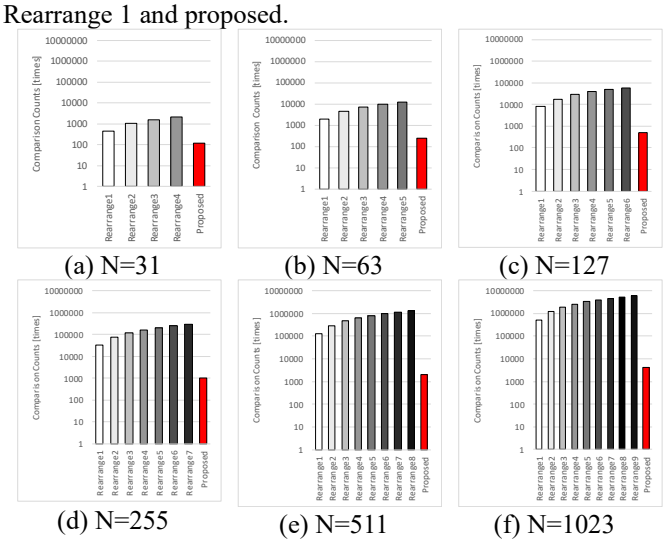


Fig. 11. Reduced INL, where INL before calibration is 1.0.

Figure 12 shows the number of comparisons calculated in the same way as in Fig. 8. The vertical axis is logarithmic. The number of comparisons between Rearrange 1 and proposed is summarized in Fig. 13. Number of comparisons of Rearrange 1 is about $\frac{1}{2}N^2$, proportional to N^2 because all N current sources need to be sorted. But that of the proposed method is $4N$, proportional to only N. Therefore, the larger N, the greater the difference in the number of comparisons between Rearrange 1 and proposed.



(a) N=31 (b) N=63 (c) N=127

(d) N=255 (e) N=511 (f) N=1023

Fig. 12. Number of comparisons performed to sort current sources.

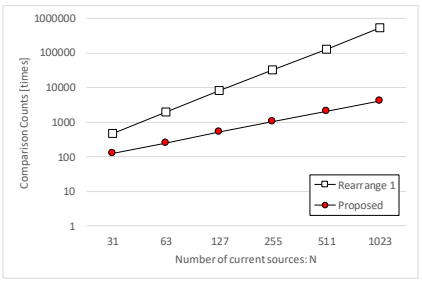


Fig.13. Changes in comparison counts due to number of current sources and calibration method.

V. DAC Architecture with Sorting Algorithm

We investigate here unit current cell sorting techniques. Notice that we can measure the order from the smallest to the largest unit current cell values with a digital method; we measure the number of the VCO cycles during long enough constant time by a digital counter. Fig. 14 shows the segmented current-steering DAC with the sorting algorithm. Current comparator is used in conventional SSPA.

A. During calibration mode

As shown in Fig. 14, the CPU controls the switches one by one, and the VCO and the binary counter measure each unit current cell value as a digital value and stored in the memory. Then the CPU performs the above-mentioned sorting

algorithm: two switches are on and again the VCO and the binary counter measure the sum of them. Their measured values and their order information are stored in the memory.

B. *During normal mode*

The binary input data are decoded into the thermometer code data, and combined with the calibration data stored in the memory, the switches are controlled.

Fig. 15 shows a VCO circuit with current-controlled inverters and START circuit.

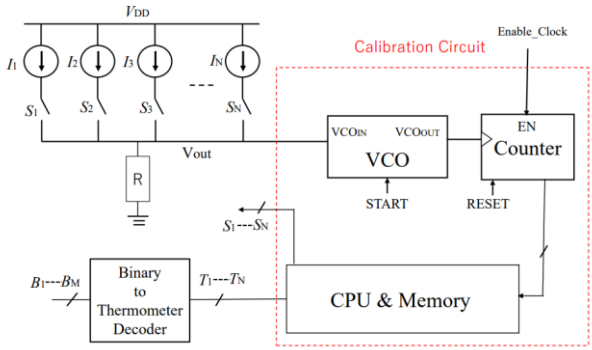


Fig. 14. Explanation of the calibration circuit.

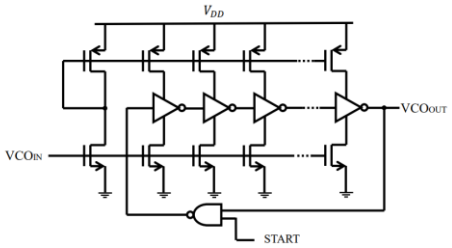


Fig. 15. VCO circuit with current-controlled inverters and START circuit.

VI. Conclusion

This paper has investigated the segmented current-steering DAC linearity improvement algorithm using the unit current cell sorting. Current cells can be arranged alternately larger or smaller than an ideally sized current source to offset mismatches and reduce overall INL. The algorithm is named "Alternate". Our simulation results show that the proposed "Alternate" method cannot reduce INL as much as "Rearrange", but INL is reduced to about 0.4 – 0.6 if INL of before calibration is 1.0. On the other hand, the number of comparisons during calibration of the proposed method significantly reduces. That of "Rearrange" is proportional to the square of the number of current sources, that of the proposed method is proportional to the number of current sources, so the difference in the number of times increases as the number of current sources increases.

Furthermore, the required memory space can be reduced. SSPA and Rearrange requires $N \times 2^M$ memory spaces when the number of current sources are N and the DAC input is M-bit [2]. The proposed method only requires N memory spaces, since memory only need to remember whether each current source is larger or smaller.

Quantitative evaluation is a future work. It is particularly important to consider the target max INL quantitatively. There is no specific target max INL in this study. The priority in the proposed method is simplicity of circuit design. At the cost of this, the INL is worse than "Rearrange". However, we consider that INL become sufficiently small compared to before calibration, so that the DAC yields become improved.

The actual time of comparisons is also important but has not yet been measured. The VCOs will be implemented or simulated to measure the time.

We also consider the unit current cell method in a digital manner. These techniques are suitable to digital-oriented advanced CMOS circuit implementation.

Finally, we close this paper by remarking that recently much attention is being paid to Physical Unclonable Function(PUF) technology for secure ICs [6] and the current cell value order information here can be also utilized for PUF.

Acknowledgements

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