# Optimization of Segmented DAC Linearity Improvement Algorithm Using Unit Cell Sorting with Digital Method

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Digital-to-Analog Converter (DAC) is a key component for modern transmitter circuits, and there its high linearity is required. For its nano-CMOS implementation, the device mismatch is large and hence the analog circuit characteristics may be deteriorated. However, there, digital circuit can be implemented with small chip area and hence so-called the digitally-assisted analog technology is attractive. This paper investigates the DAC linearity improvement algorithm and circuit; the DAC under investigation employs the current-steering segmented architecture for high-speed and low glitch applications as shown in Fig. 1. We mainly examine the switching sequence post adjustment (SSPA) algorithm [1] using simulation in details, and its digital-oriented implementation without an analog current comparator. The concept of SSPA is shown in Fig. 2. We have found that the SSPA algorithm can be more effective in large mismatch cases [2]. However, when there are $N=2^n$ current sources, SSPA takes long time because "combine, sort, and rearrange" must be performed $n$ times. This study is based on the idea that SSPA can be stopped midway and the number of rearrangements optimized. 127 current sources (about $2^7$) were simulated. One of the results is shown in Fig. 3. DNLpp does not change the result after 1 time. INLpp temporarily increases at 1time, but the result does not change after 2 times. Therefore, rearrangement can be stopped after 2 times.

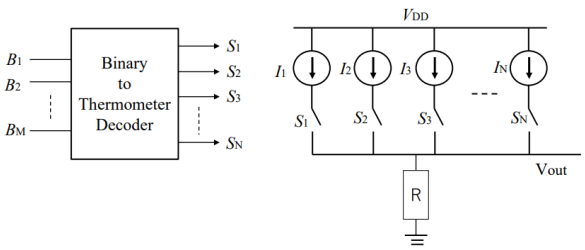


Fig 1. Segmented current-steering DAC configuration.

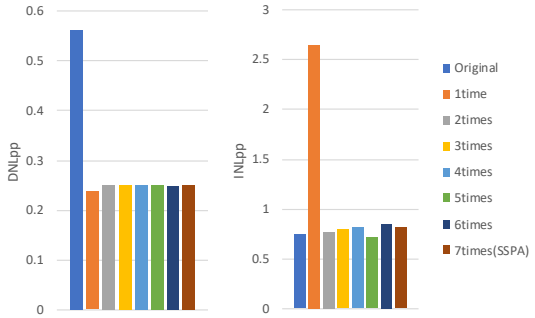


Fig 3. DNL and INL reduction.

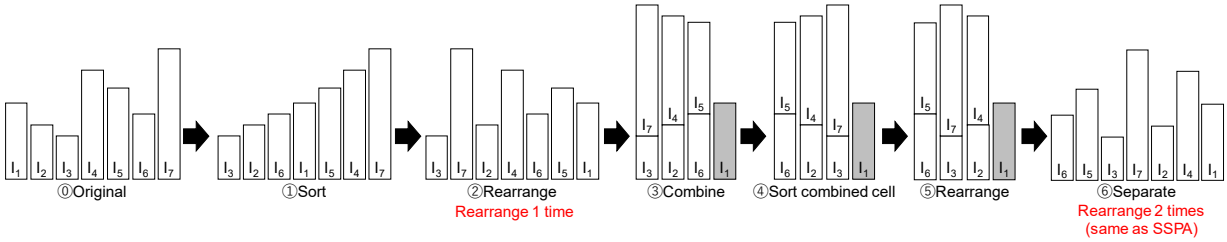


Fig 2. Explanation of the switching sequence post adjustment algorithm.

## References

[1] T. Chen, et.al., "A 14-bit 200-MHz Current-Steering DAC with Switching Sequence Post-Adjustment Calibration", IEEE Asian Solid-State Circuits Conference, Hangzhou, China (Nov. 2006).

[2] Y. Liu, et. al., "Segmented DAC Linearity Improvement Algorithm Using Unit Cell Sorting with Digital Method", ICTSS 2021, Kiryu, Japan (Dec. 2021).