

Low Switching Loss Dual RESURF 40V N-LDMOS with Grounded Field Plate for DC-DC Converters

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Research Objective and Background

Research Objective

Development of LDMOS structure for DC-DC converters handling 40V in automotive applications

LDMOS: Lateral Double Diffused MOS

Research Background

DC-DC Converter for Automotive Application

- High efficiency
- High frequency
- High reliability

Requirements for its Switching Device

- Low specific on-resistance
- Low switching loss
- High hot carrier endurance
- Wide SOA

SOA: Safe Operating Area



Our Approach

LDMOS for 40V switching device

- Mature CMOS process usage
- One-chip integration with other circuits

Based on our Previous Proposed LDMOS

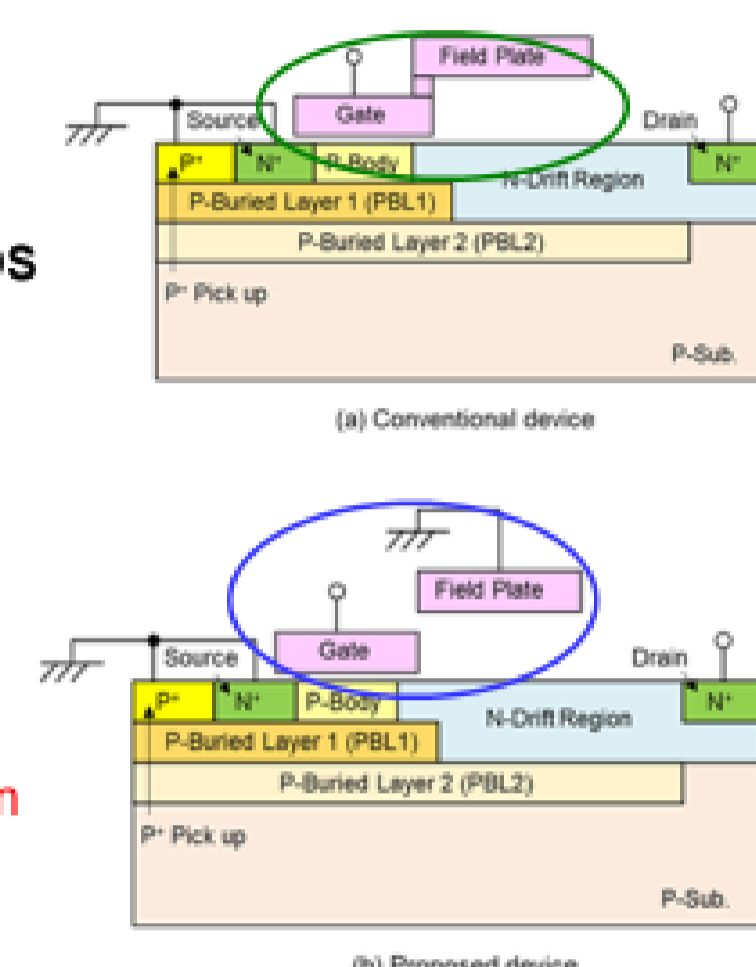
- Dual RESURF structure
- Field plate connected to gate

New Proposal

- Dual RESURF structure
- Field plate connected to ground → Miller capacitance reduction

Investigation of its optimal size and location

TCAD Simulation Verification

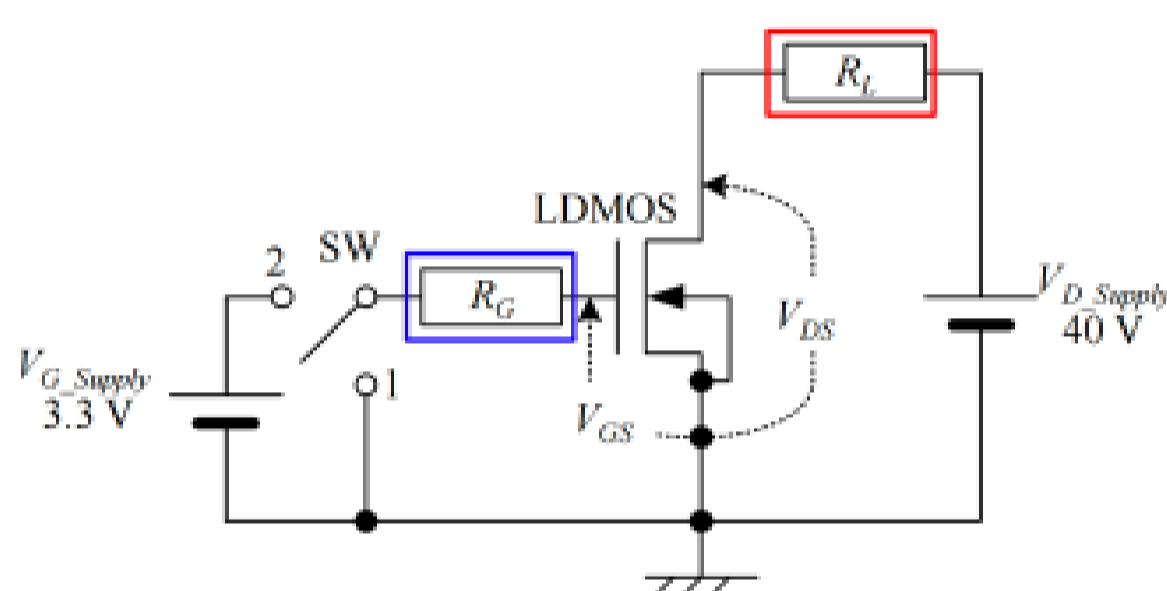


Proposed LDMOS Structure and Operation

Proposed LDMOS Structure and Feature

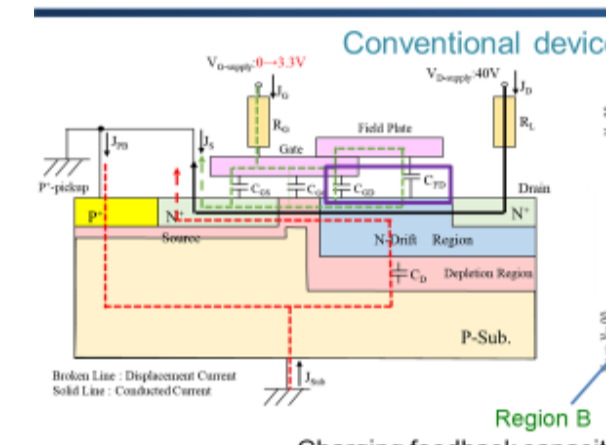
- Length of drift region L_D : 2650 nm
- Field plate L_{FP} (standard $L_{FP, std}$): 1625 nm
- Thickness of oxide interlayer between field plate and drift region T_{OX1} (standard $T_{OX1, std}$): 308 nm
- Oxide interlayer between field plate and the gate T_{OX2} (standard $T_{OX2, std}$): 100 nm
- Breakdown voltage between drain and source BV_{DS} : 61 V

Simulation Circuit as Switching Device



- Specific on-resistance: 40.8 mΩmm²
- Load resistance R_L : 5.33Ωmm²
- Gate resistance R_G : 1.07Ωmm²
- Extrapolated threshold voltage: 1.05V

Turn-On Simulation Results (Region B)

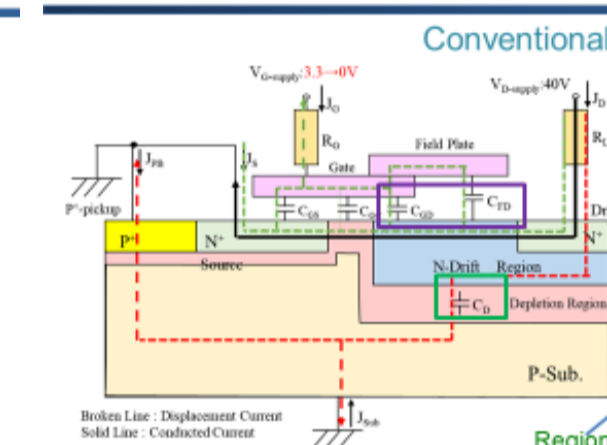


Charging feedback capacitance ($C_{CG} + C_{CP}$)

In gate plateau state (Long, intense Miller effect)

Discharging output capacitance (C_O)

Turn-Off Simulation Results (Region B)

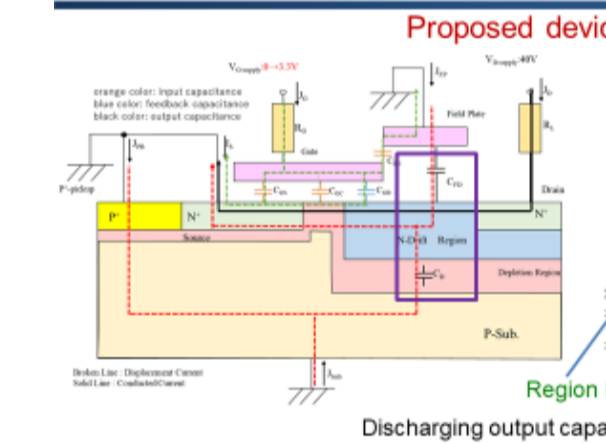


Charging output capacitance (C_O)

In gate plateau state (Long, intense Miller effect)

Discharging output capacitance ($C_{CG} + C_{CP}$)

Turn-On Simulation Results (Region B)

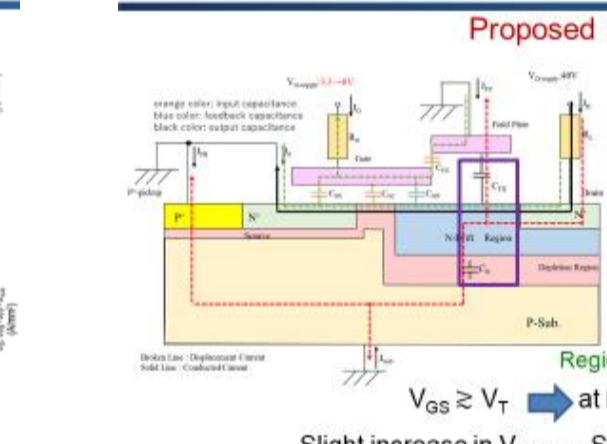


Discharging output capacitance ($C_{CG} + C_{CP}$)

Increase in displacement current ($J_{FP} + J_{FP} + J_{DB}$)

Gradual decrease in $V_{DS, int}$ (Weak Miller effect)

Turn-Off Simulation Results (Region B)



$V_{GS} \approx V_T$ at beginning of turn-off

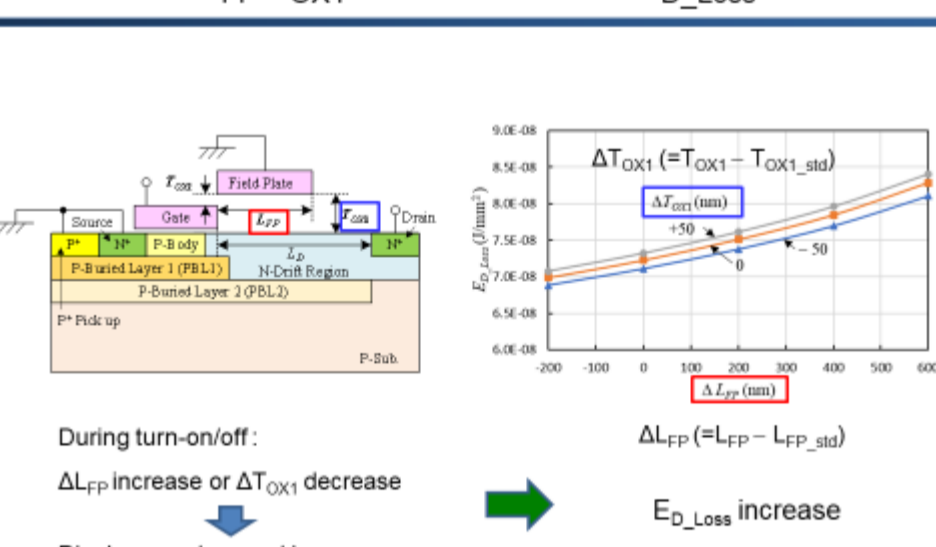
Slight increase in $V_{DS, int}$ Slight decrease in V_{DS}

Short, weak Miller effect (no gate plateau)

Charging output capacitance ($C_O + C_{CP}$)

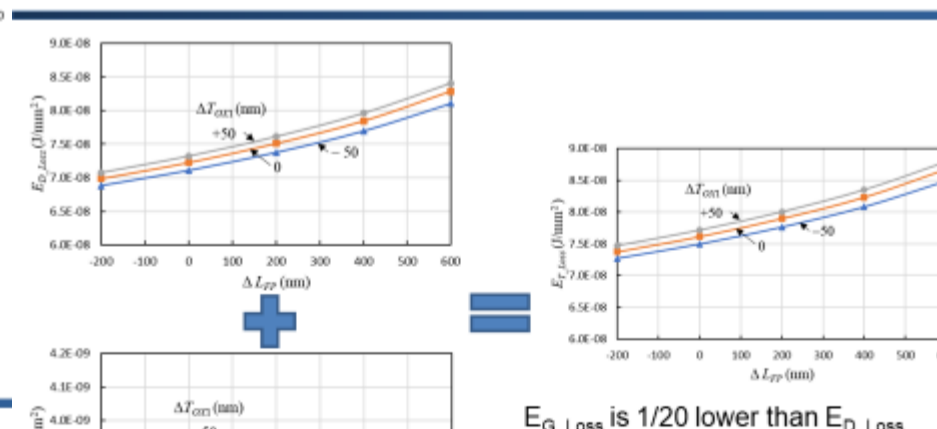
Optimization Simulation Results

L_{FP} T_{OX1} for Drain Loss $E_{D, Loss}$



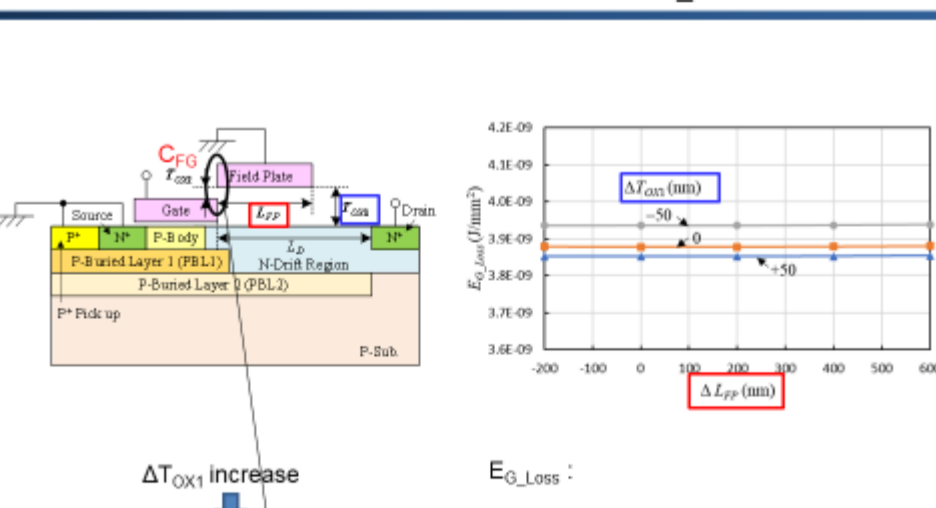
During turn-on/off: ΔL_{FP} increase or ΔT_{OX1} decrease → Displacement current increase → $E_{D, Loss}$ increase

L_{FP} T_{OX1} for Switching Loss



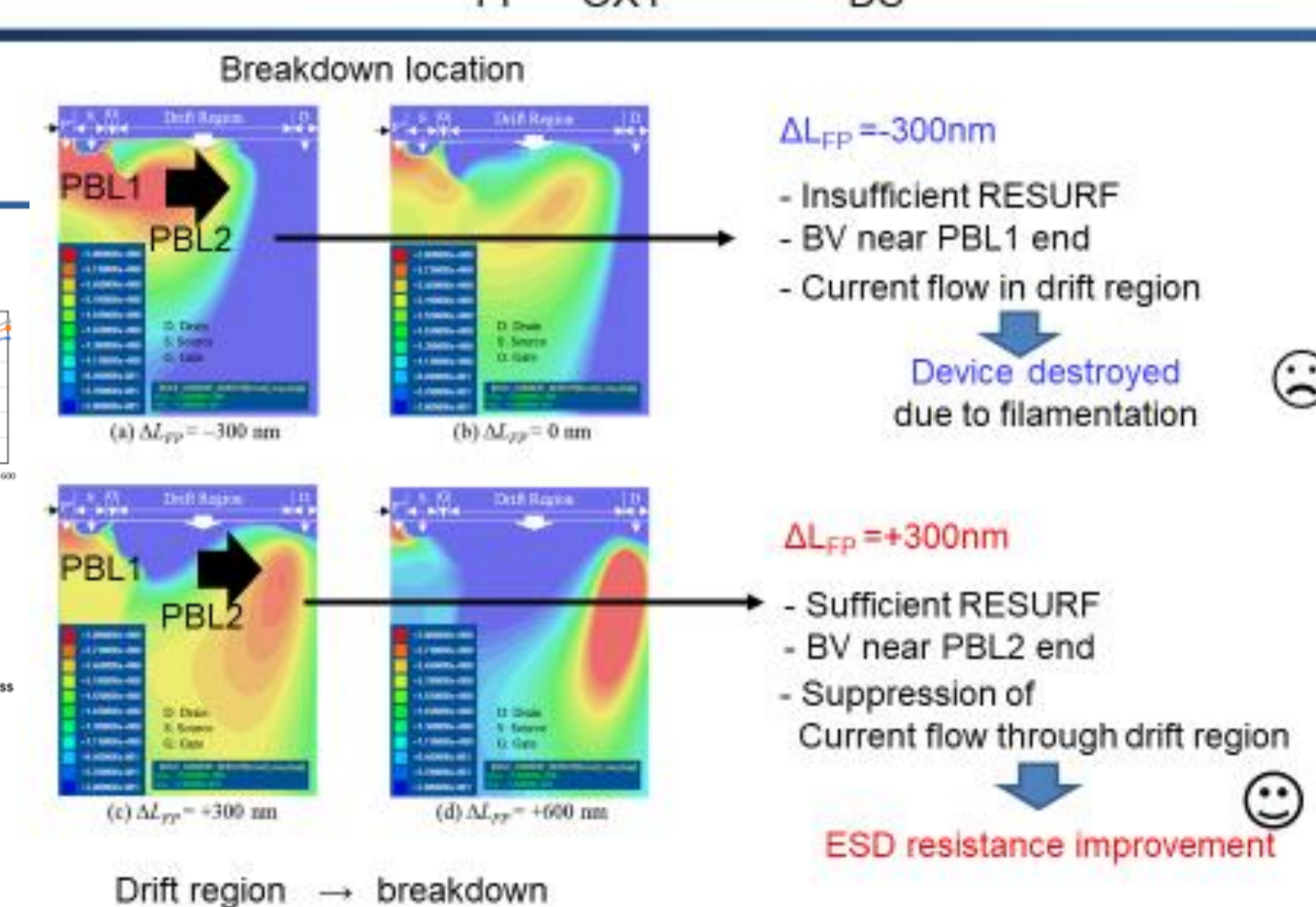
$E_{D, Loss}$ is 1/20 lower than $E_{D, Loss}$ → $E_{T, Loss} \approx E_{D, Loss} * E_{D, Loss}$ → Increase for ΔL_{FP} → Increase $E_{T, Loss}$

L_{FP} T_{OX1} for Gate Loss $E_{G, Loss}$

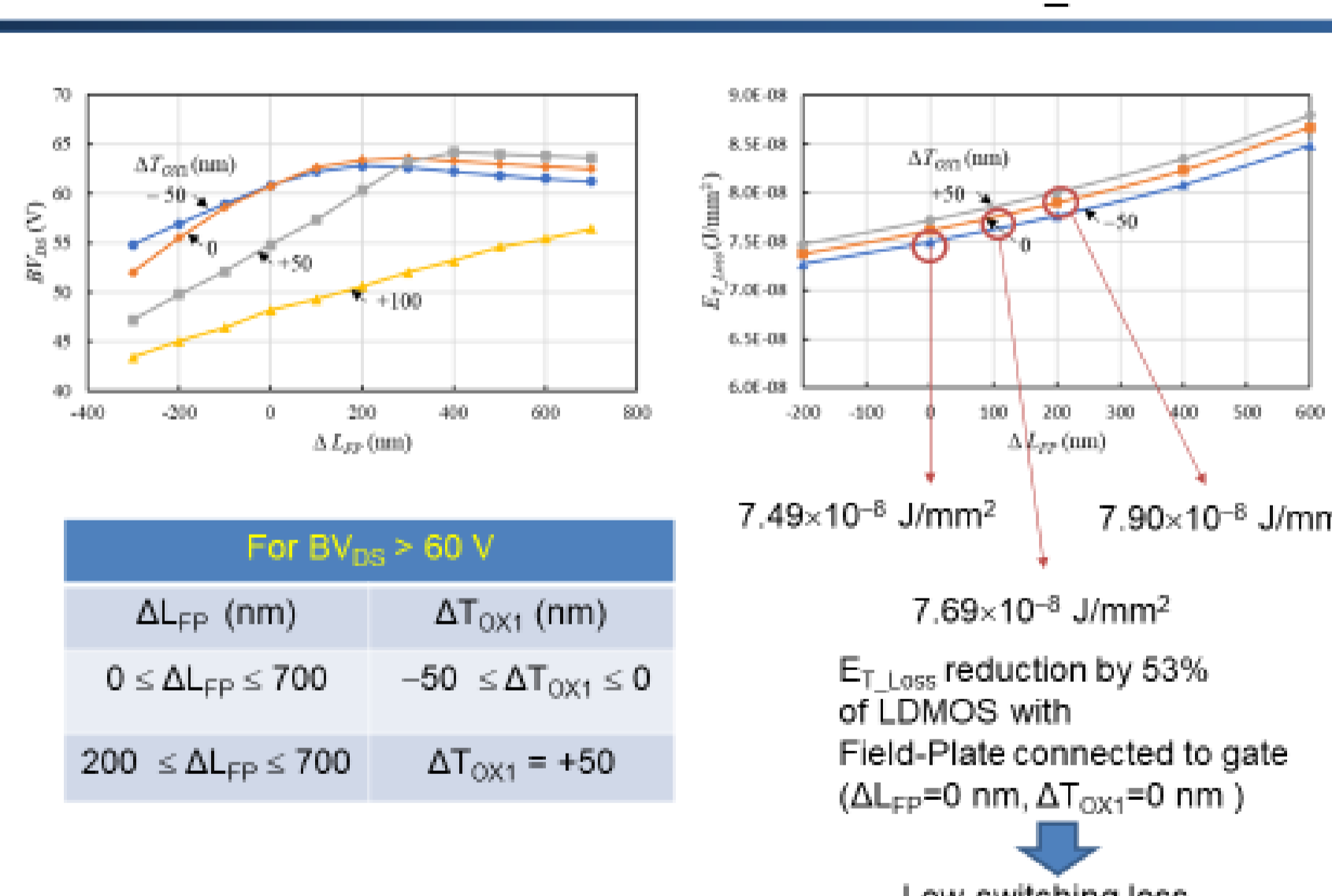


ΔT_{OX1} increase → Input capacitance C_{in} decrease → $E_{G, Loss}$ decrease → Increase for ΔT_{OX1} decrease

L_{FP} T_{OX1} for BV_{DS}

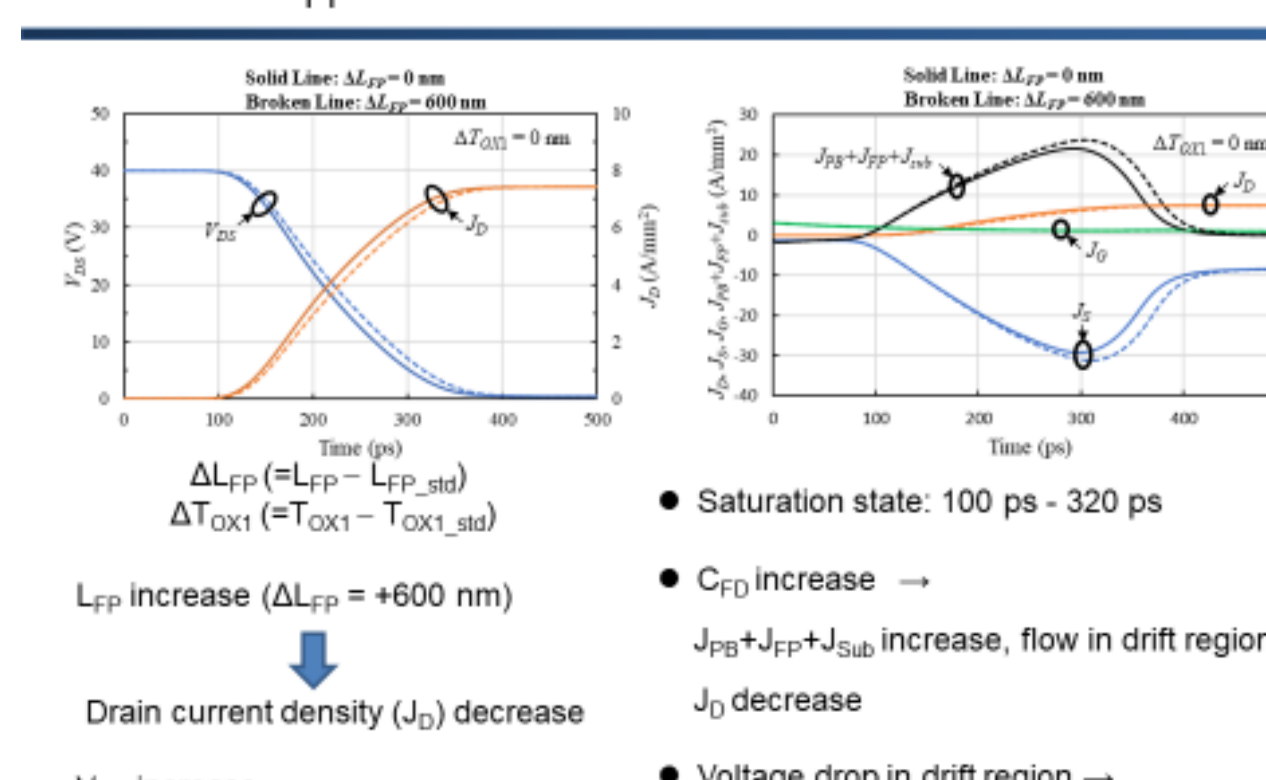


L_{FP} , T_{OX1} for Switching Loss $E_{T, Loss}$



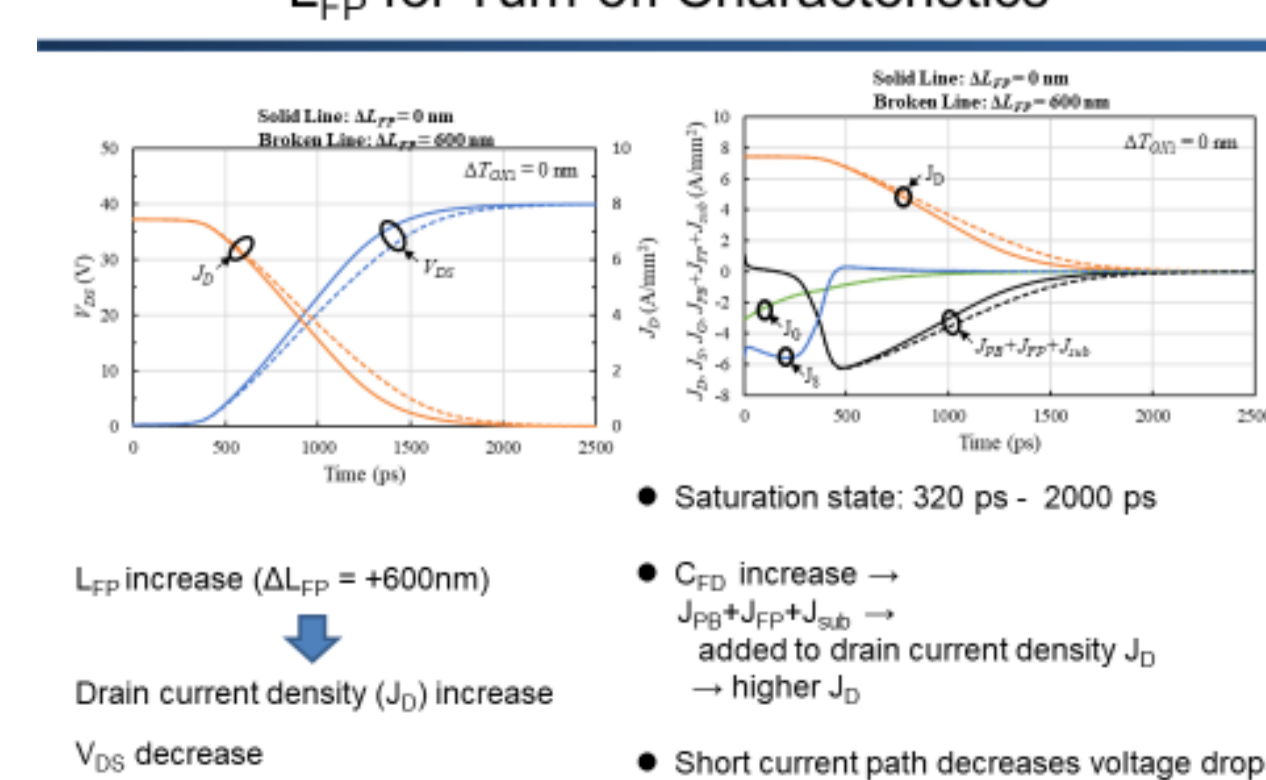
Discussion & Conclusion

L_{FP} for Turn-on Characteristics



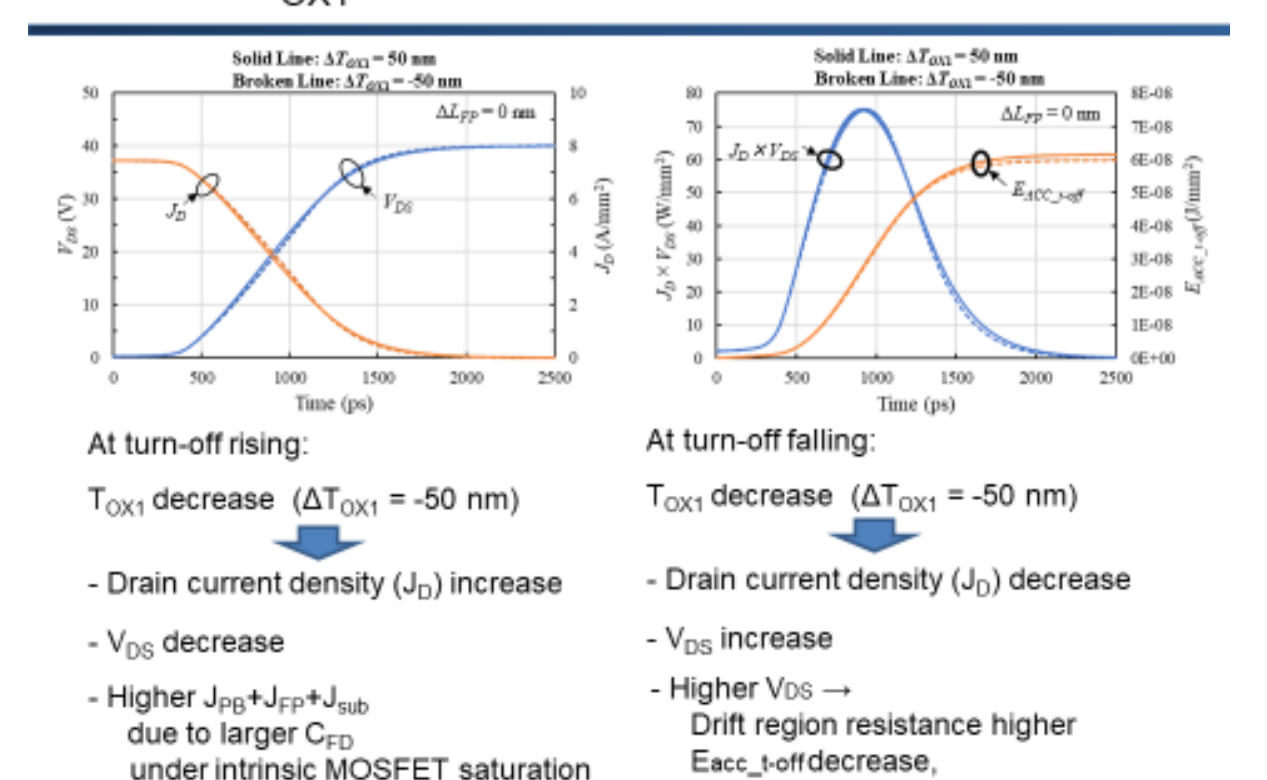
- Saturation state: 100 ps - 320 ps
- C_{FP} increase → $J_{FP} + J_{FP} + J_{DB}$ increase, flow in drift region J_D decrease
- Voltage drop in drift region → Higher V_{DS}

L_{FP} for Turn-off Characteristics



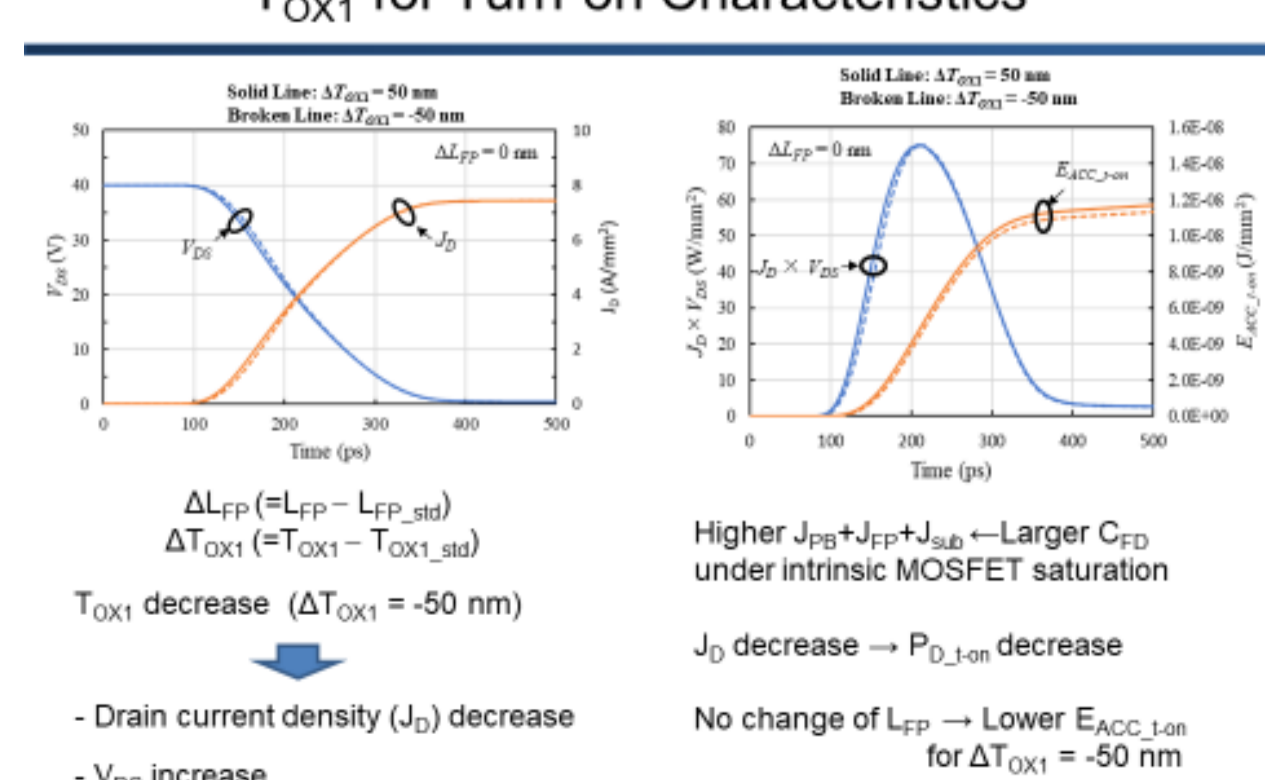
- Saturation state: 320 ps - 2000 ps
- C_{FP} increase → $J_{FP} + J_{FP} + J_{DB}$ added to drain current density J_D → higher J_D
- Short current path decreases voltage drop in drift region → lower V_{DS}

T_{OX1} for Turn-off Characteristics



- At turn-off rising: T_{OX1} decrease ($\Delta T_{OX1} = -50$ nm) → Drain current density (J_D) increase → V_{DS} decrease → Higher $J_{DB} + J_{FP} + J_{DB}$ due to larger C_{FP} under intrinsic MOSFET saturation
- At turn-off falling: T_{OX1} decrease ($\Delta T_{OX1} = -50$ nm) → Drain current density (J_D) decrease → V_{DS} increase → Drift region resistance higher $E_{acc, off}$ decrease, Turn-off loss increase with T_{OX1} increase

T_{OX1} for Turn-on Characteristics



- Higher $J_{DB} + J_{FP} + J_{DB}$ → Larger C_{FP} under intrinsic MOSFET saturation
- J_D decrease → $P_{D, int}$ decrease
- No change of L_{FP} → Lower $E_{DCC, Loss}$ for $\Delta T_{OX1} = -50$ nm

- Its size, location optimization of ΔL_{FP} , ΔT_{OX1}
 - Field Plate connected to ground
 - Verified with TCAD simulation
 - Switching loss reduction by 50 %
 - High ESD endurance
- For $0 \text{ nm} \leq \Delta L_{FP} \leq 200 \text{ nm}$, $-50 \text{ nm} \leq \Delta T_{OX1} \leq 0 \text{ nm}$

H.Y. Du, J. Matsuda, A. Kuwana, and H. Kobayashi, "Low Switching Loss Dual RESURF 40 V N-LDMOS with Ground Field Plate for DC-DC Converters," in MWSCAS, Fukuoka, Japan (Aug. 2022)