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15:45-16:15

Invited

Signal Generation Technologies for Analog/Mixed-Signal IC Testing

Haruo Kobayashi

Gunma University

koba@gunma-u.ac.jp

Outline

- Objective
- One-Tone and Two-Tone Signal Generation with AWG
- One-Tone Signal Generation from Digital Clock
- One-Tone Signal Generation with Digital ATE
- Multi-Tone Signal Generation Algorithm
- Wideband Signal Generation
- ΔΣ DAC Limit Cycle Suppression
- Clock Jitter Reduction
- Analog Filter
- Conclusion

AWG: Arbitrary Waveform Generator
ATE: Automatic Test Equipment

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Objective of This Paper

- To introduce research achievements of
  - Author's group
  - Signal generation technologies for analog/mixed-signal IC testing

- To see trend of test signal generation technologies

Research Background

Analog/mixed-signal circuits ⇨ Troublesome

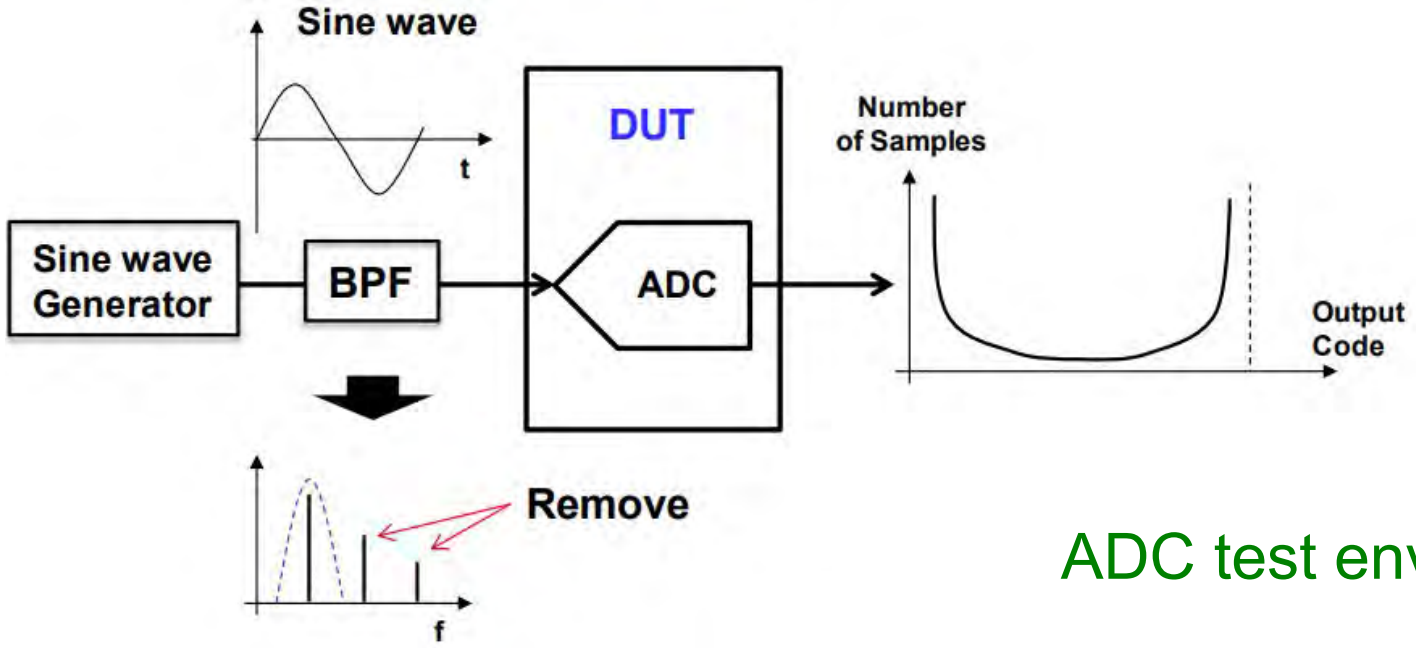
⇩

Their high-quality, low-cost testing at mass production stage

⇩

High quality, low cost signal generation is a key.

LSI test in factory



ADC test environment

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AWG: Arbitrary Waveform Generator

Arbitrary Waveform Generator (AWG)

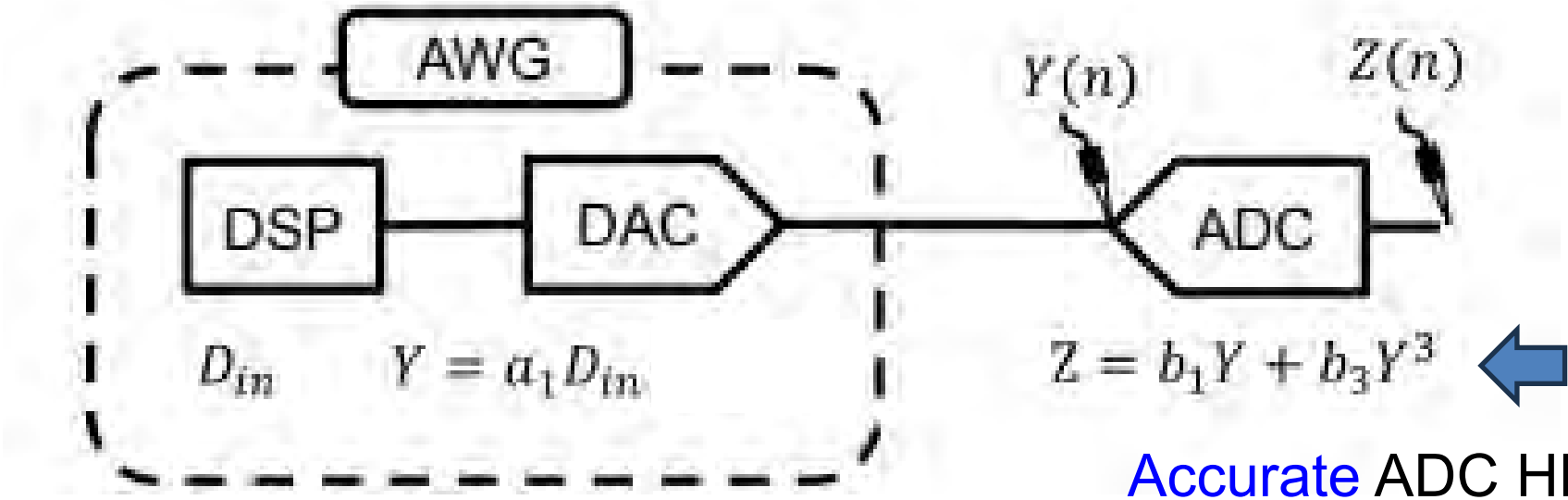
Ideal

HD3: 3rd-order Harmonic Distortion

DSP (or waveform memory) + DAC

Arbitrary waveform can be generated

➡ by changing DSP program

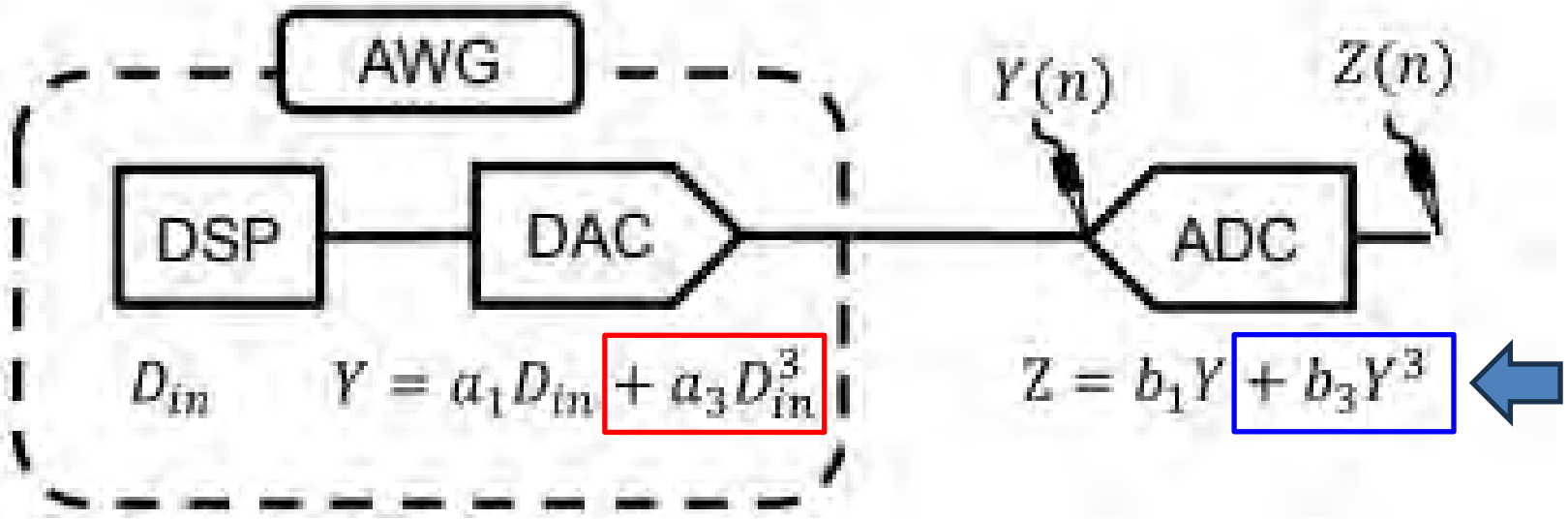


⬅ ADC HD3

Accurate ADC HD3 measurement

Arbitrary Waveform Generator (AWG)

Actual

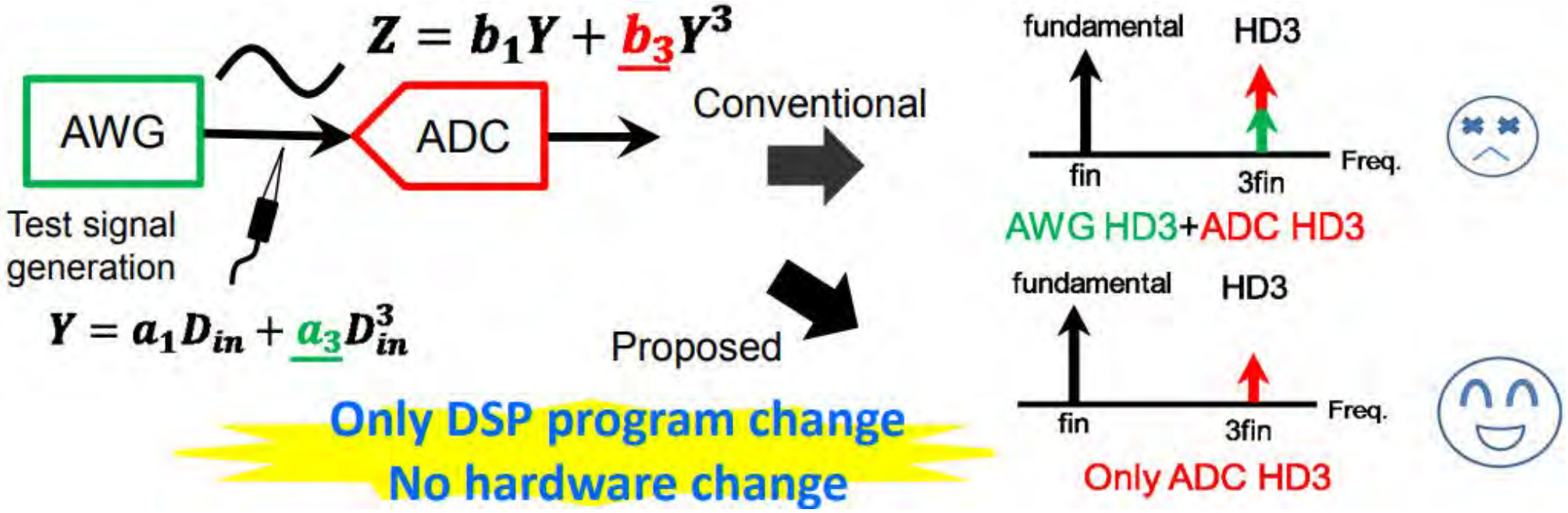


DAC HD3 + ADC HD3

NOT accurate ADC HD3 measurement

DAC nonlinearity ⇒ Limit AWG output signal quality

One-Tone Signal Generation: Phase Switching



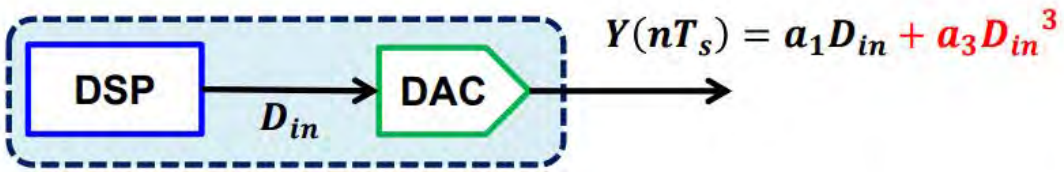
No requirement for DAC nonlinearity identification

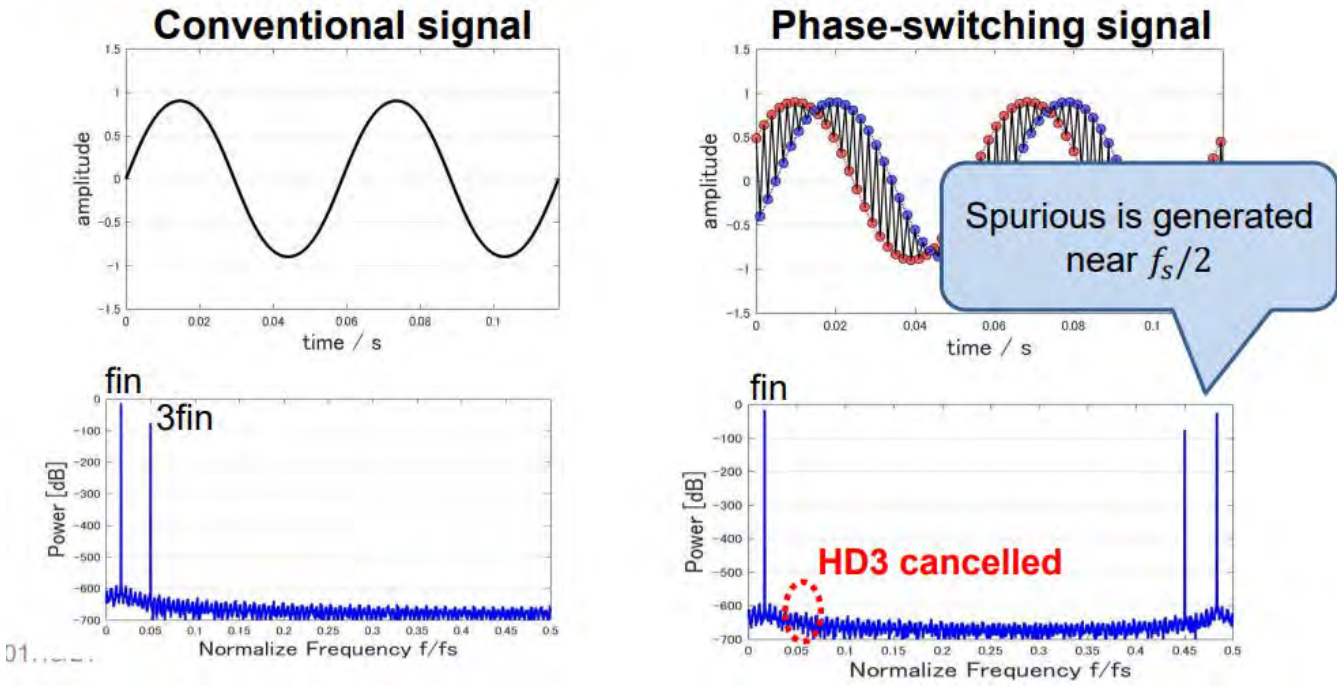
Low-cost, low-distortion sine signal generation

[1] “Low-Distortion Signal Generation for ADC Testing,” IEEE International Test Conference (Oct. 2014).

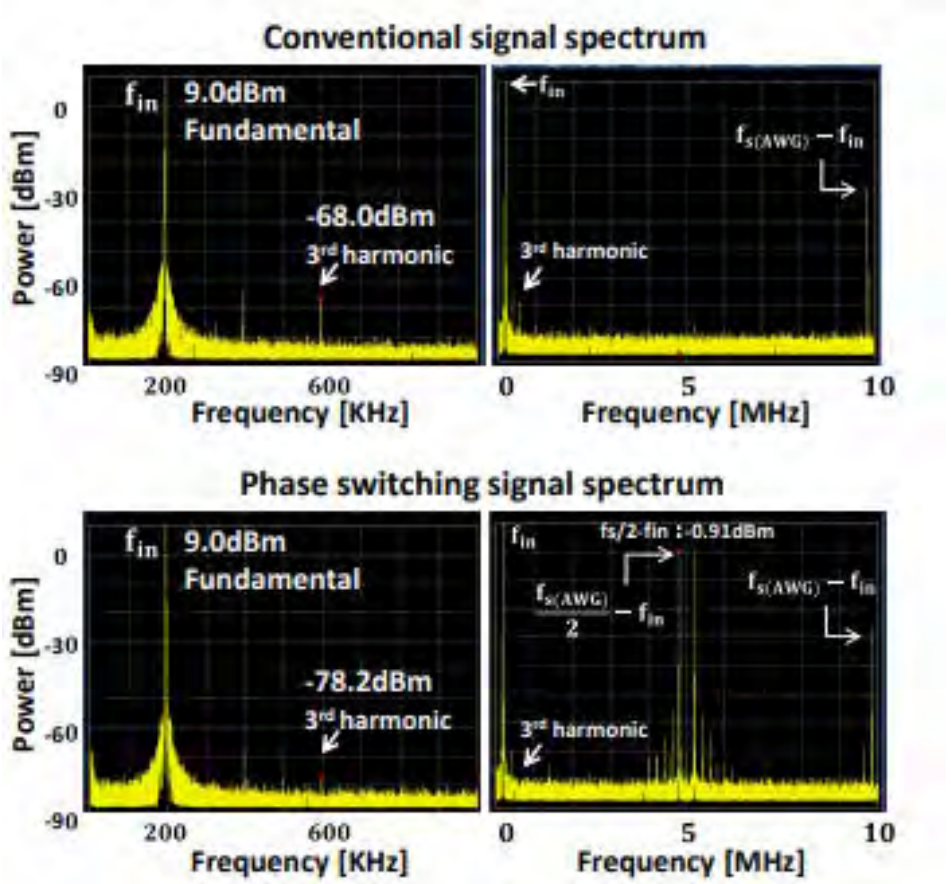
One-Tone: Phase Switching

$$D_{in} = \begin{cases} X_0 = A\sin(2\pi f_{in} n T_s + \pi/6) & n: \text{even} \\ X_1 = A\sin(2\pi f_{in} n T_s - \pi/6) & n: \text{odd} \end{cases}$$





Measurement Results



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AWG: Arbitrary Waveform Generator

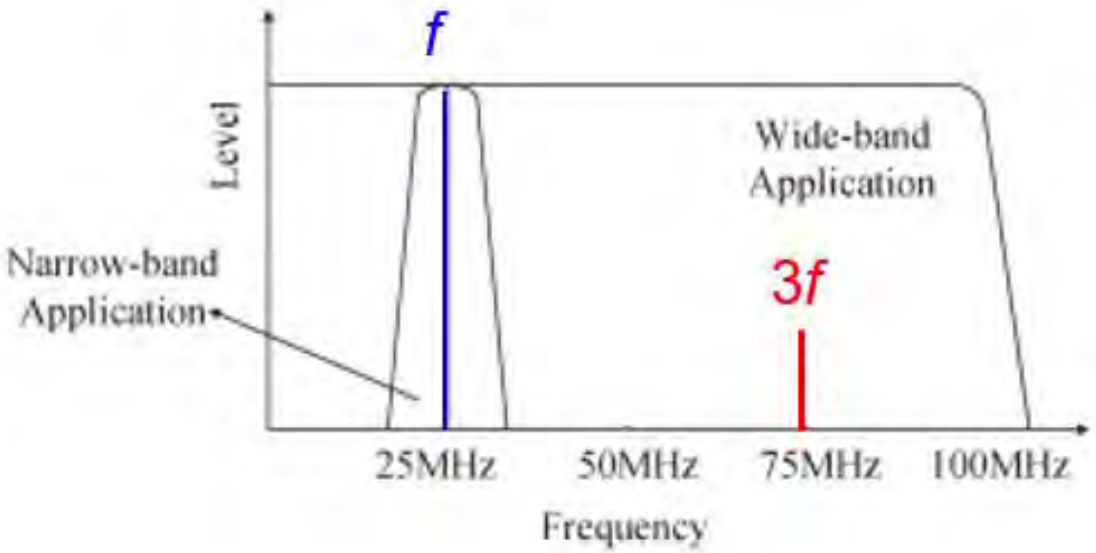
Why Two-Tone Testing ?

Linearity testing of narrow-band device with 3rd order-distortion

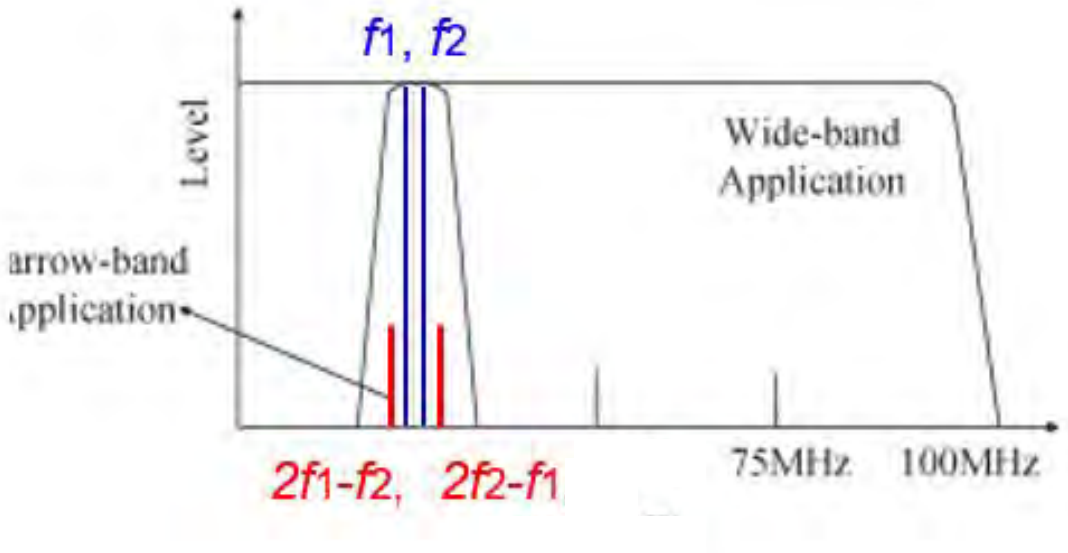
Communication applications

Single-tone: HD3 ➡ Out of band

Two-tone: IMD3 ➡ In-band



HD3: 3rd-order Harmonic Distortion



IMD3: 3rd-order Intermodulation Distortion

Two-Tone Signal: Phase Switching

AWG 3rd-order nonlinearity

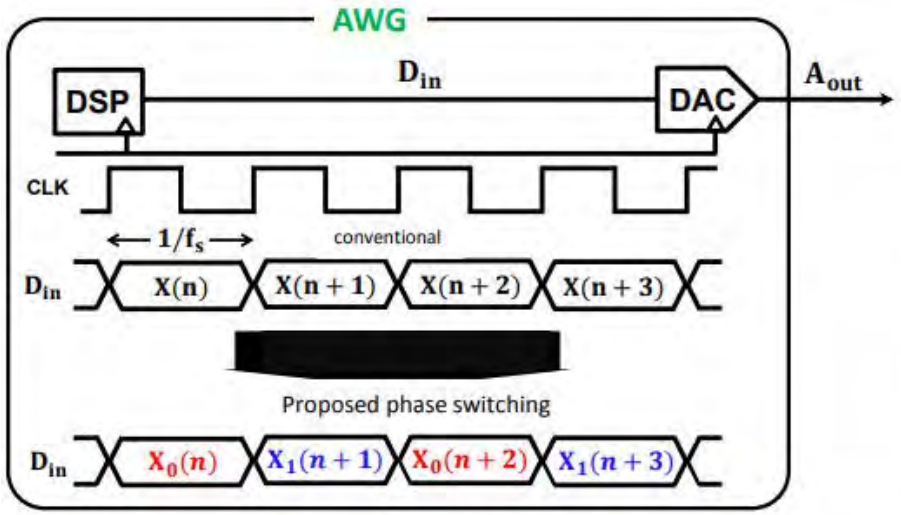
⇩

Two-tone signal with IMD3

⇩

Compensation by digital algorithm

Low IMD3 two-tone signal generation for communication application ICs



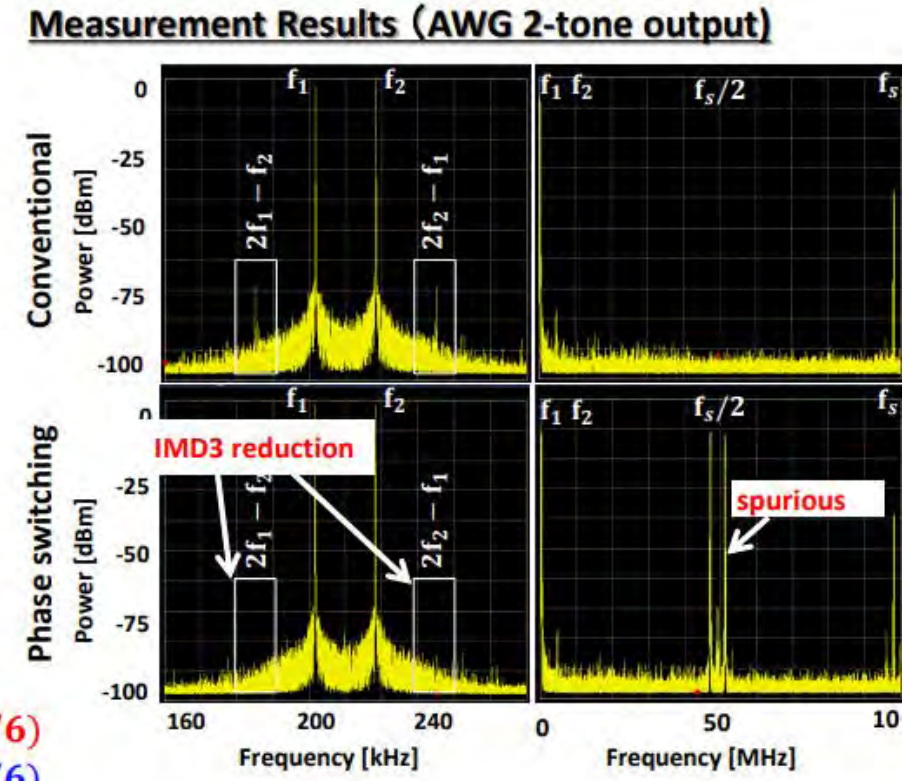
Conventional

$$X(n) = A\cos(2\pi f_1 nT_s) + A\cos(2\pi f_2 nT_s)$$

Proposed phase switching

n: even $\quad X_0(n) = B\cos(2\pi f_1 nT_s + \pi/6) + B\cos(2\pi f_2 nT_s - \pi/6)$

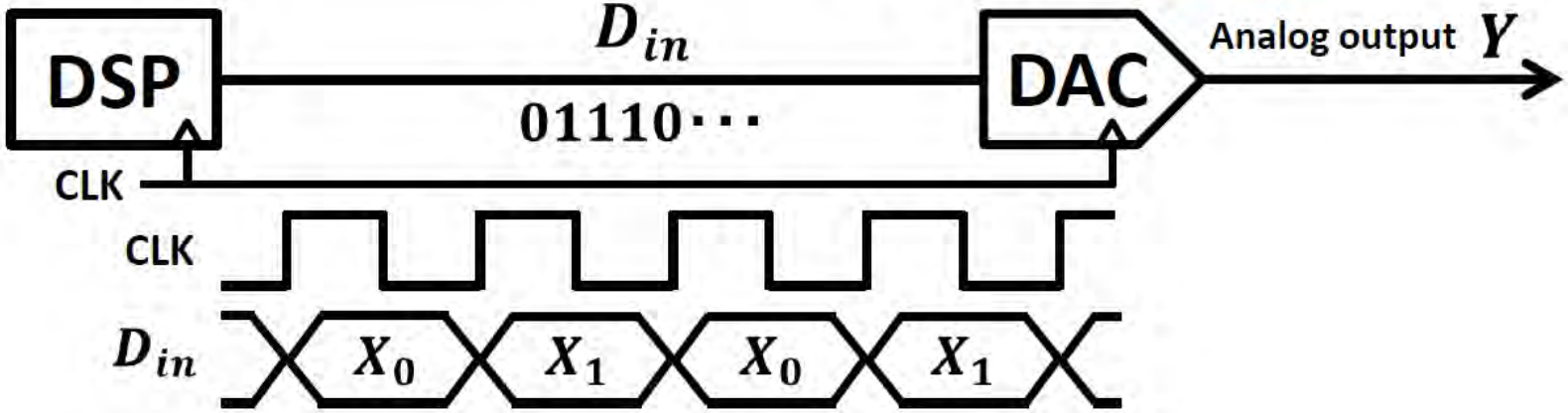
n: odd $\quad X_1(n) = B\cos(2\pi f_1 nT_s - \pi/6) + B\cos(2\pi f_2 nT_s + \pi/6)$



[2] "Two-Tone Signal Generation for Communication Application ADC Testing," IEEE Asian Test Symposium (Nov. 2012).

Two-Tone Signal: Frequency Switching

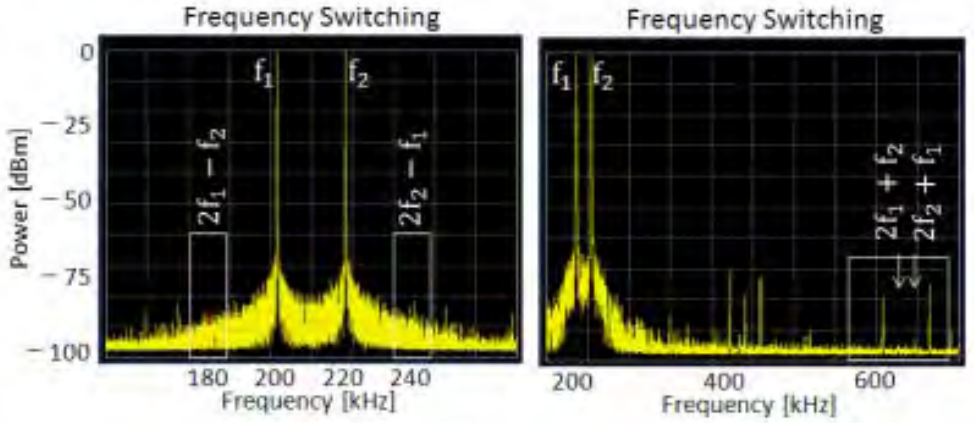
$$Y = a_1 D_{in} + a_3 D_{in}^{\,3}$$



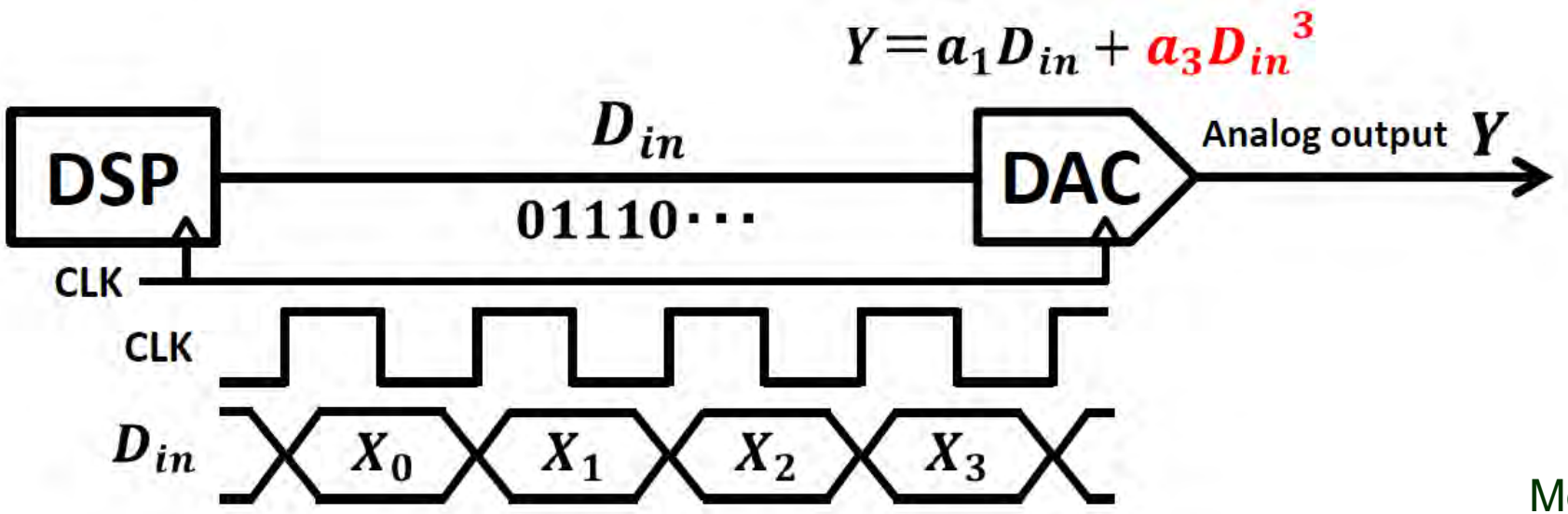
$$X_0 = 2A \cdot cos(2\pi f_1 (n-1) T_s)$$

$$X_1 = 2A \cdot cos(2\pi f_2 n T_s)$$

Measurement results



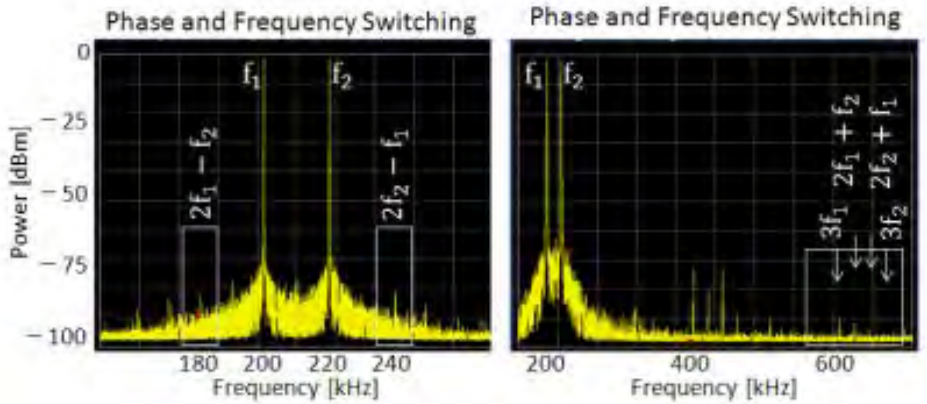
Two-Tone Signal: Phase Frequency Switching



4-time interleave

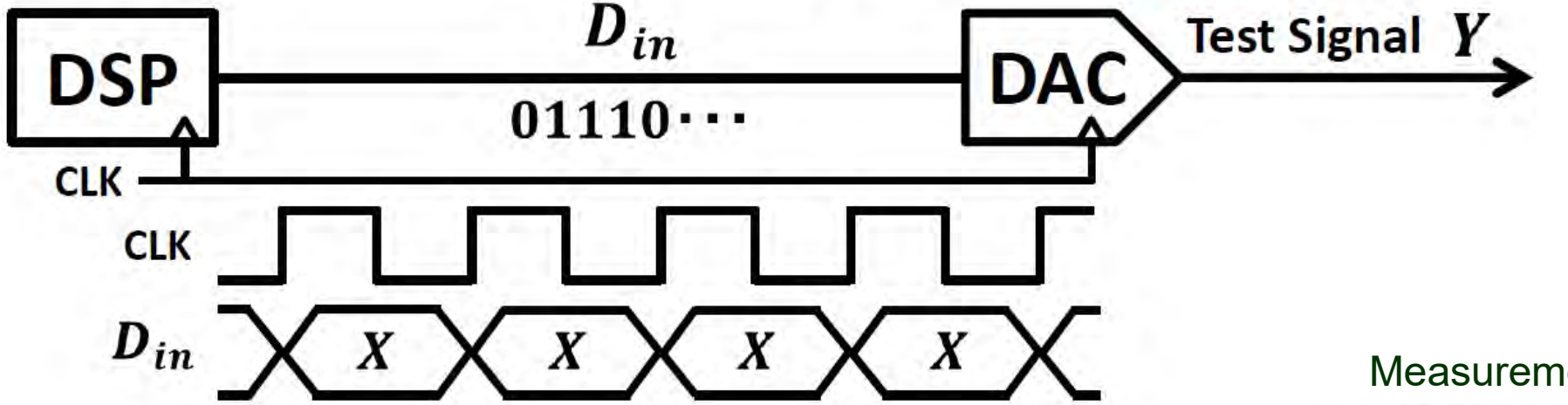
$$X_0 = A \cdot cos(2\pi f_1 (n-3) T_s)$$
$$X_1 = A \cdot cos(2\pi f_1 (n-2) T_s + \pi/3)$$
$$X_2 = A \cdot cos(2\pi f_2 (n-1) T_s)$$
$$X_3 = A \cdot cos(2\pi f_2 n T_s + \pi/3)$$

Measurement results



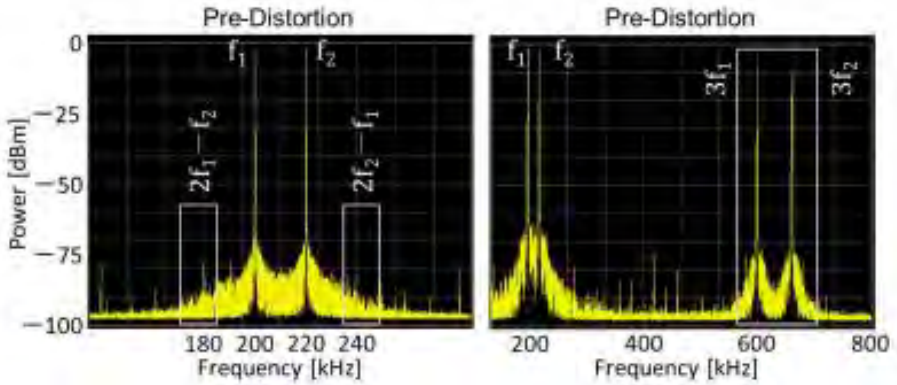
Two-Tone Signal: Pre-Distortion

$$Y = a_1 D_{in} + a_3 D_{in}^{\ 3}$$



Add HD3 components in Din.

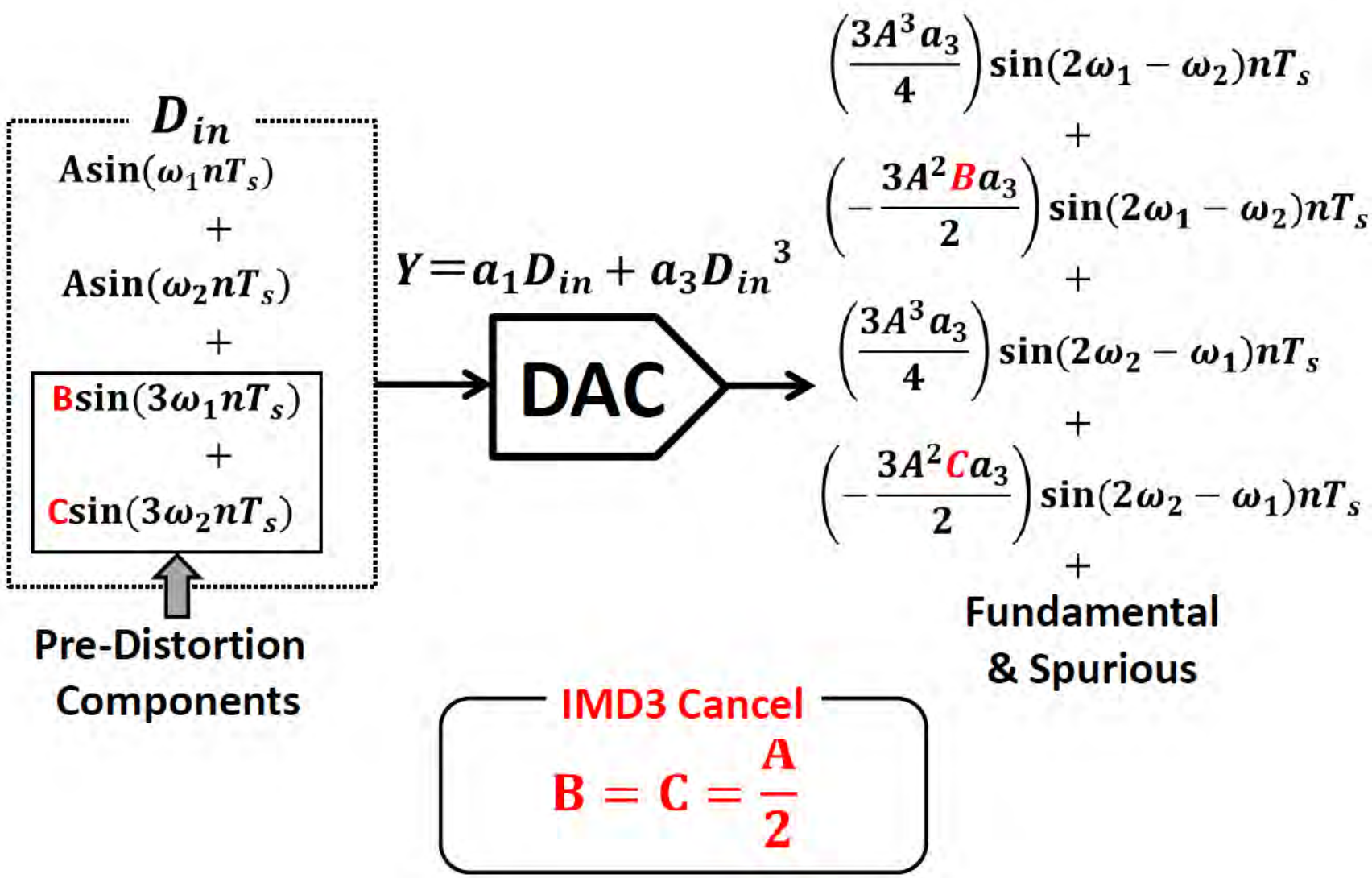
Measurement results



$$X = A \cdot cos(2\pi f_1 nT_s) + A \cdot cos(2\pi f_2 nT_s)$$

$$+ A/2 \cdot cos(2\pi (3f_1) nT_s) + A/2 \cdot cos(2\pi (3f_2) nT_s)$$

Two-Tone Signal: Pre-Distortion Principle

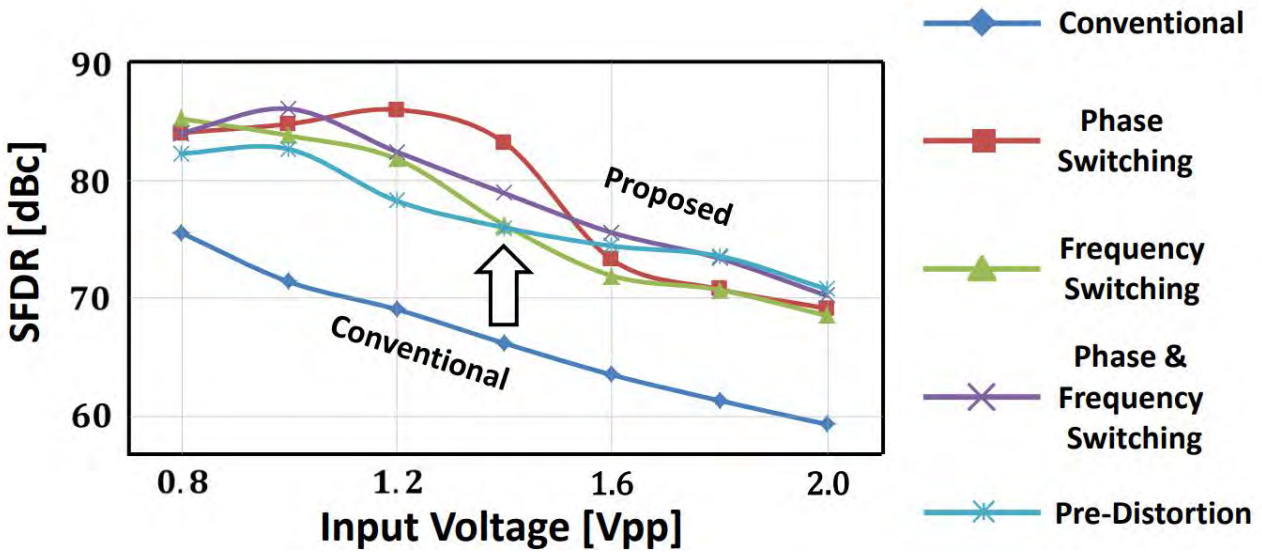


Proposed Four Methods Comparison

Power Spectrum Map

	Disappear	Appear
Conventional		$2f_1 - f_2$ $2f_2 - f_1$
Phase Switching	$2f_1 - f_2$ $2f_2 - f_1$ $3f_1$ $3f_2$	Around $f_s/2$
Frequency Switching	$2f_1 - f_2$ $2f_2 - f_1$ $2f_1 + f_2$ $2f_2 + f_1$	Around $f_s/2$
Phase & Freq. Switching	$2f_1 - f_2$ $2f_2 - f_1$ $2f_1 + f_2$ $2f_2 + f_1$ $3f_1$ $3f_2$	Around $f_s/2$ $f_s/4$
Pre-Distortion	$2f_1 - f_2$ $2f_2 - f_1$	$4f_1 - 3f_2$ $4f_2 - 3f_1$ Around $3f_1$ $5f_1$ $7f_1$ $9f_1$

Measurement Results



- Four methods are comparable.
- SFDR improvement by ~10 dB

SFDR: Spurious Free Dynamic Range

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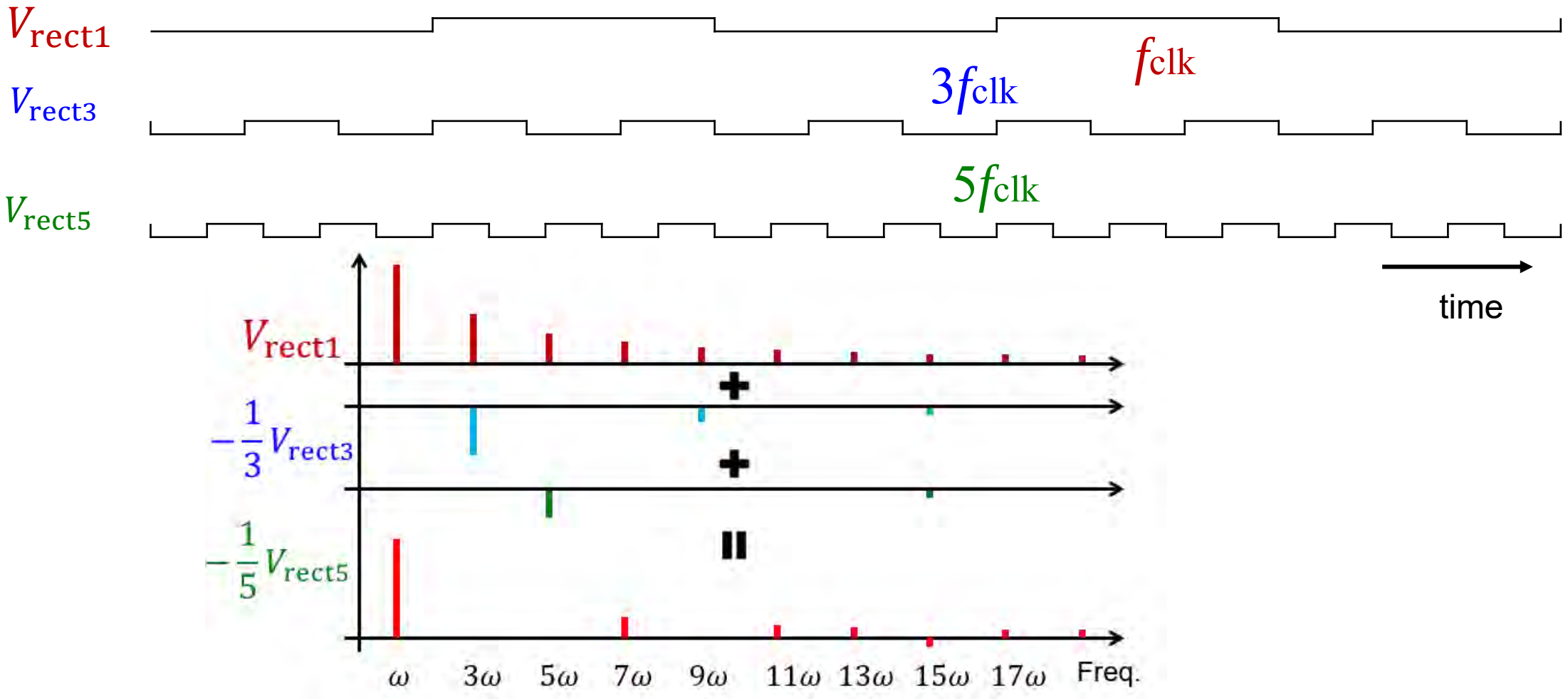
One-Tone Signal from Digital Clock

HD3, HD5 Cancellation Using Summing Multiple Square Waves



Fourier Series Analysis

- 100kHz Square Wave

$$V_{rect1}(t) = \sin(\omega t) + \frac{1}{3}\sin(3\omega t) + \frac{1}{5}\sin(5\omega t) + \frac{1}{7}\sin(7\omega t)\cdots$$

- 300kHz Square Wave

$$V_{rect2}(t) = \sin(3\omega t) + \frac{1}{3}\sin(9\omega t) + \frac{1}{5}\sin(15\omega t) + \frac{1}{7}\sin(21\omega t)\cdots$$

- 500kHz Square Wave

$$V_{rect3}(t) = \sin(5\omega t) + \frac{1}{3}\sin(15\omega t) + \frac{1}{5}\sin(25\omega t) + \frac{1}{7}\sin(35\omega t)\cdots$$

- Summing Multiple Square Waves

$$f(t) = V_{rect1}(t) - \frac{1}{3}V_{rect2}(t) - \frac{1}{5}V_{rect3}(t)$$

$$= \sin(\omega t) + \frac{1}{3}\sin(3\omega t) + \frac{1}{5}\sin(5\omega t) + \frac{1}{7}\sin(7\omega t)\cdots$$

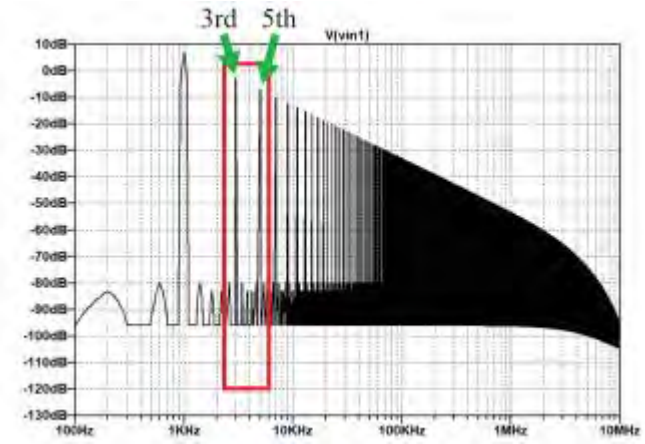
$$-\frac{1}{3}\left[\sin(3\omega t) + \frac{1}{3}\sin(9\omega t) + \frac{1}{5}\sin(15\omega t) + \frac{1}{7}\sin(21\omega t)\cdots\right]$$

$$-\frac{1}{5}\left[\sin(5\omega t) + \frac{1}{3}\sin(15\omega t) + \frac{1}{5}\sin(25\omega t) + \frac{1}{7}\sin(35\omega t)\cdots\right]$$

$$= \sin(\omega t) + \frac{1}{7}\sin(7\omega t) + \frac{1}{11}\sin(11\omega t) + \cdots$$

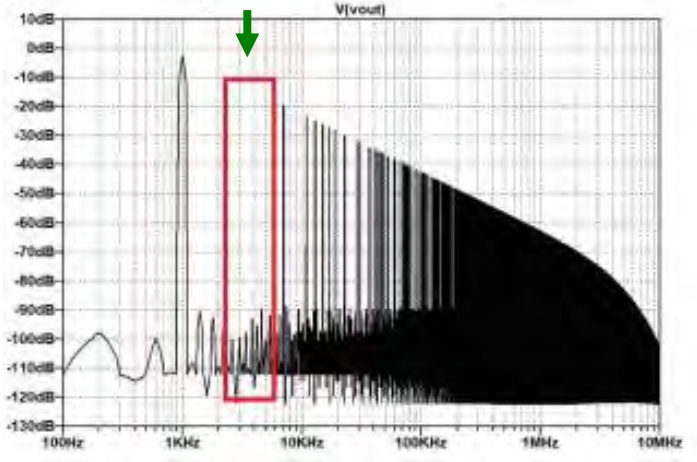
↑ $\sin(3\omega t)$ and $\sin(5\omega t)$ are cancelled

Simulated Power Spectrum



Rectangular V_{rect1}

HD3, HD5 cancellation

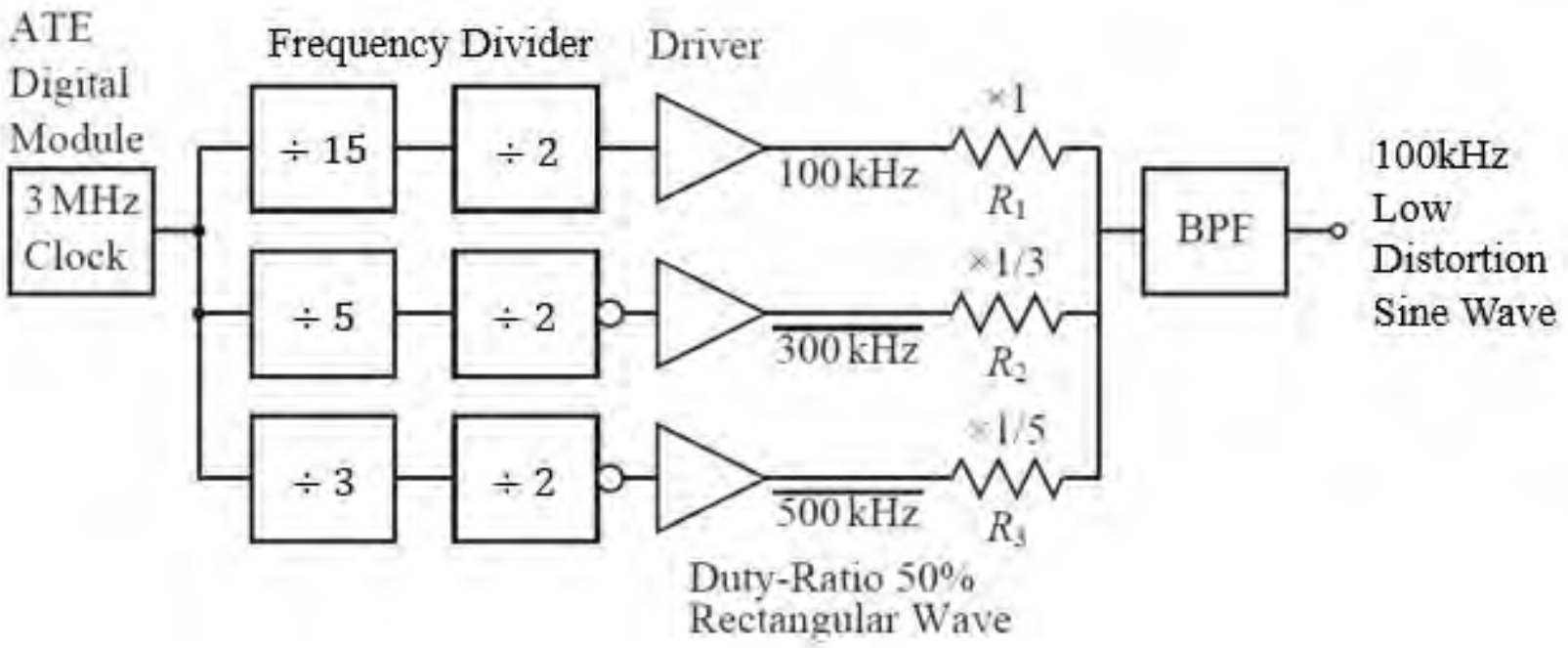


Summing of multiple

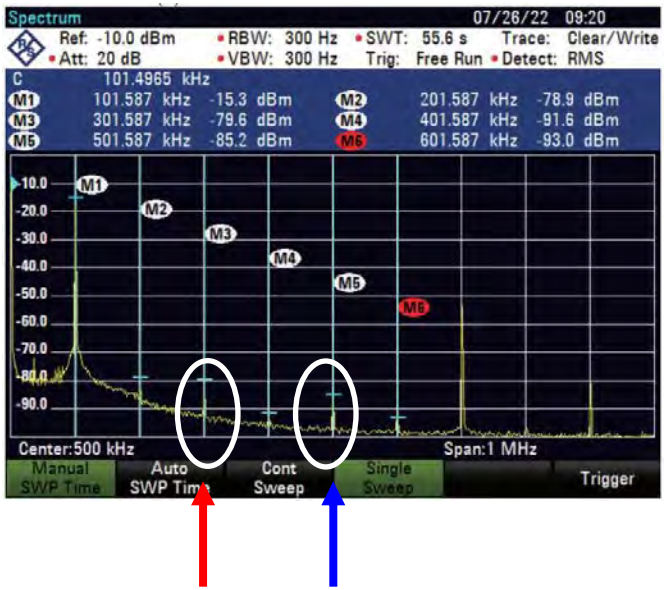
Circuit Implementation and Measurement

Implementation with very simple circuits

Low-cost, low-distortion sine wave signal generation



Measurement Results

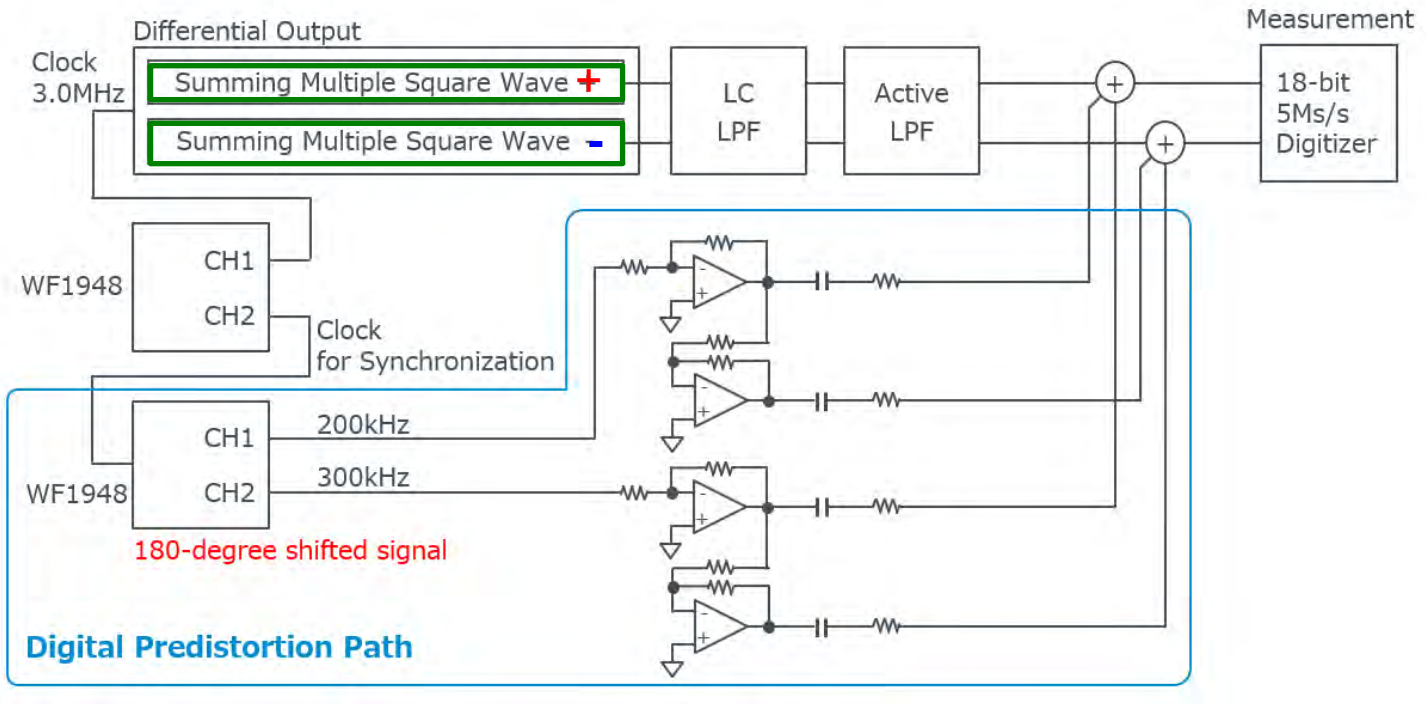


HD3 HD5
suppression

[3] "Low Distortion Sine Wave Generator with Simple Harmonics Cancellation Circuit and Filter for Analog Device Testing," IEICE Electronics Express (Jan. 2023)

Combination with Digital Predistortion

(i) Measure HD2, HD3
(ii) Add their 180-degree shifted signals by function generators



➡ Low-distortion signal generation for 16-bit ADC test

[4] "Low Distortion Sinusoidal Signal Generator with Harmonics Cancellation Using Two Types of Digital Predistortion", IEEE International Test Conference (Oct. 2023)

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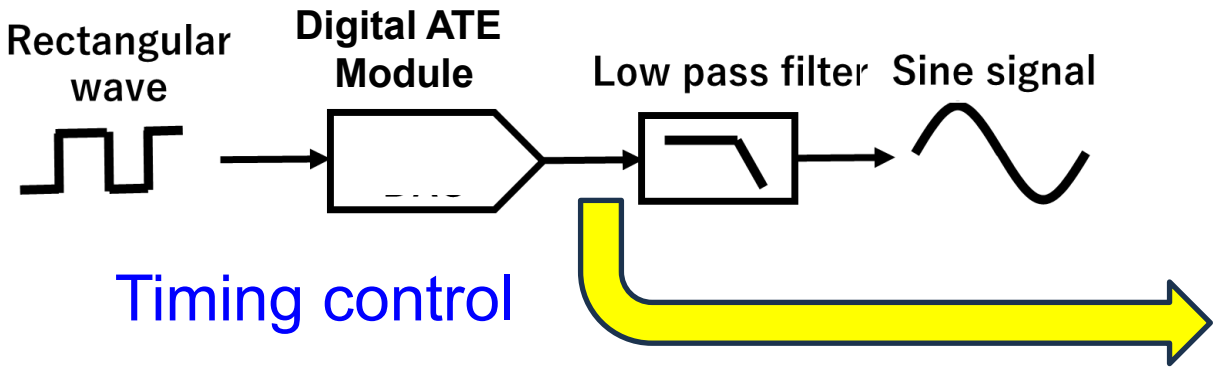
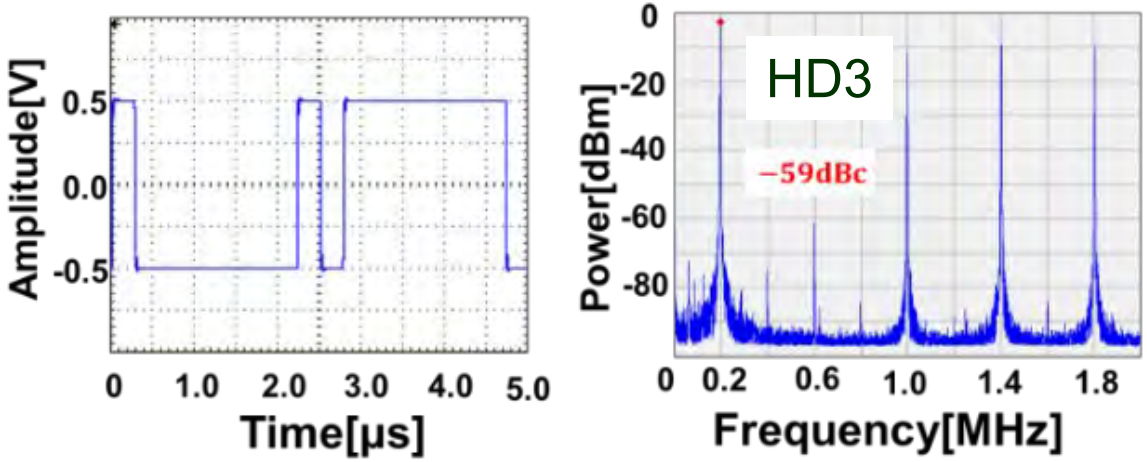
ATE: Automatic Test Equipment

One-Tone Signal from Digital ATE Module

Proposed sine signal generation



HD3 suppression



Digital ATE: Inexpensive

Mixed-Signal ATE: Expensive

[5] "Low-Distortion Signal Generation for Analog/Mixed-Signal Circuit Testing Using Digital ATE," IEEE International Test Conference in Asia (Sept. 2017).

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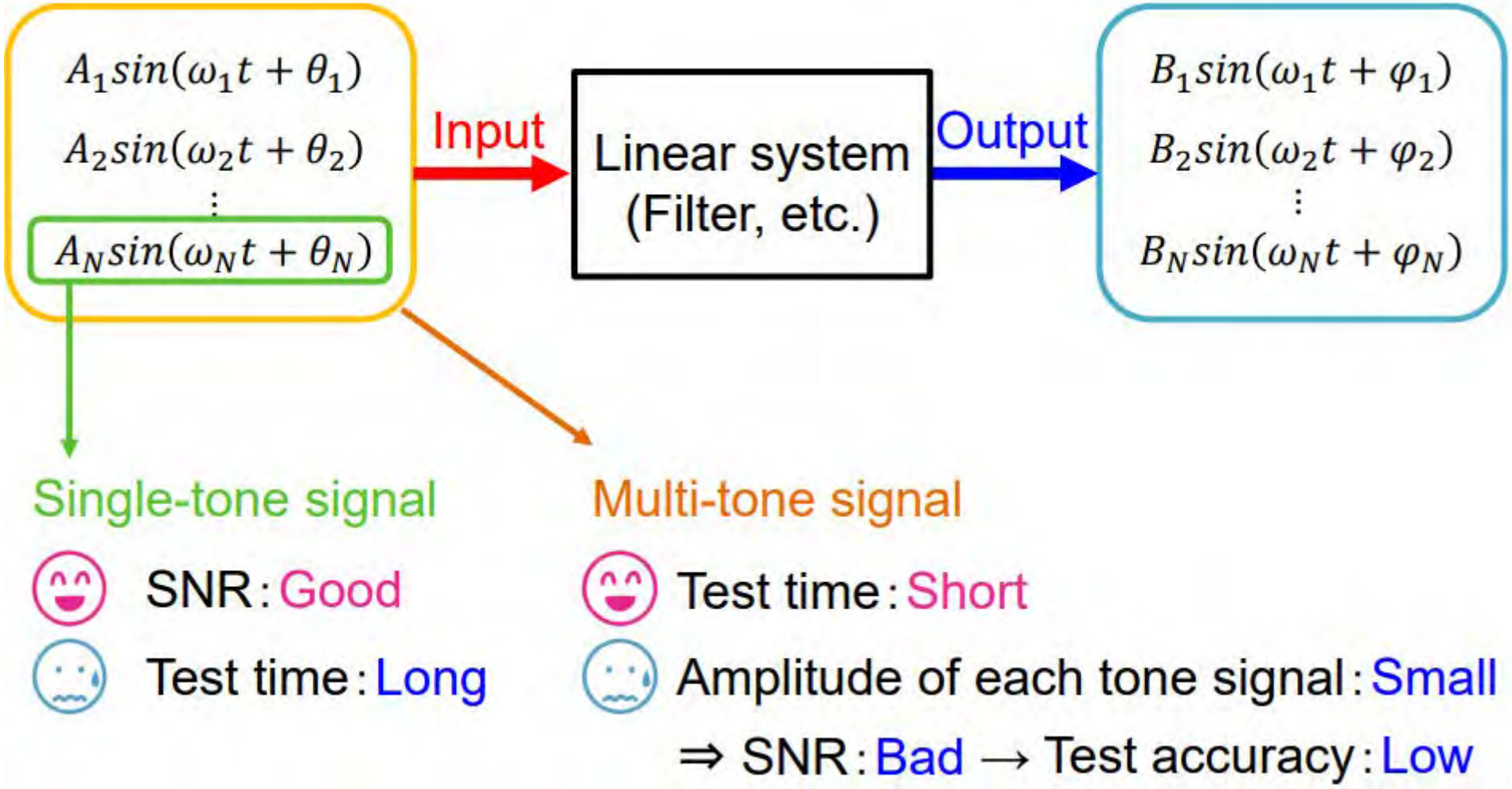
Use of Multi-Tone Signal for Analog IC Test

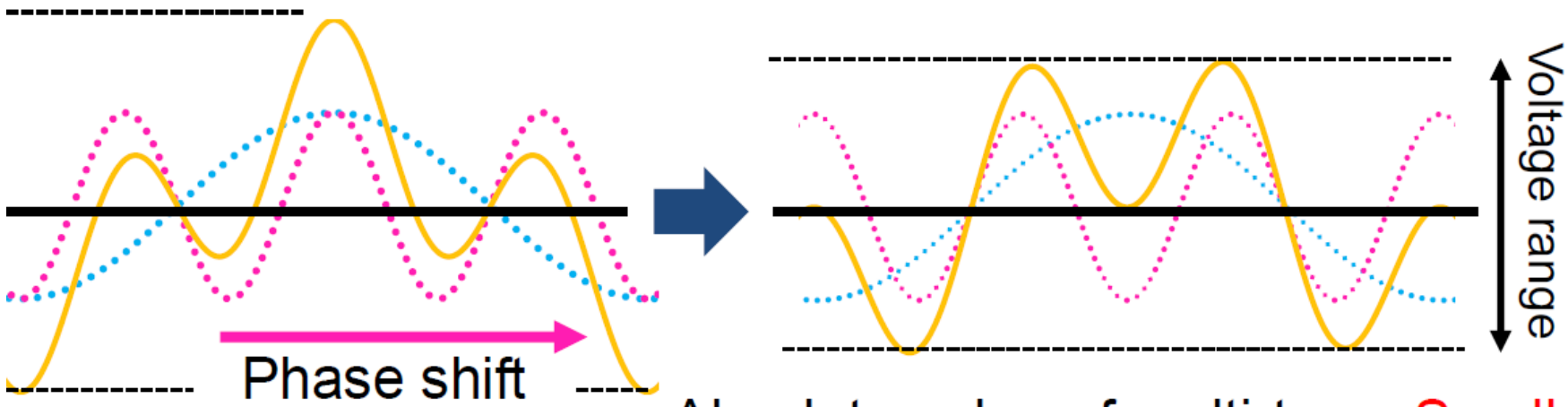


[6] "Analysis and Design of Multi-Tone Signal Generation Algorithms for Reducing Crest Factor", IEEE Asian Test Symposium (Nov. 2020).

What is Crest Factor ?

$$Crest\ Factor[dB] = 20log_{10}\left[\frac{\text{Maximum amplitude}}{\text{effective value}}\right]$$

Crest



Absolute value of multi-tone : Small

Crest factor (CF) reduction = Amplitude of each tone signal : Large

Improve SNR for multi-tone signals

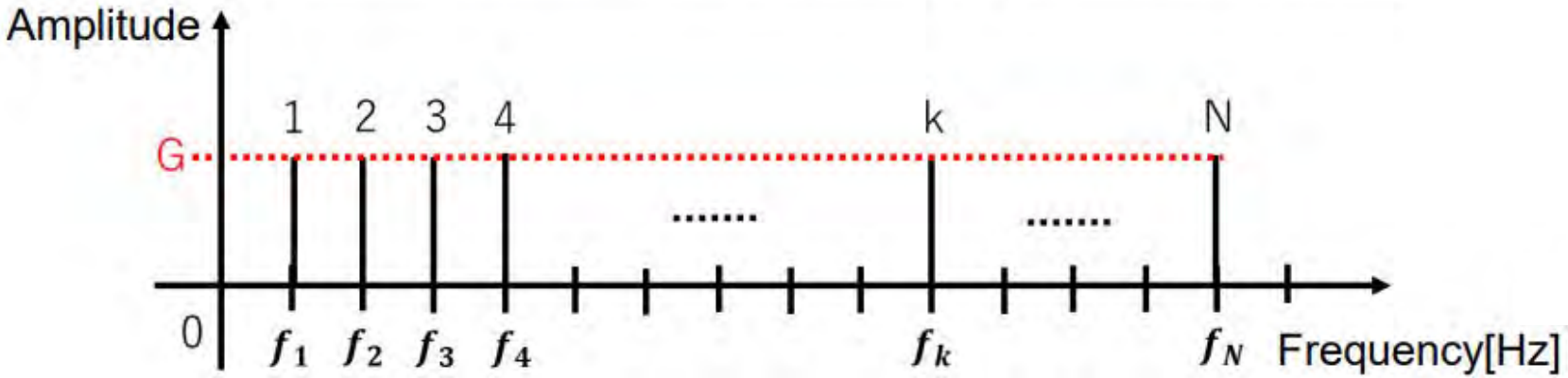
Multi-Tone Signal: Crest Factor Reduction

Basic equation : $s(t) = G\sum_{k=1}^{N} cos(\frac{2\pi f_k t}{T} + \theta_k)$

N : number of tones
T : resolution of 1 cycle

Newman Phase	$\theta_k = \frac{\pi}{N}(k-1)^2$
Kitayoshi Phase	$\theta_k = \frac{\pi}{N}k(k+1)$
Schroeder Phase	$\theta_k = -\frac{\pi}{N}k(k-1)$
Narahashi Phase	$\theta_k = \frac{\pi}{N-1}(k-1)(k-2)$

We showed these are equivalent for crest factor reduction



Crest factor ⇒ ~1.6

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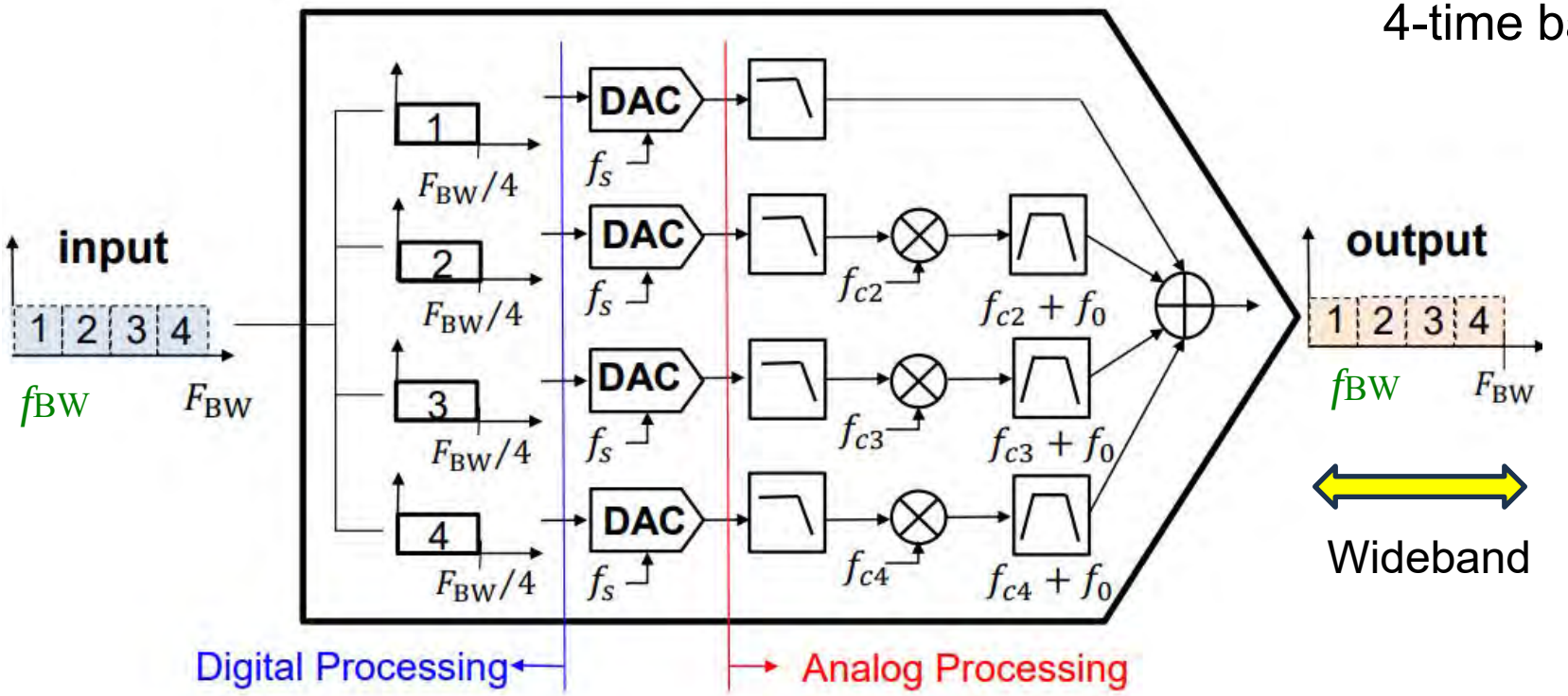
Wideband Signal: Bandwidth Interleaved DAC

4-time bandwidth of single DAC f_{BW}

$$F_{BW} = 4\, f_{BW}$$



Design of digital filters, analog filters, mixers is a key

[7] "Frequency Interleaved DAC System Design: Fundamental Problems and Compensation Methods,“ 8th International Congress on Information and Communication (Feb. 2023)

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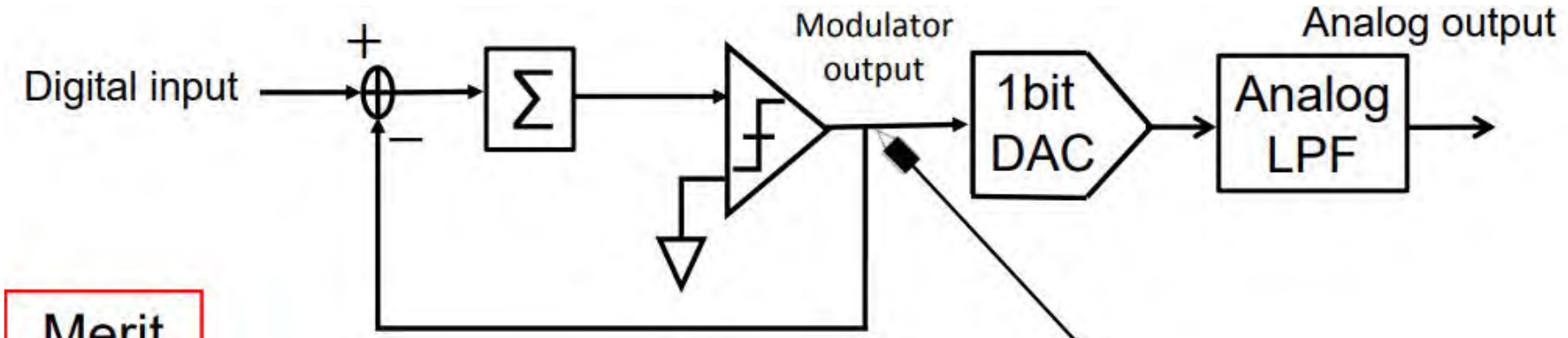
ΔΣ DAC: Limit Cycle



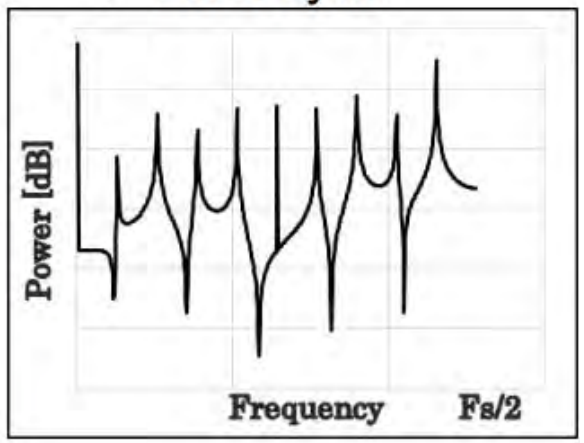
Merit

- Mostly digital circuit
- High linear & high resolution for low frequency signal generation

Demerit

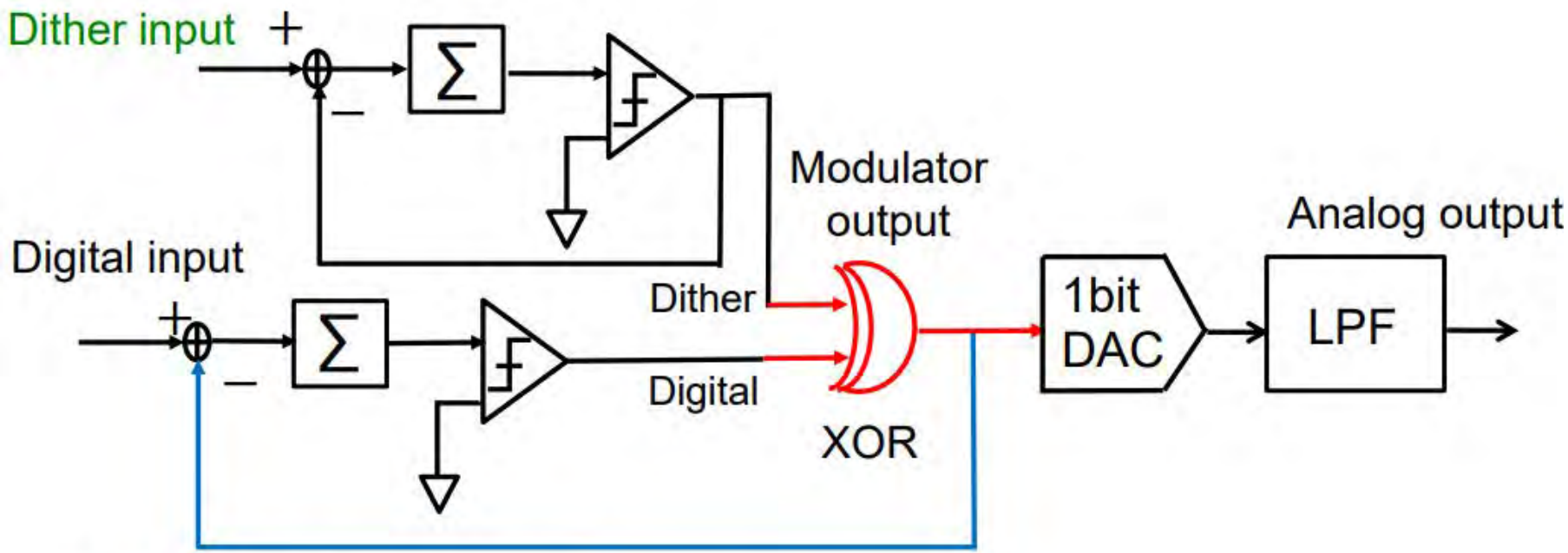
- Limit cycle problem for small input

Limit cycle



[8] "Limit Cycle Suppression Technique Using Digital Dither in Delta Sigma DA Modulator", IEEE International Conference on Solid-State and Integrated Circuit Technology (Oct. 2016).

ΔΣ DAC: Digital Dither Usage



< Features >

① 1-bit output

② Digital dither

⇒ NOT affect output signal, thanks to feedback

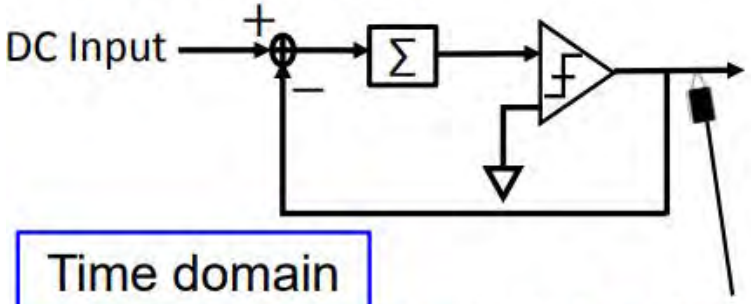
③ Easily generated digital dither

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Digital signal “1” reverses comparator output with XOR

ΔΣ DAC: Limit Cycle Suppression with Dither

- Without dither

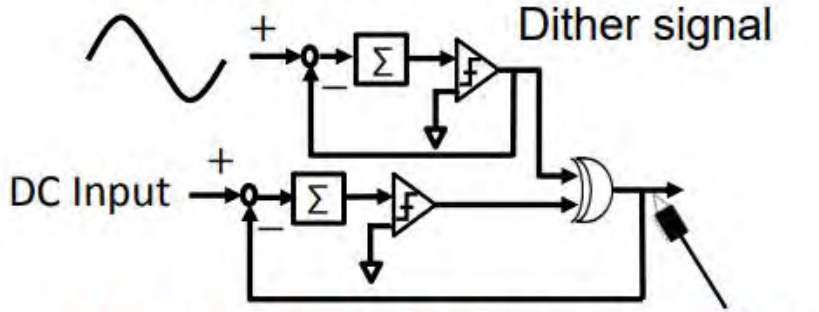


Time domain

1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0

Period

- With dither



1 0 0 0 0 1 0 1 0 0 0 0 0 1 0 0

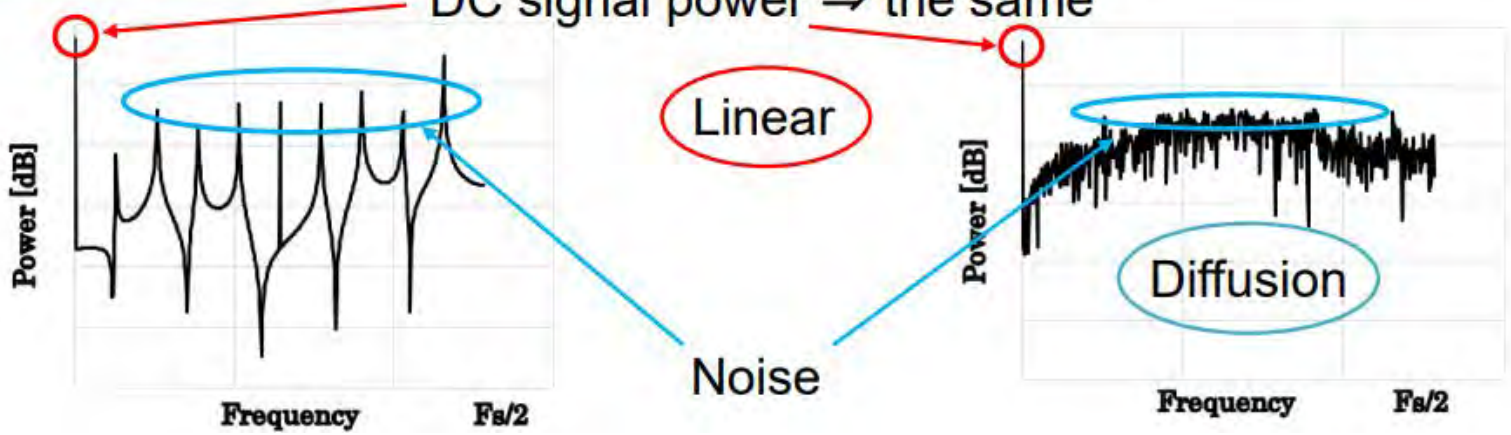
Not Periodic

✓ Orders of '0' and '1' ⇒ different

✓ Total numbers of 1's ⇒ the same

Frequency domain

DC signal power ⇒ the same



Outline

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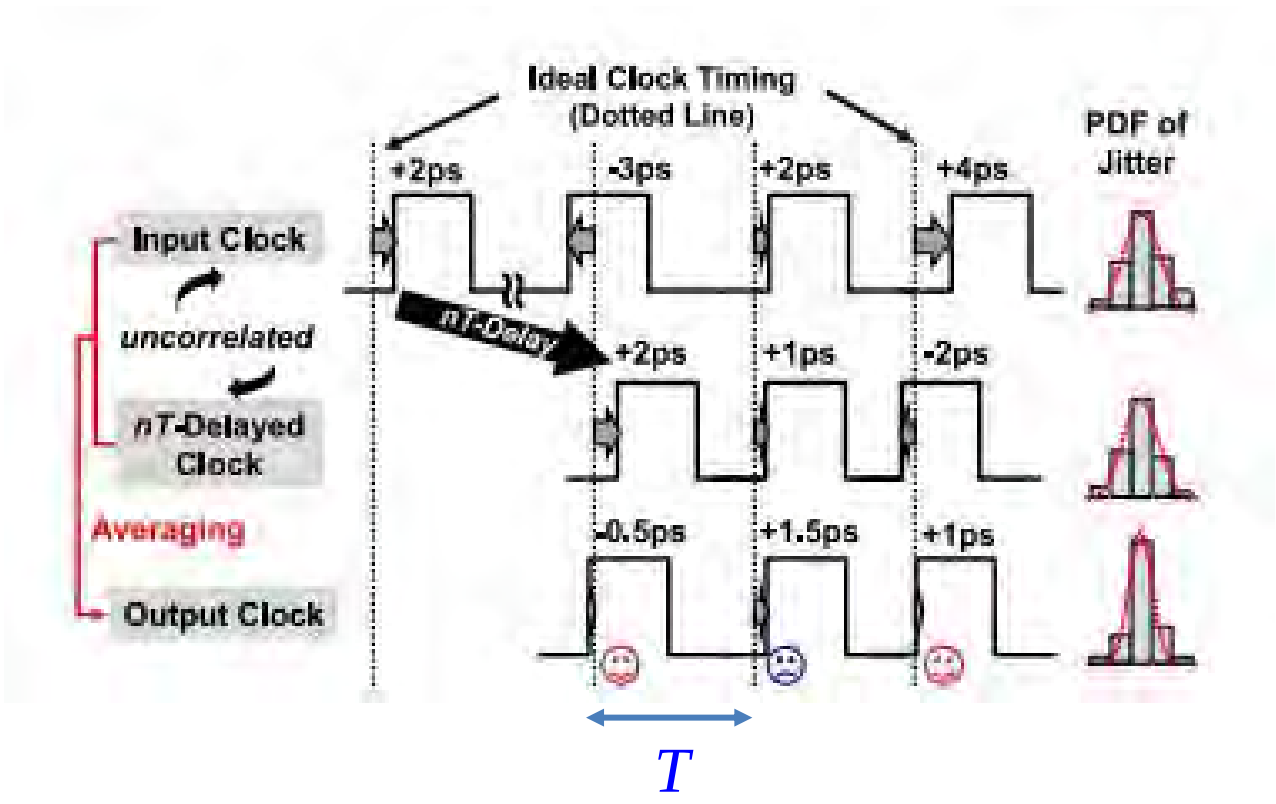
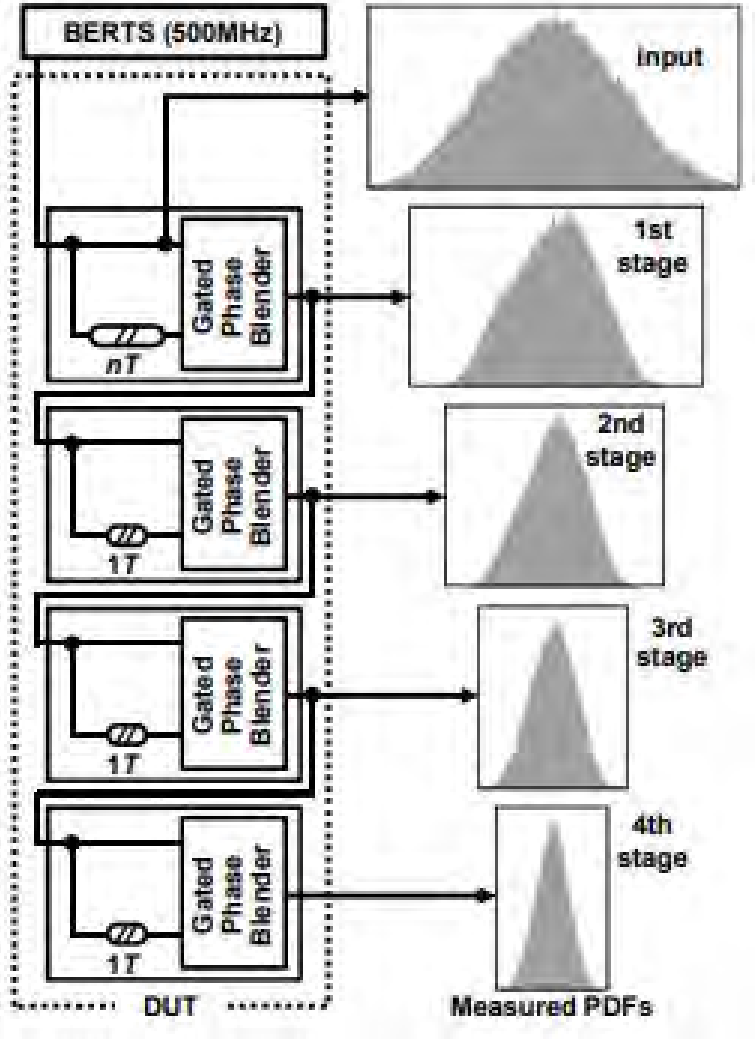
- Clock Jitter Reduction
- Analog Filter
- Conclusion

Clock Jitter Reduction: Phase Blending Method



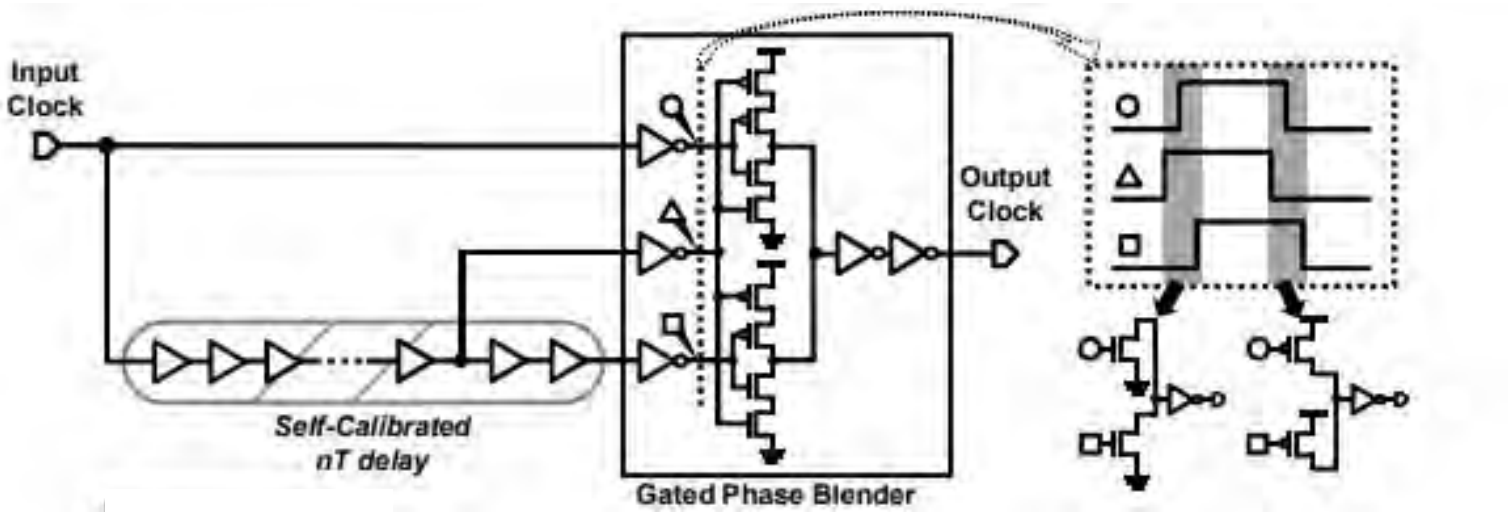


Clock edges are averaged ⇨ Jitter reduction

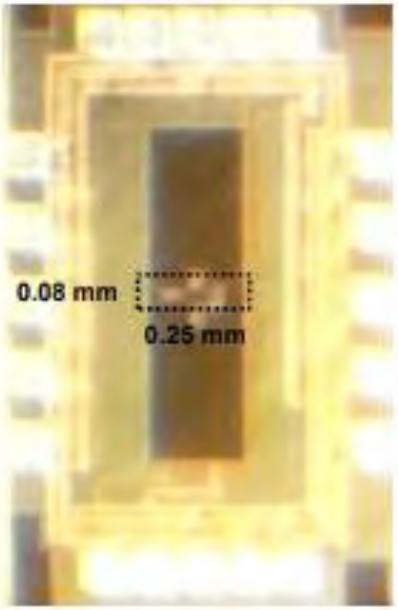
[9] "A Clock Jitter Reduction Circuit Using Gated Phase Blending Between Self-Delayed Clock Edges," IEEE Symposium on VLSI Circuits, Honolulu (June 2012).

Circuit, Measurement Results

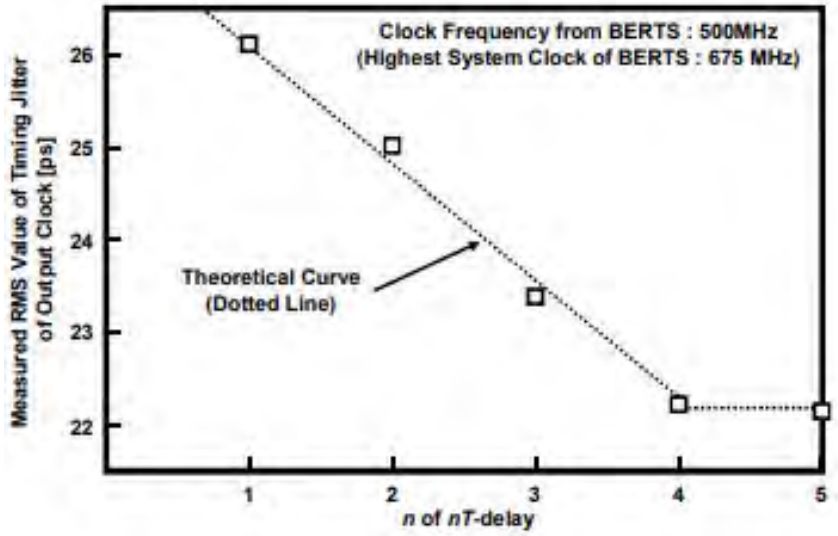
Phase blended circuit



Chip photo (180nm CMOS)



Measurement result per stage



Jitter

30.2ps

8.8ps with 4-stage

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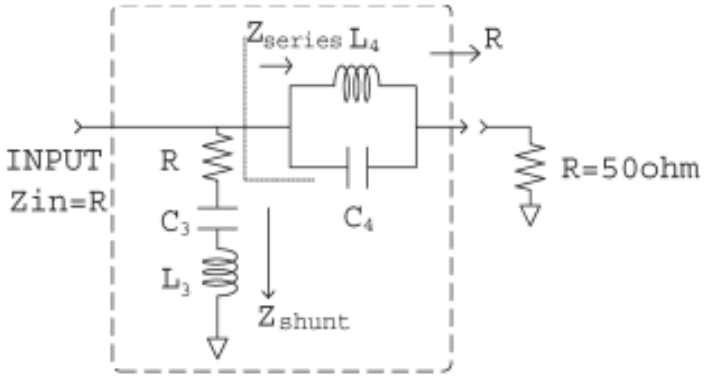
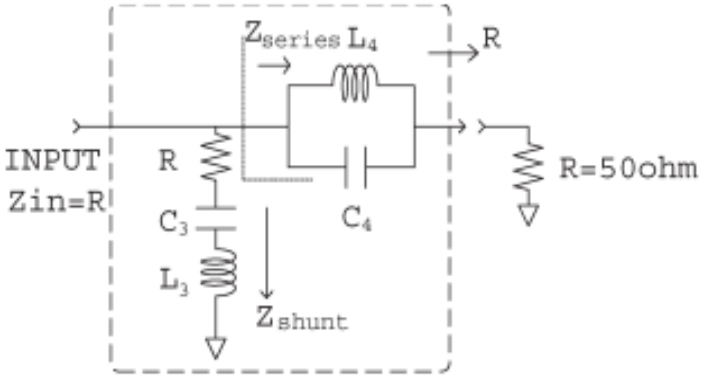
High Performance Analog Filter

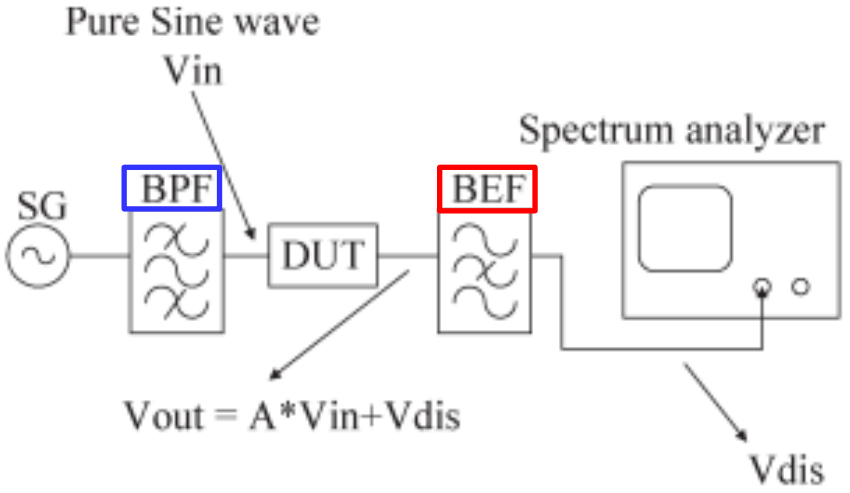
- Cascade of LCR passive filters
  - ⇨ Very linear, High Q
  - ⇨ Direct sinewave generation from clock is possible.



Single-stage of
Band Pass Filter (BPF)



Single-stage of
Band Elimination Filter (BEF)

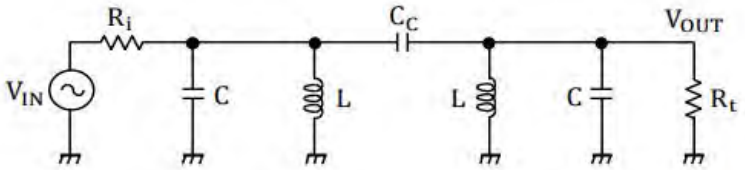


Total Harmonic Distortion (THD)
Measurement System

20-stage BPF:
Integration of discrete components

[10] "Total Harmonic Distortion Measurement System for Electronic Devices up to100MHz with Remarkable Sensitivity"
IEEE Trans. Instrumentation and Measurement (Dec. 2007).

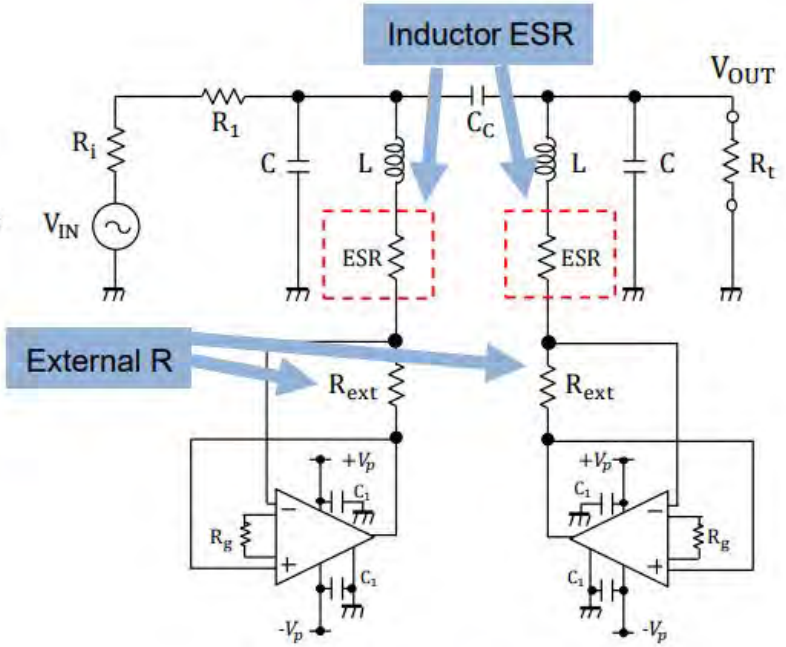
Low Cost Analog Filter



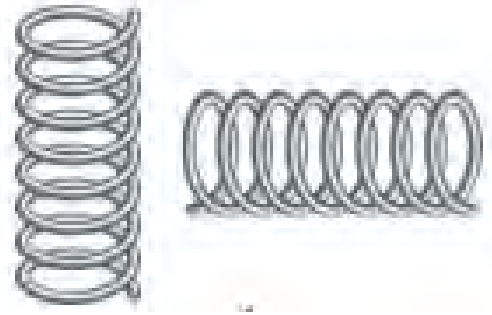
Ideal LC BPF

Only 4th-order BPF filter

Low cost



Active compensation
for series resistance
of inductor L

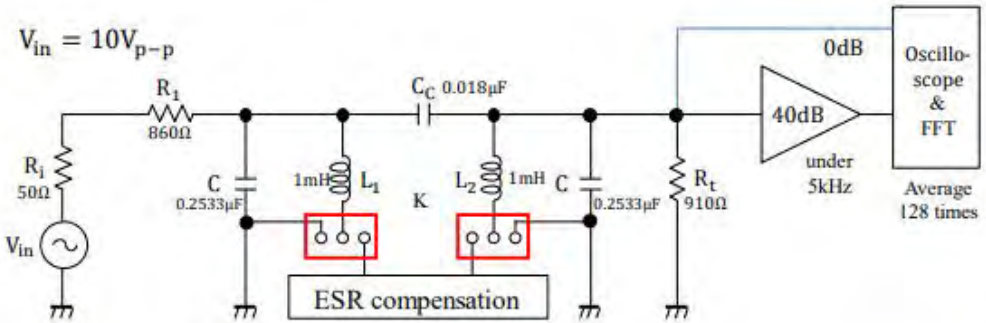


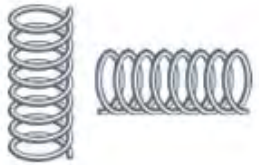
Perpendicular placement
of two inductors L
for mutual inductance M reduction

High Q

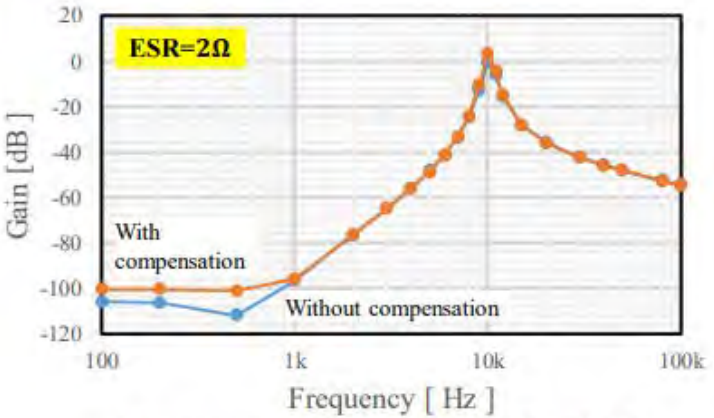
[11] "Design Consideration for LC Analog Filters:
Inductor ESR Compensation, Mutual Inductance Effect and Variable Center Frequency"
8th International Congress on Information and Communication (Feb. 2023)

Measurement Verification

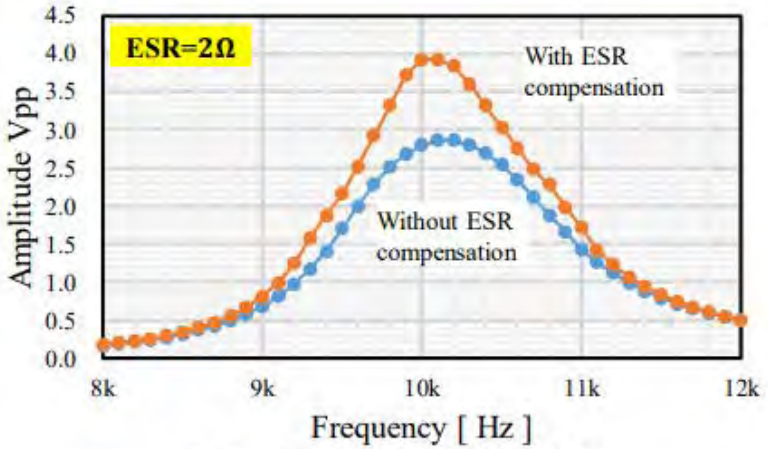




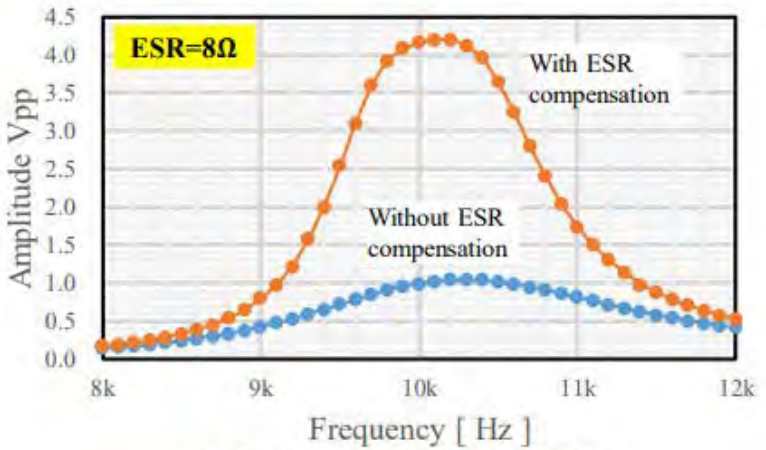
Perpendicular placement of L_1, L_2



Measured result with ESR of 2Ω



Enlarged with ESR of 2Ω



Enlarged with ESR of 8Ω

Q is enhanced

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Conclusion

- Explained research achievements
  - Author's Group
  - Signal generation technologies for AMS IC testing

- Trend is found:
  - Digital-oriented methods become more employed
  - Often the analog circuit is a key for very high performance.

Acknowledgements

Kobayashi laboratory members and research associates, especially O. Kobayashi, K. Asami, K. Niitsu, T. Nakatani, K. Sato, M. Kawabata, T. Komuro and P. Sarson