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15:45-16:15

Invited

Back to the Analog Neural Network and Linear Circuit

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Outline

- Objective of This Paper
- Dynamics of Active Resistor Network in Vision Chip
- Switched Capacitor Network ADC
  Inspired by Hopfield Network
- Design and Analysis of Resistor Network DAC
- Conclusion

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Objective of This Paper

Revisit legacy analog neural networks and
explore new analog circuit areas

[RC Network Theory]

Spatial and temporal dynamics of active resistor network

[New ADC Architecture]

Hopfield Network ADC with switched capacitor circuits

[New Resistor Ladder DAC]

Motivated by the above two analog neural networks

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- Objective of This Paper
- Dynamics of Active Resistor Network in Vision Chip
- Switched Capacitor Network ADC
  Inspired by Hopfield Network
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- Conclusion

Active resistor network: positive and negative resistors

Research Outline of Active Network Dynamics

Our previous theorem:

Spatial and temporal stability conditions are equivalent

for uniform active resistor network

This paper:

Investigation of spatial and temporal dynamics

for non-uniform active resistor network

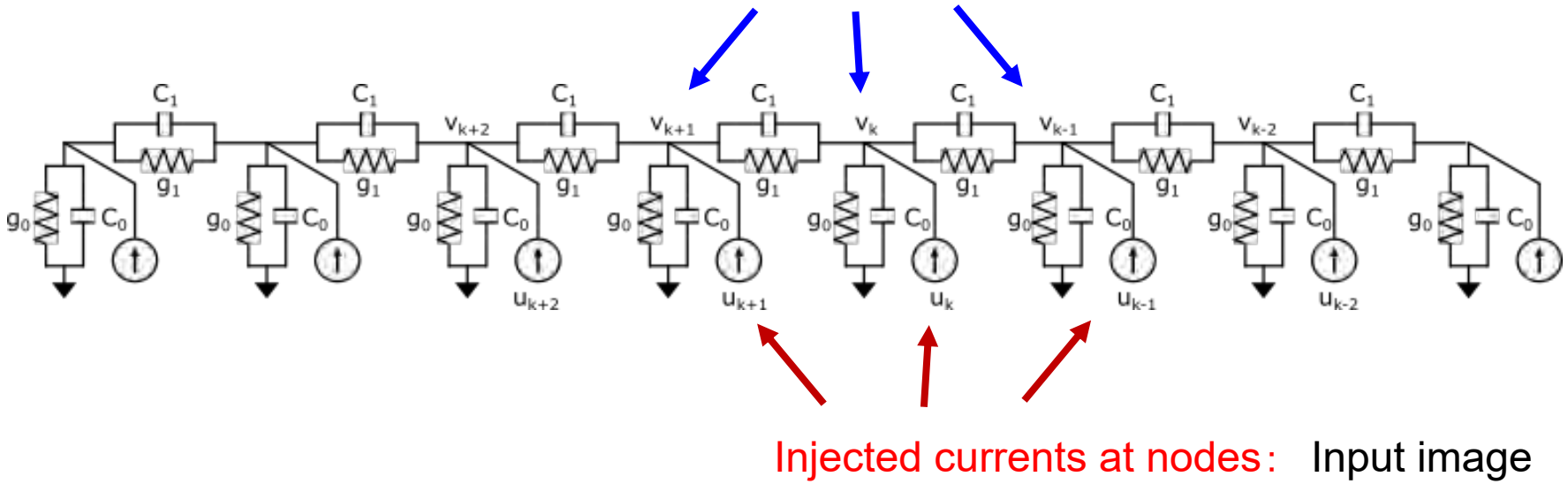
⇨ Four new findings

Retina Chip with Positive Resistor Network

High-speed analog image-smoothing processor

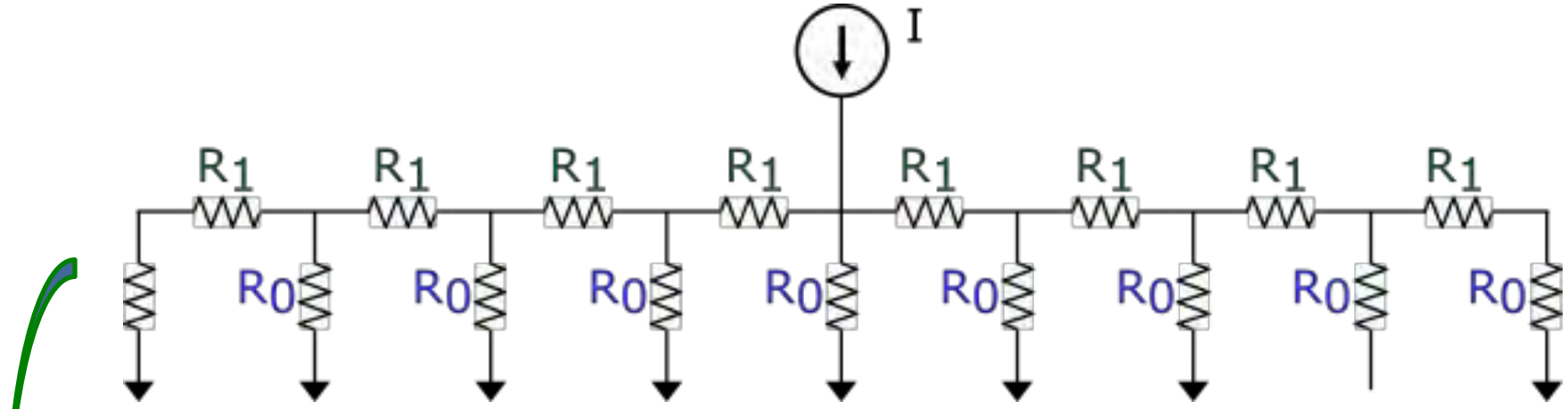
1D image case

$g_0 = 1/R_0$
$g_1 = 1/R_1$



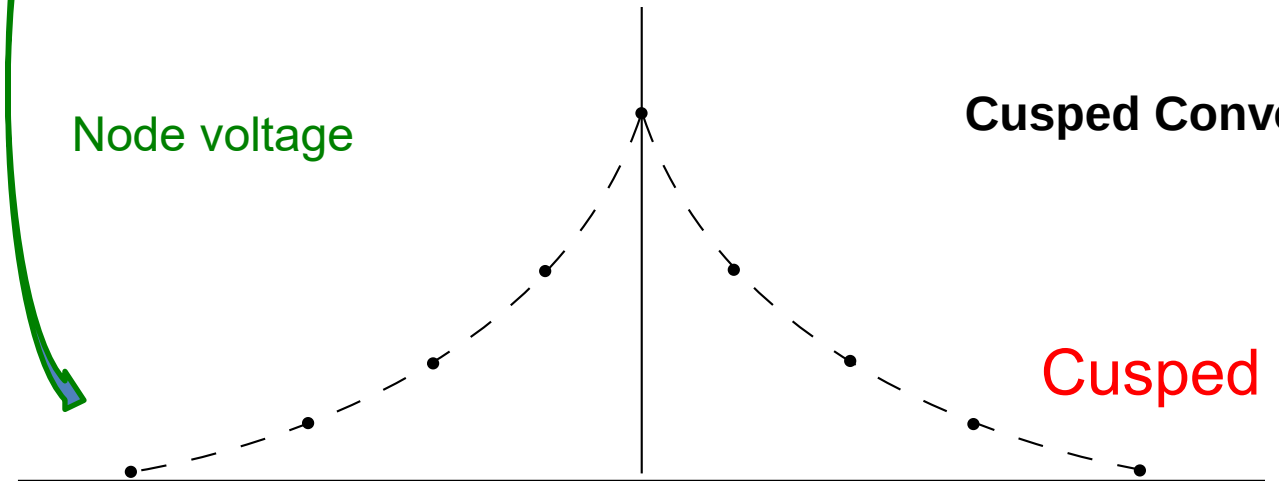
[1] C. A. Mead, Analog VLSI and Neural Systems, Addison Wesley, 1989

Spatial Impulse Response of Retina Chip



Node voltage

Cusped Convolution Kernel



Cusped spatial impulse response

Gaussian Chip with Active Resistor Network

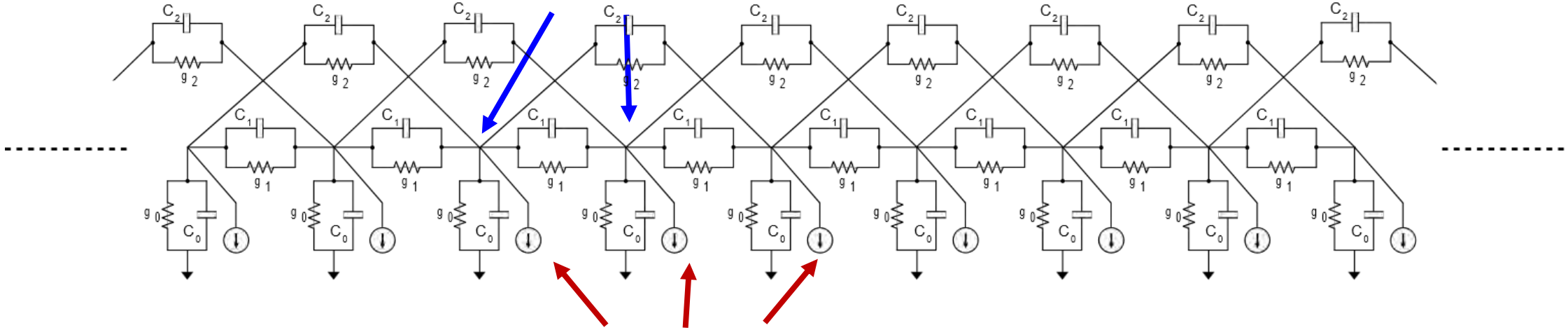
High-speed analog image processor

$$g0 = 1/R0$$
$$g1 = 1/R1$$
$$g2 = 1/R2$$

1D image case

Negative resistor $R2 = -4R1 < 0$

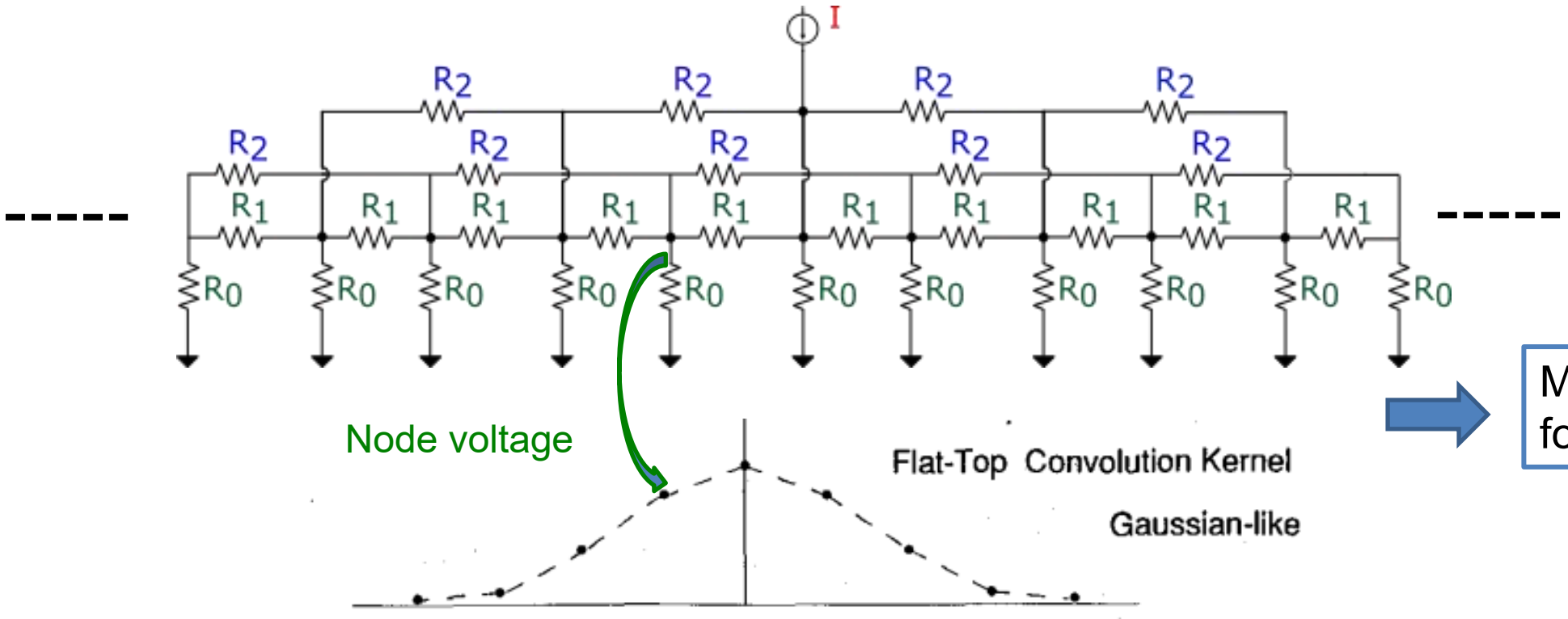
Node voltages: Output image



Injected currents at nodes: Input image

[2] H. Kobayashi, J. L. White, A. A. Abidi, “An Active Resistor Network for Gaussian Filtering of Images", IEEE Journal of Solid-State Circuits (May 1991)

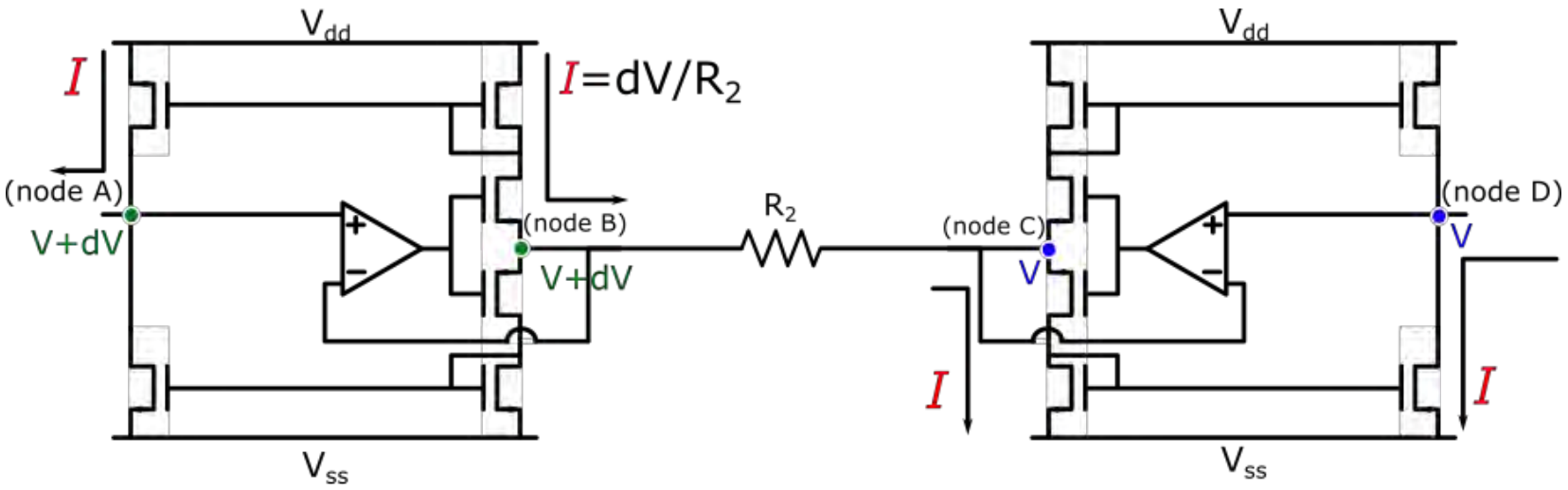
Spatial Impulse Response of Gaussian Chip



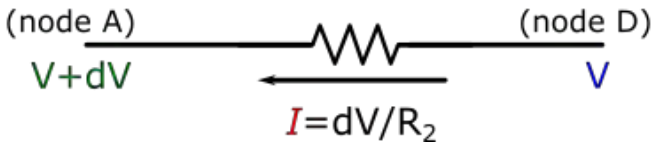
More desirable
for image processing

Flat-top spatial impulse response

Negative Resistor with Standard CMOS



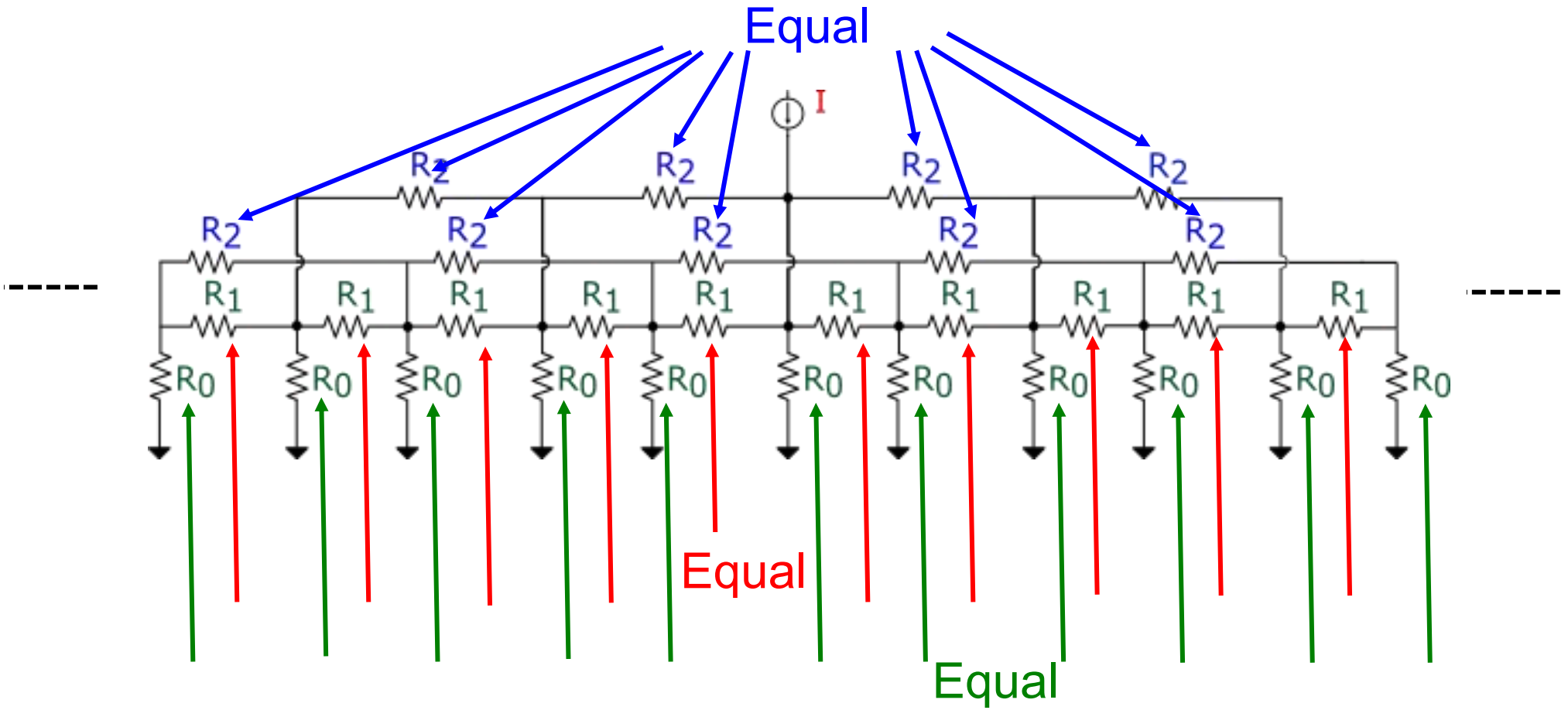
Negative Resistor $-R_2$



V+dV @ Node A > V @ Node B

Current $I = \frac{dV}{R_2}$

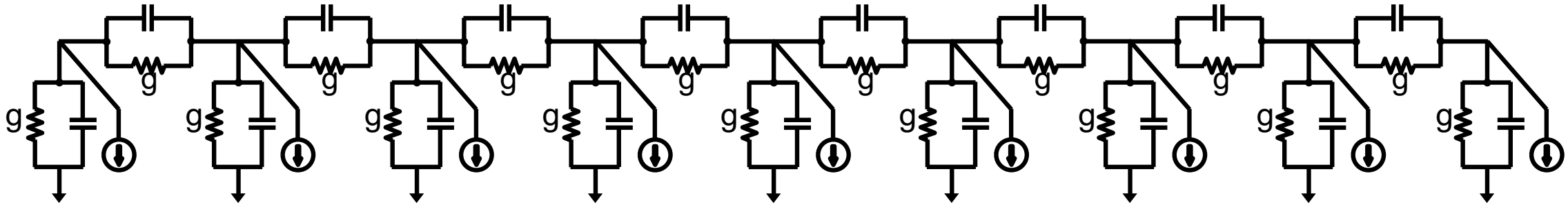
Uniform Resistor Network for Spatial Dynamics

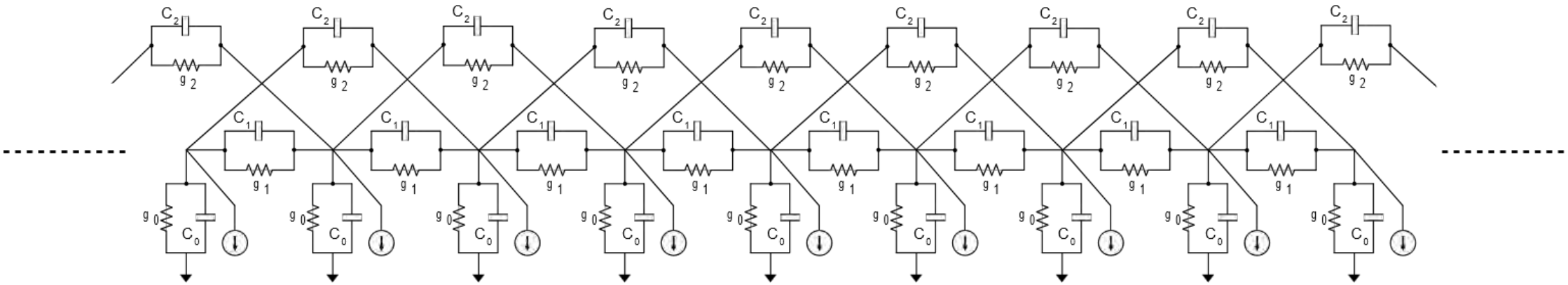


- Shift invariant
- Spatial transfer function can be defined

Temporal Dynamics with R, C

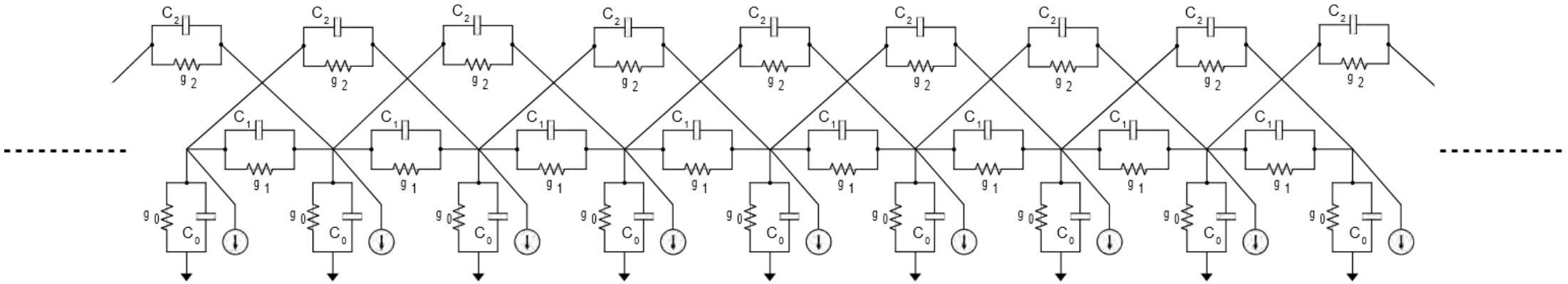
Capacitances are considered for temporal dynamics





Simulation Results: Spatial Temporal Stabilities

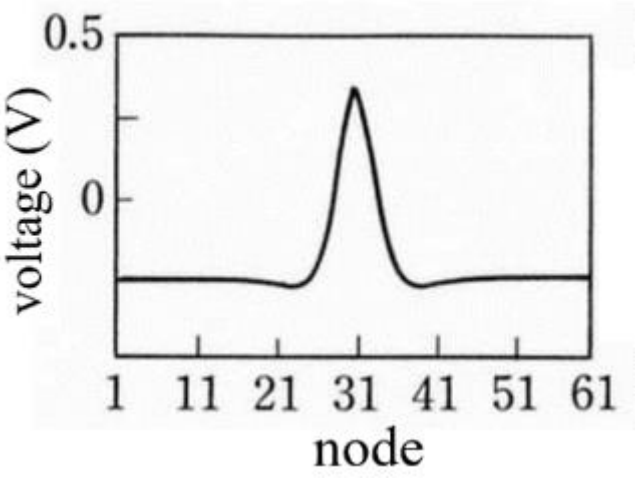
$R_0 = 1/g_0 = 200\text{k}\Omega, \quad R_1 = 1/g_1 = 5\text{k}\Omega, \quad R_2 = 1/g_2 = -20\text{k}\Omega$

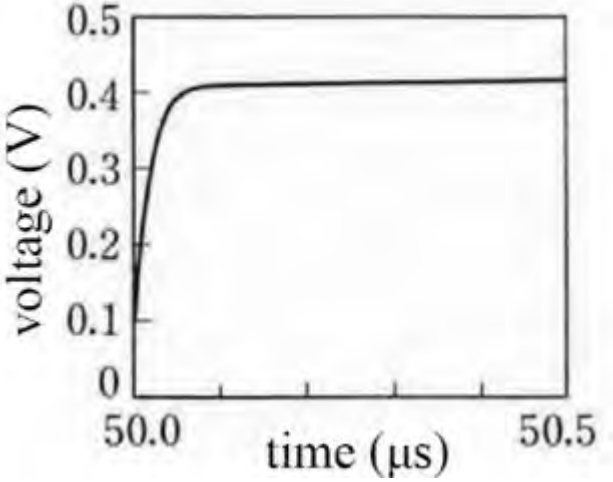


Spatially stable

Temporally stable

Spatial impulse response

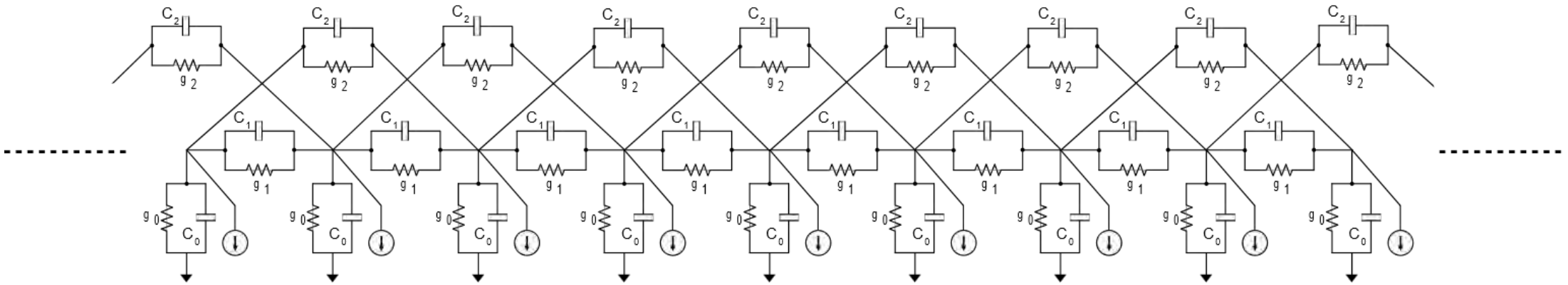




Temporal step response

Simulation Results: Spatial Temporal Instabilities

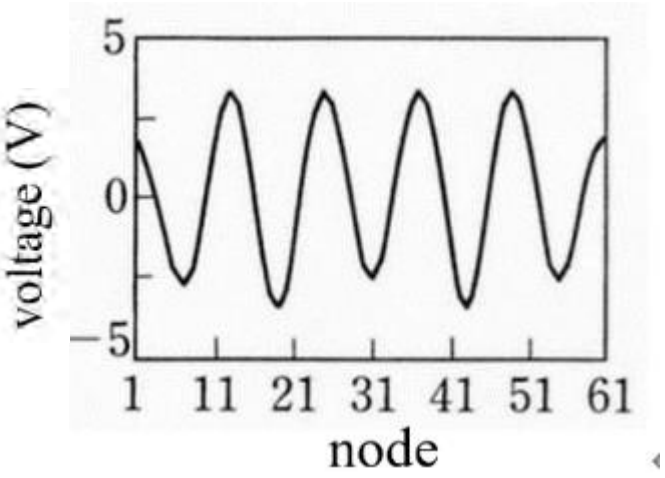
$R_0 = 1/g_0 = 200\text{k}\Omega, \quad R_1 = 1/g_1 = 5\text{k}\Omega, \quad R_2 = 1/g_2 = -17\text{k}\Omega$

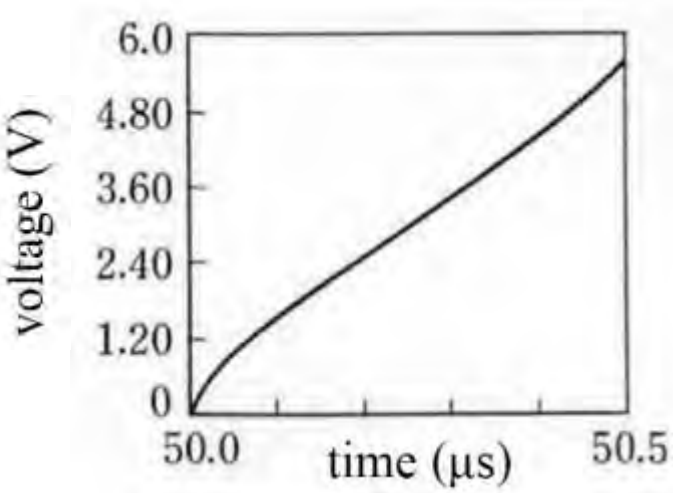


Spatially unstable

Temporally unstable

Spatial impulse response





Temporal step response

Circuit Network Theorem

For uniform network with positive and negative resistors, spatial and temporal stability conditions are equivalent.

[3] T. Matsumoto, H. Kobayashi, Y. Togawa,
"Spatial Versus Temporal Stability Issues in Image Processing Neuro h ips",
IEEE Trans. Neural Networks, (July 1992).

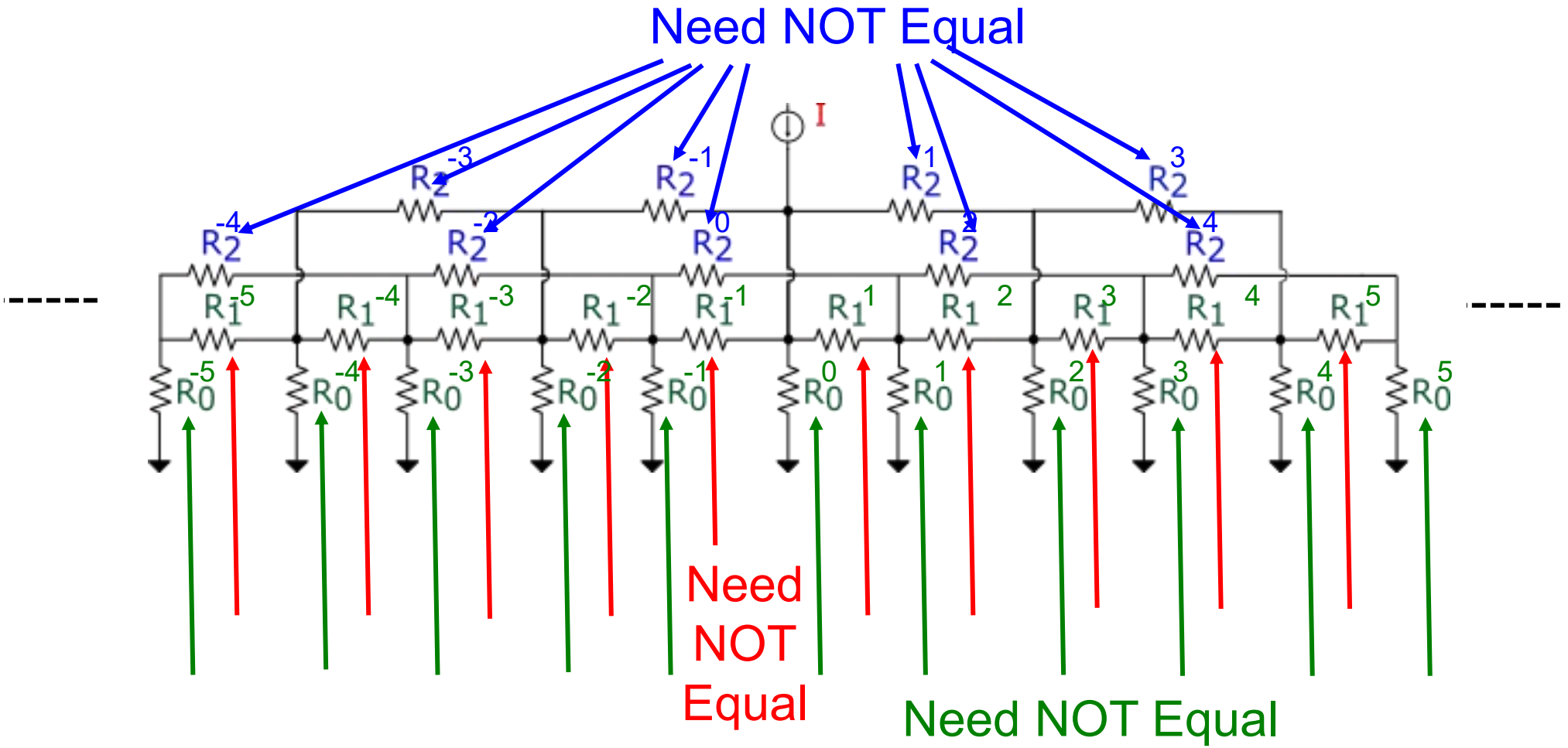
[4] H. Kobayashi, T. Matsumoto, J. Sanekata,
"Two-Dimensional Spatio-Temporal Dynamics of Analog Image Processing Neural Networks",
IEEE Trans. Neural Networks (Oct. 1995).

How about non-uniform network ?

A part is shown in

[5] M. Chiba, et. al., "Spatial and Temporal Dynamics of Non-Uniform Active Resistor Networks"
IEEE 16th International Conference on Solid-State and Integrated Circuit Technology (Oct. 2022)

Non-Uniform Resistor Network

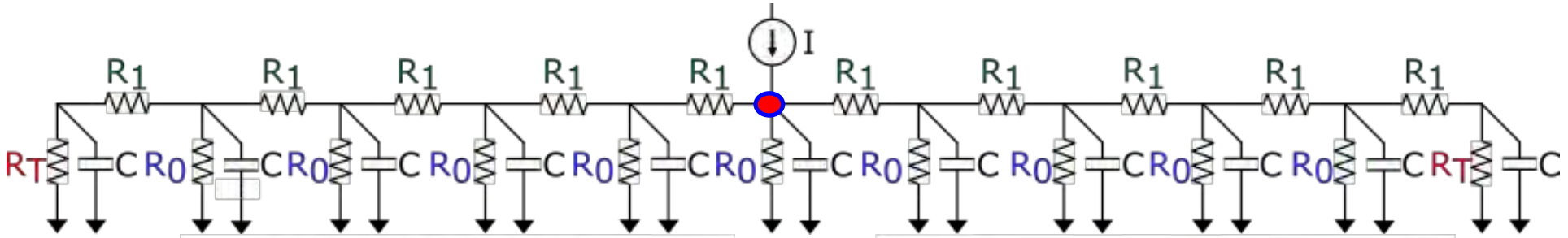


- Shift variant
- Spatial transfer function CANNOT be defined

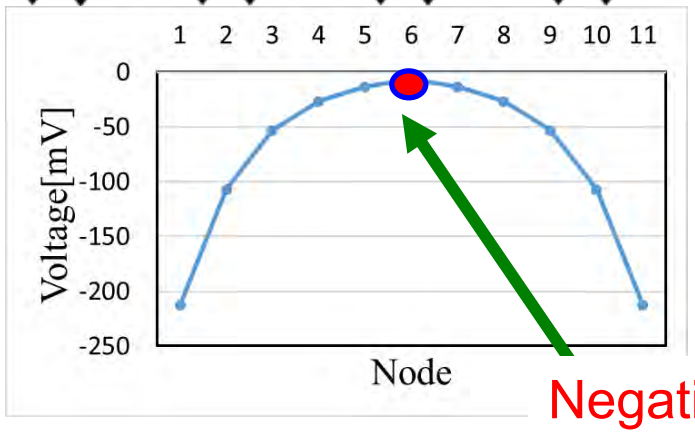
Finding 1

If there is a node where the input current is injected and its node voltage as the spatial impulse response is negative,

➡ *the network is temporally unstable*

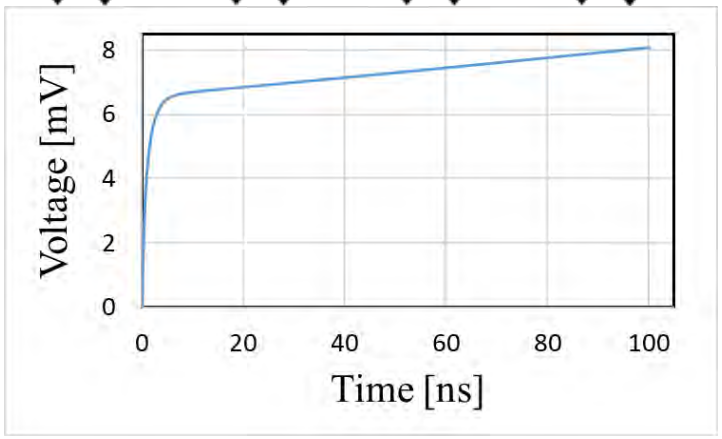


$R_0 = 2\text{k}\Omega$
$R_1 = 1\text{k}\Omega$
$R_T = -2\text{k}\Omega$



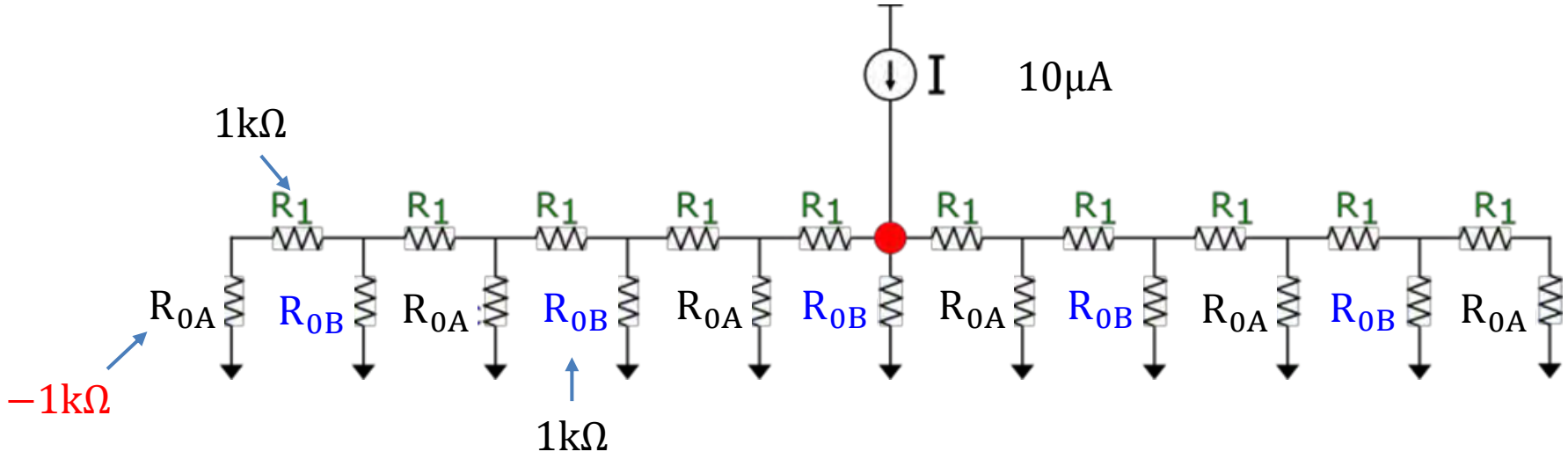
Negative

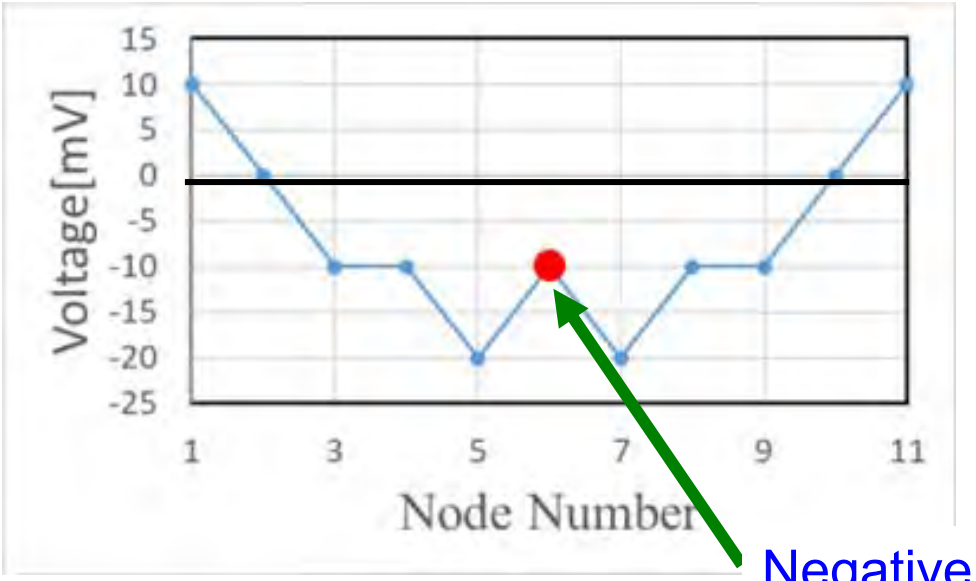
Spatial Impulse Response



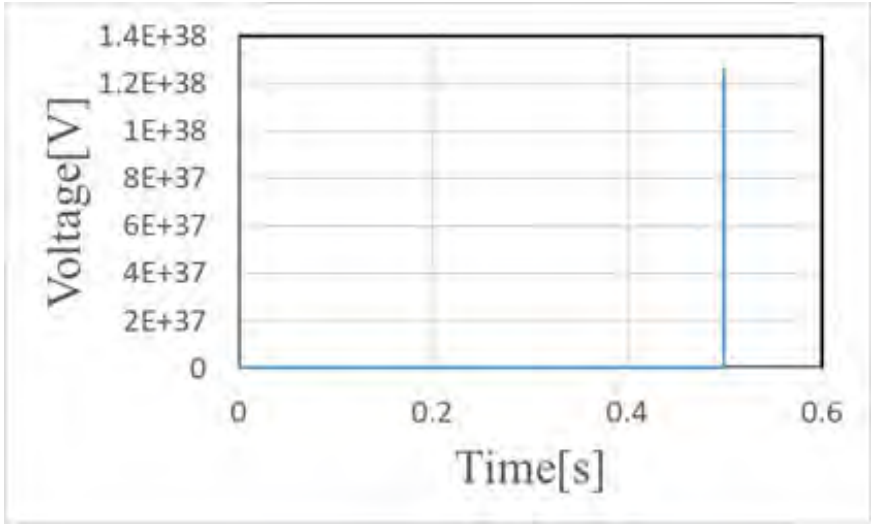
Temporally unstable

1st Nearest Connection (2)



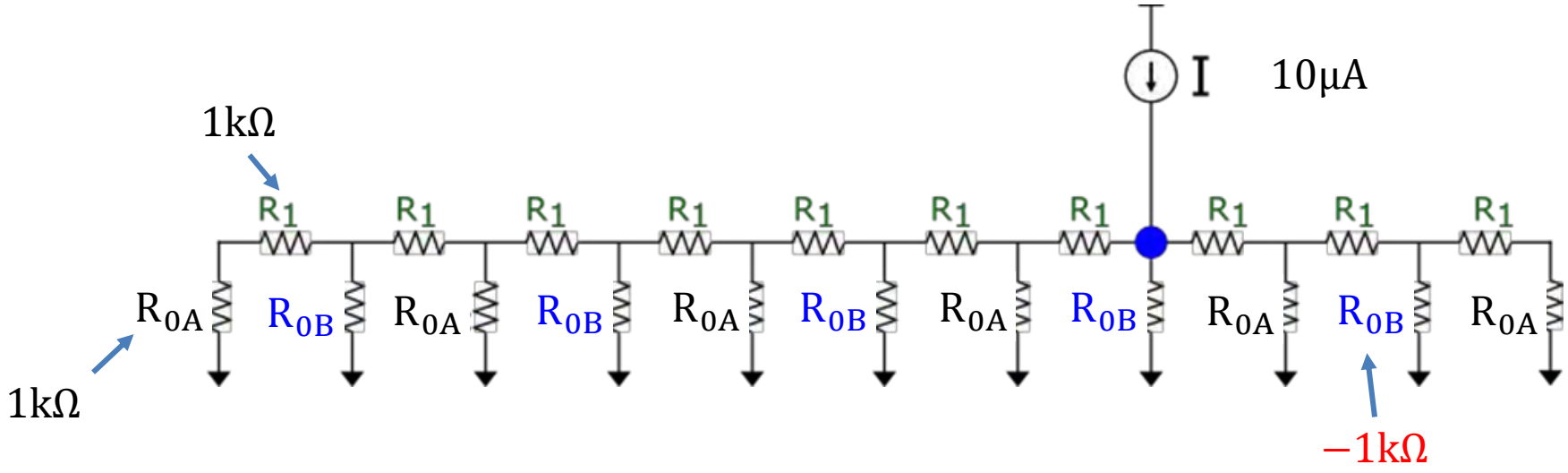


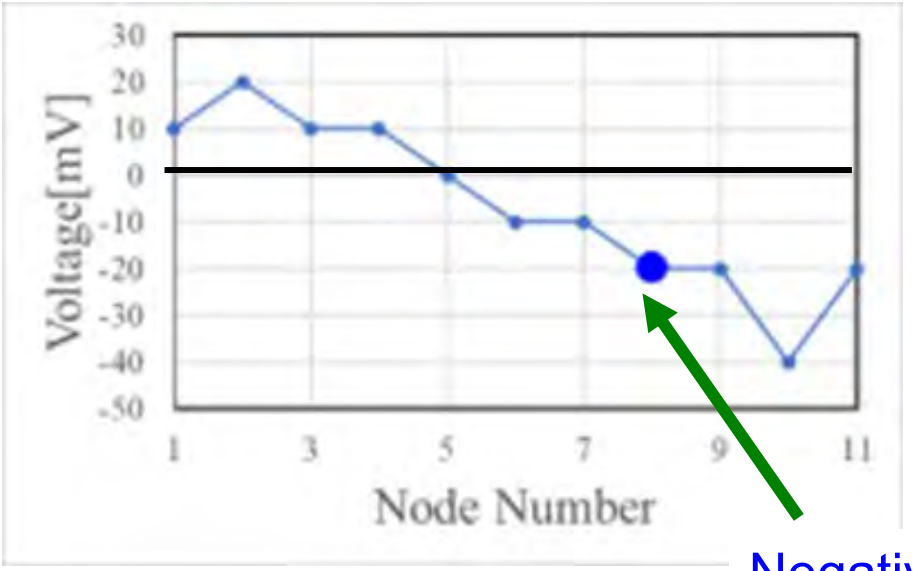
Negative



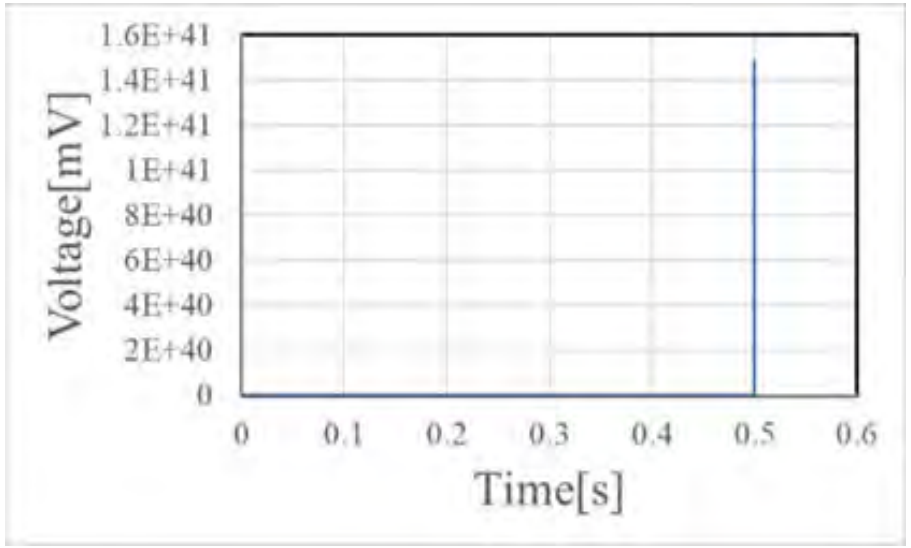
Temporally Unstable

1st Nearest Connection (3)



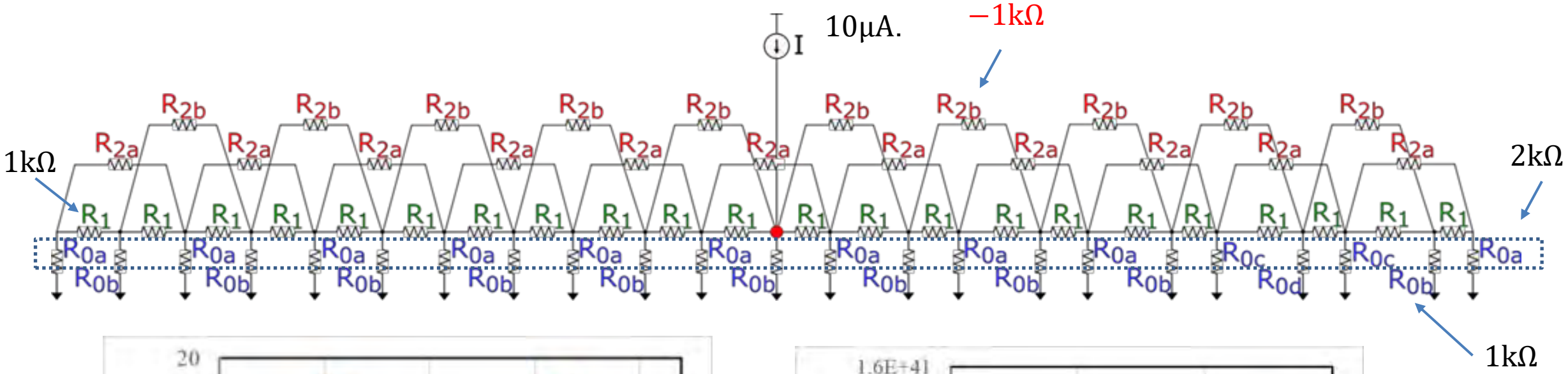


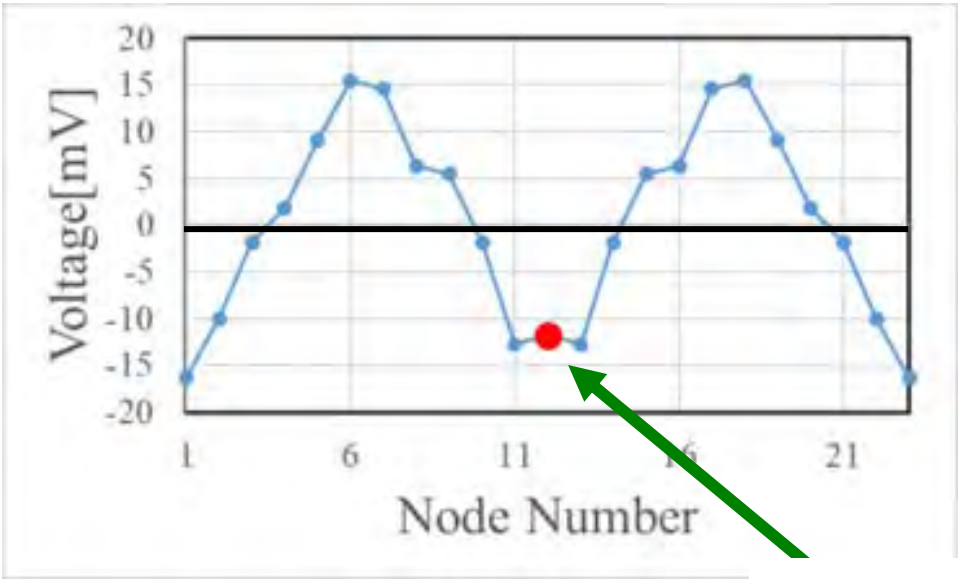
Negative



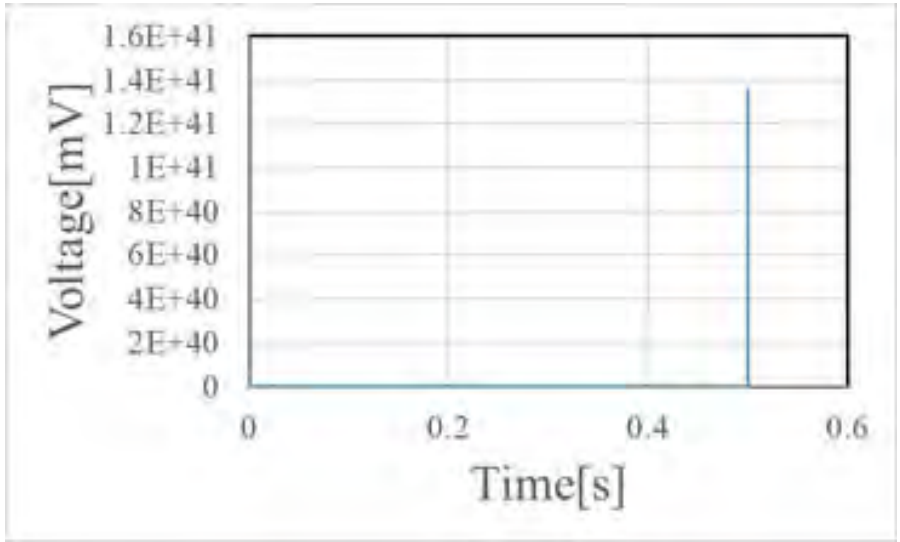
Temporally Unstable

2nd Nearest Connection (1)



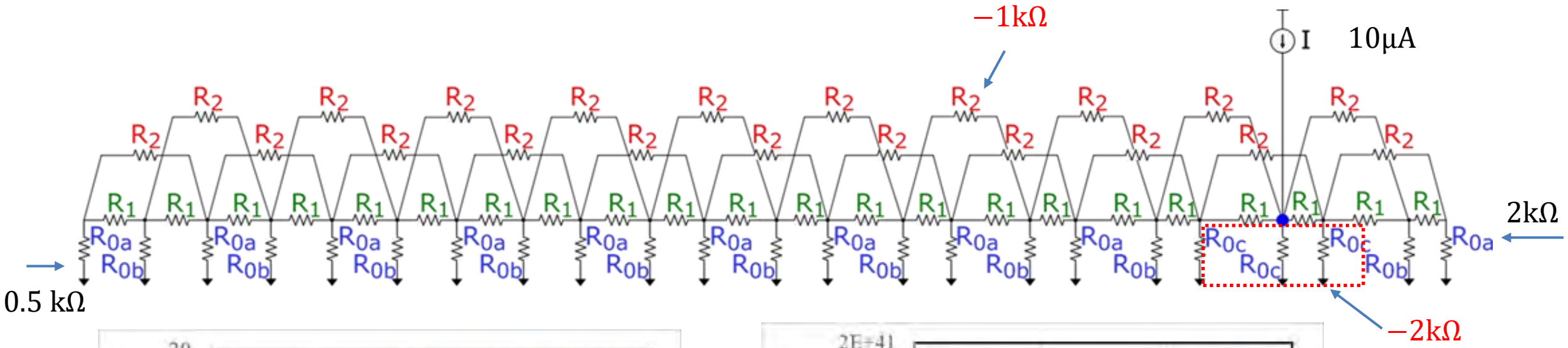


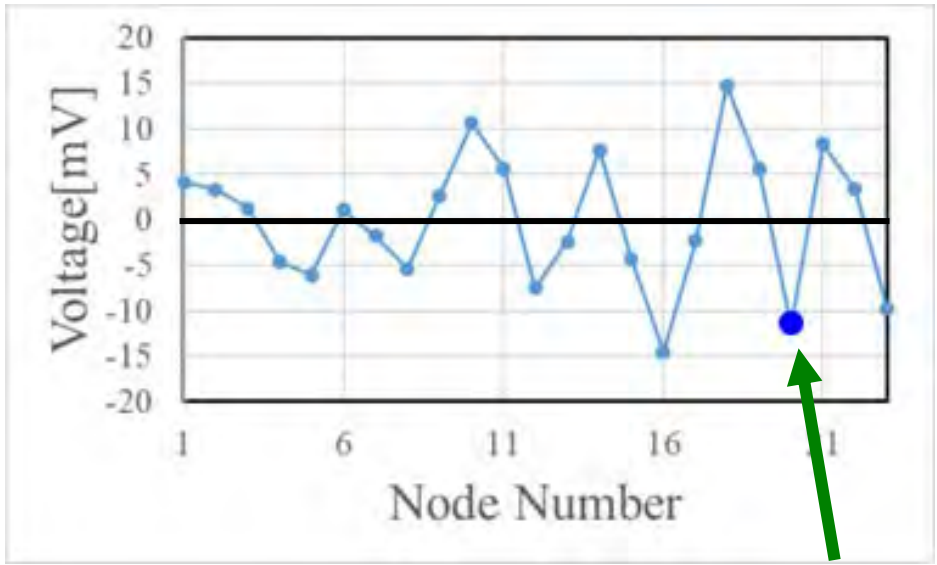
Negative



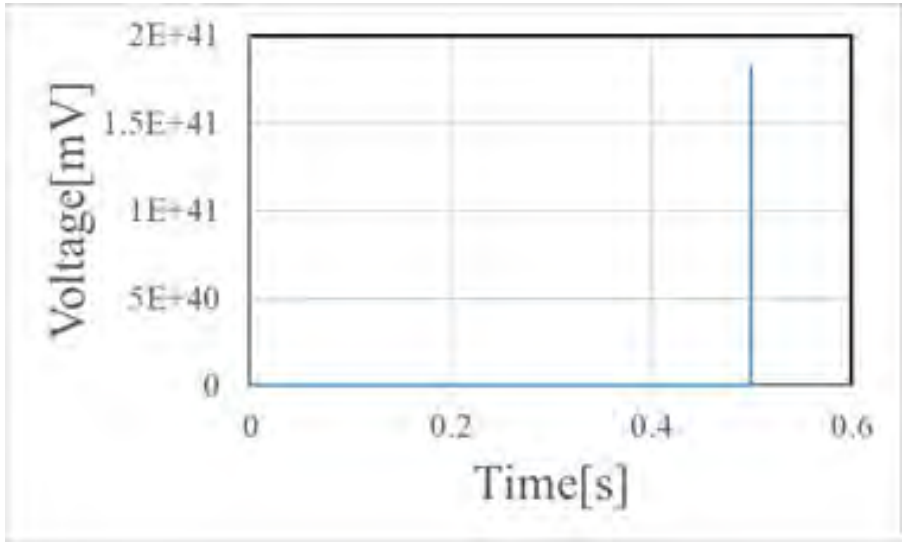
Temporally Unstable

2nd Nearest Connection (2)



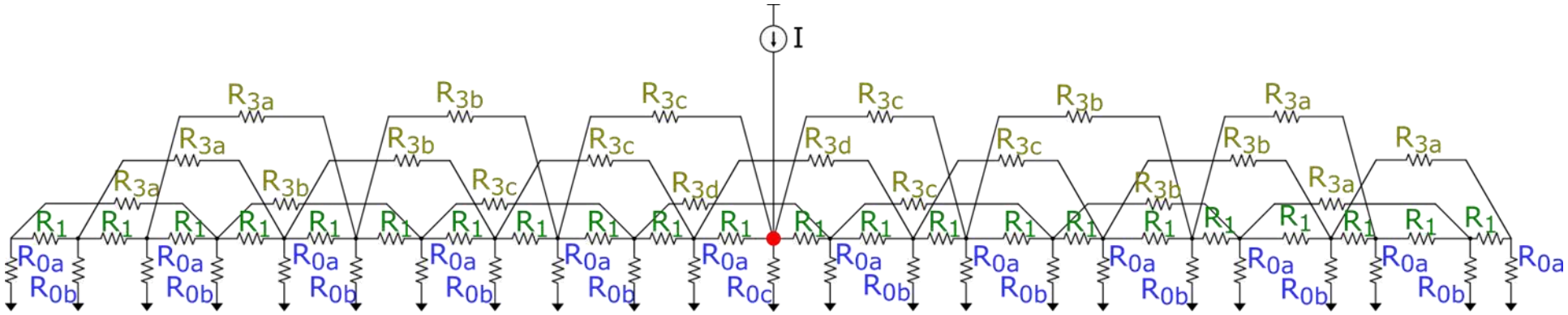


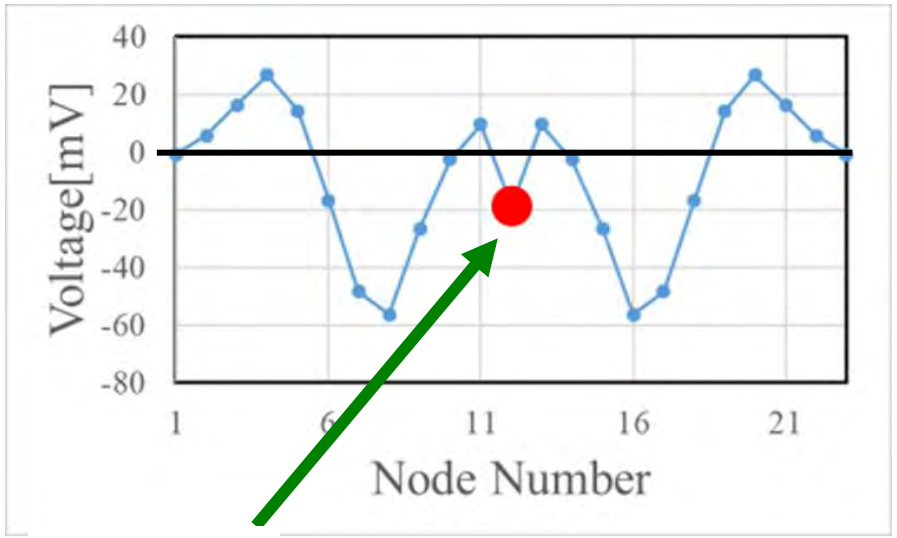
Negative



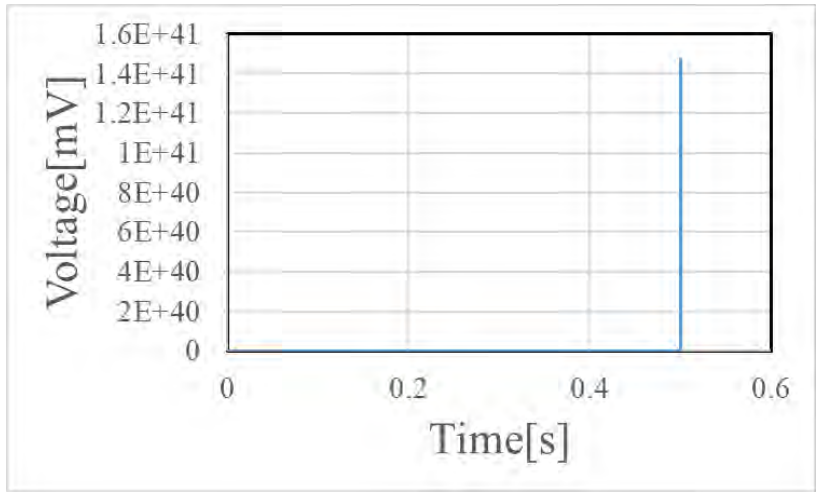
Temporally Unstable

3rd Nearest Connection





Negative



Temporally Unstable

$$R_{0a} = 2k\Omega, R_{0b} = 3k\Omega, R_{0c} = -0.25k, R_1 = 1k\Omega, R_{3a} = -4k\Omega$$
$$R_{3b} = -3k, R_{3c} = -2k, R_{3d} = -1k\Omega, I = 10\mu A$$

Finding 2

For all nodes,

"The input current is injected at each one node and

its node voltage as the spatial impulse response is positive",

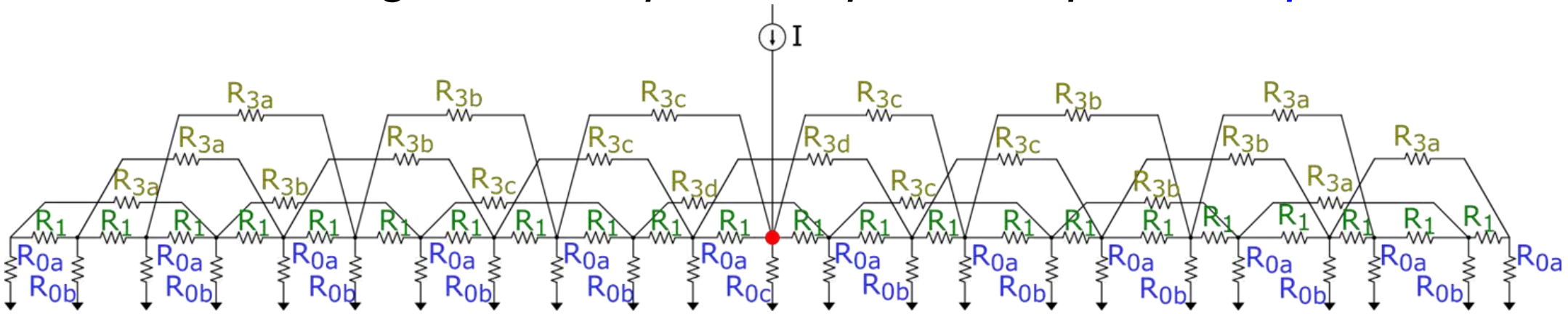
⇒ *Some networks can be temporally unstable.*

We have found such an example by simulation

Theoretical analysis is left.

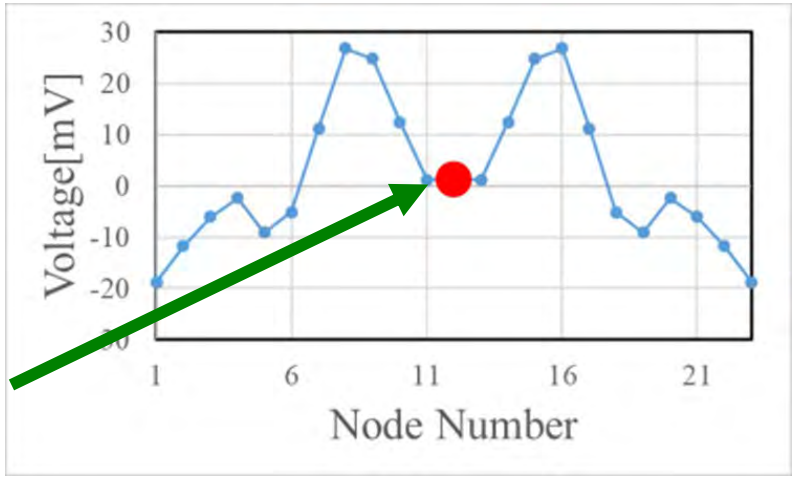
3rd Nearest Connection

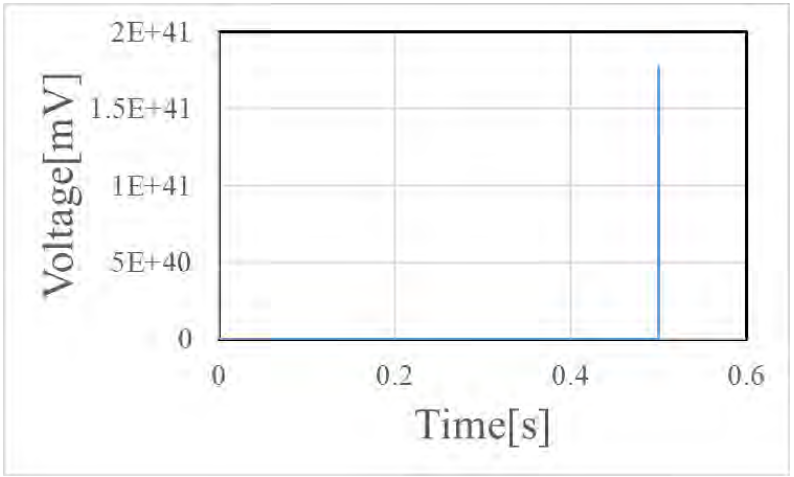
For all nodes, "the input current is injected at a node and its node voltage as the spatial impulse response is positive",



$R_{0a} = 2\text{k}\Omega,\ R_{0b} = 3\text{k}\Omega,\ R_{0c} = -0.25\text{k},\ R_1 = 1\text{k}\Omega,\ R_{3a} = -1\text{k},\ R_{3b} = -2\text{k},\ R_{3c} = -3\text{k},\ R_{3d} = -4\text{k}\Omega,\ I = 10\mu\text{A}$

Positive

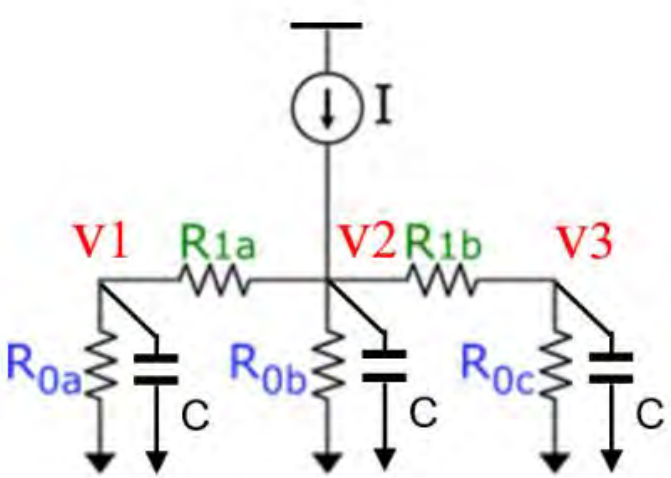


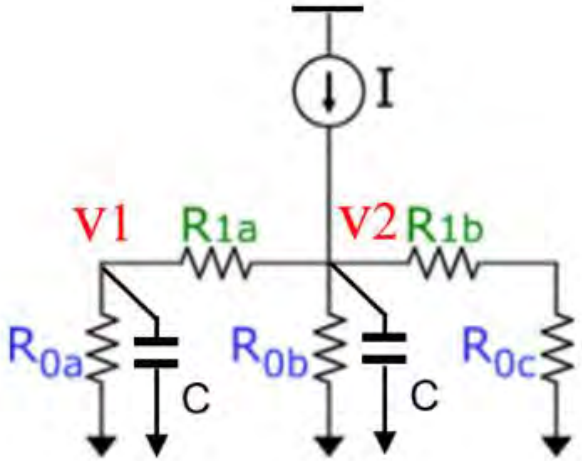


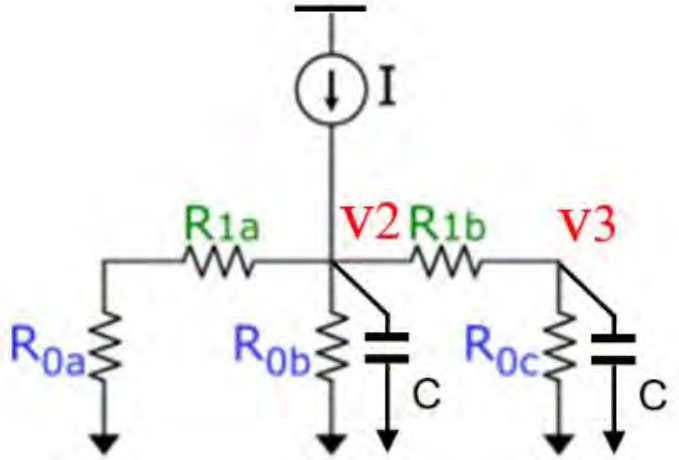
Temporally Unstable

Finding 3

Temporal stability and instability can depend on capacitors (C) from nodes to ground.







$R_{0a} = -1\ k\Omega,\quad R_{0b} = 1\ k\Omega,\quad R_{0c} = 0.5\ k\Omega,\quad R_{1a} = -1\ k\Omega,\quad R_{1b} = 0.5\ k\Omega,\quad I = 10\ \mu A,$

Temporally Unstable | Unstable | Stable

Proved with theory

Finding 4

Spatial stability cannot be defined rigorously for a finite size of the network.

Only spatial dynamics can be discussed.

Our Four New Findings

For general non-uniform active resistor network dynamics,
four new properties have been found
with simulation and theoretical analysis.

Their rigorous proof has NOT been completed yet.

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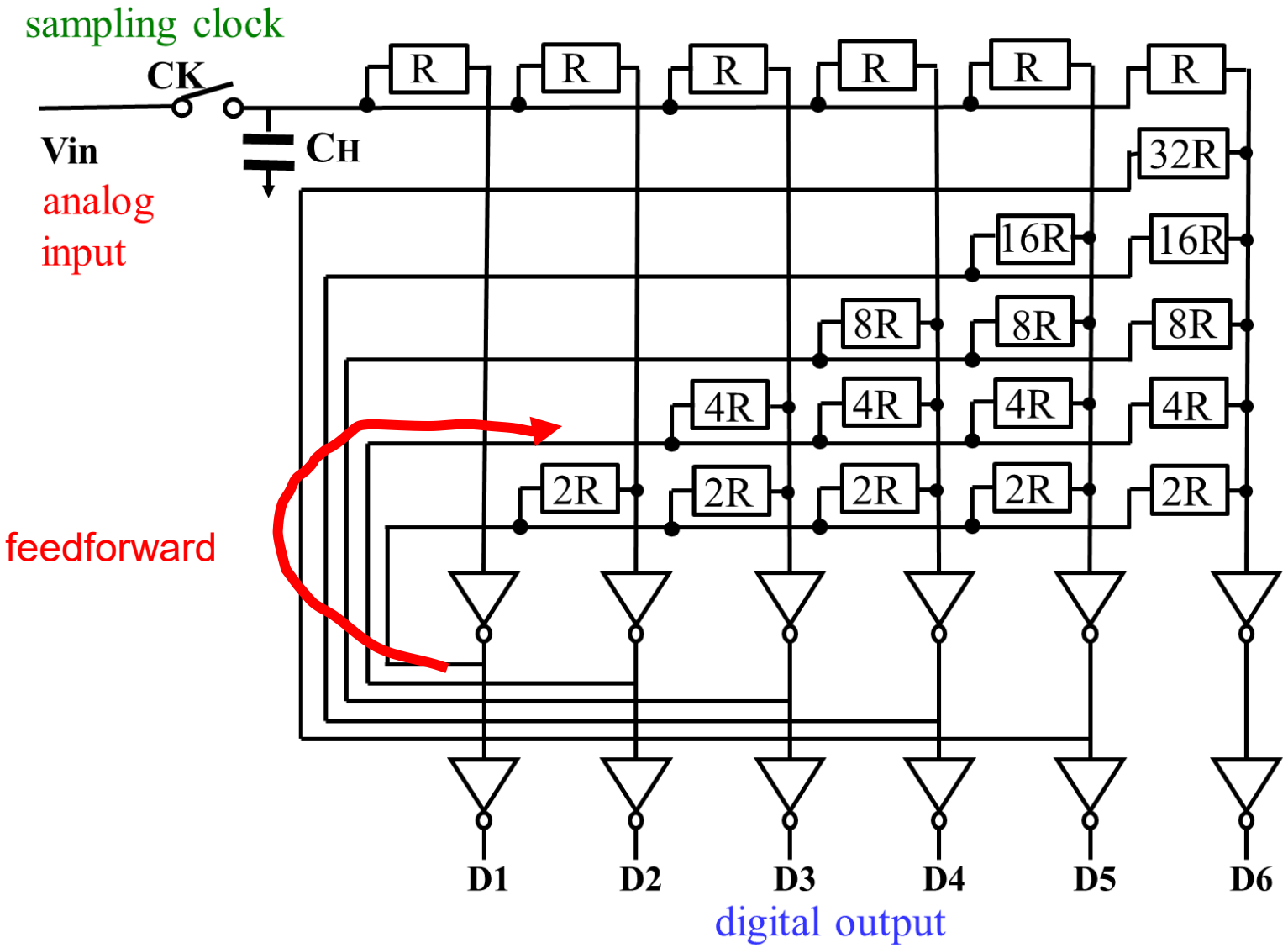
Hopfield Network



Asymmetric Hopfield Network

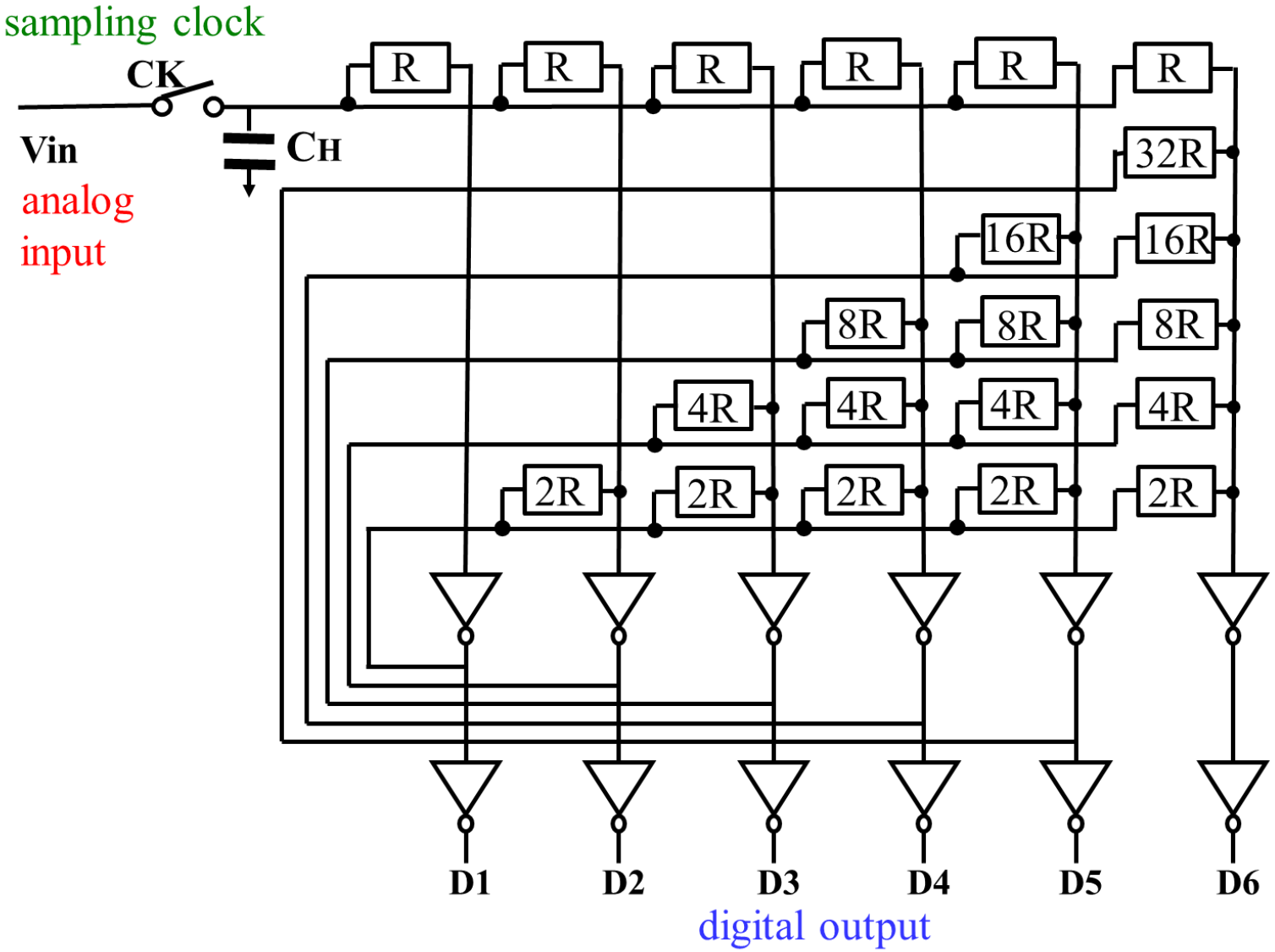
⇩

Only feedforward paths
No feedback paths

⇩

No local minima problem

Hopfield Network ADC with Resistors

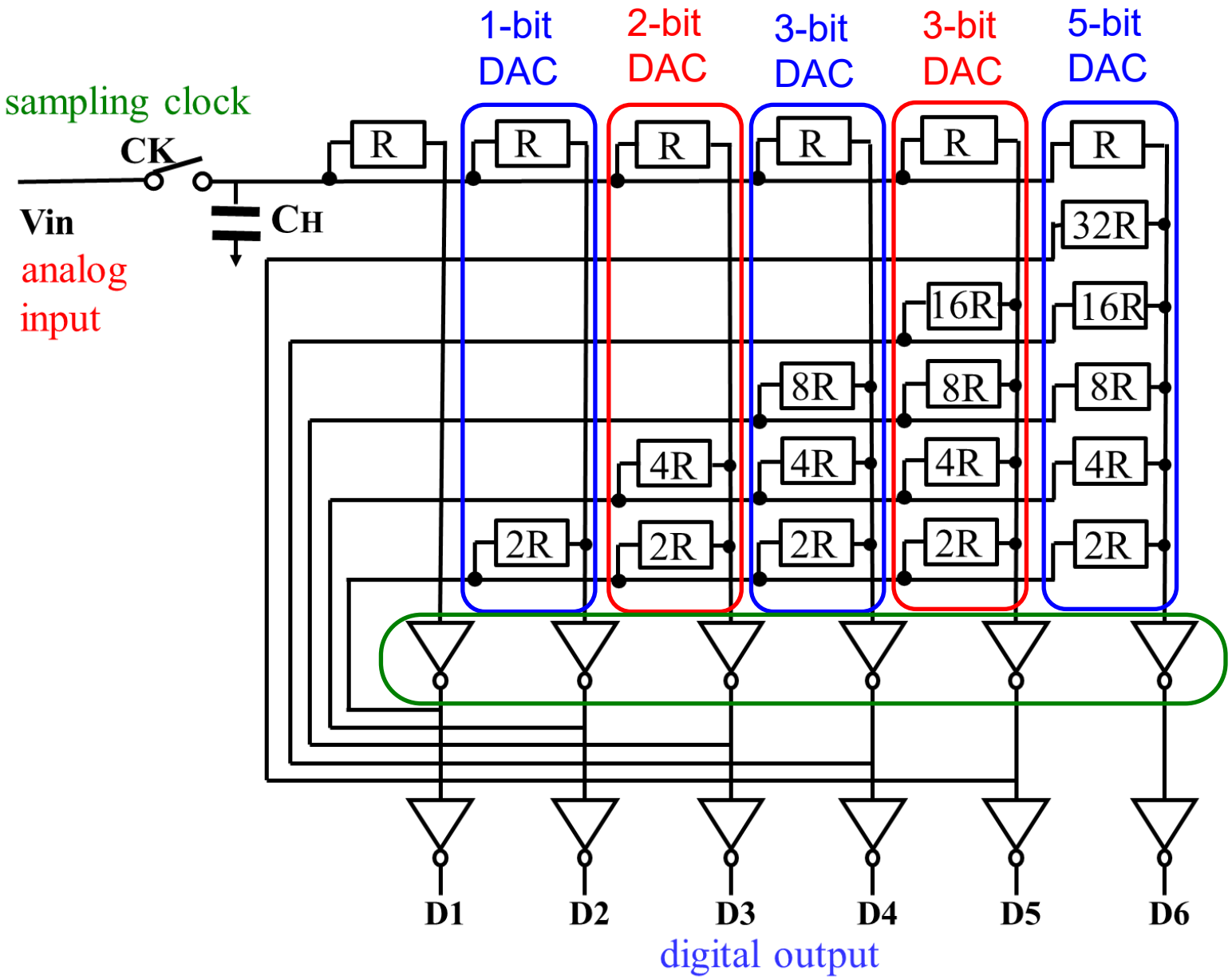


Asynchronous SAR ADC

- Very fast
- No high freq. internal clock
- N(=6) comparators (inverters)
- Huge resistors (Giga Ω-Tera Ω)
  due to inverter poor current drivability

Big disadvantage

Internal Structure of Hopfield Network ADC

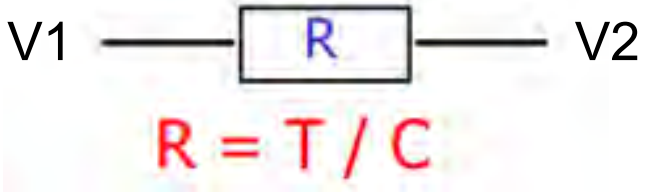


Internal DACs in parallel

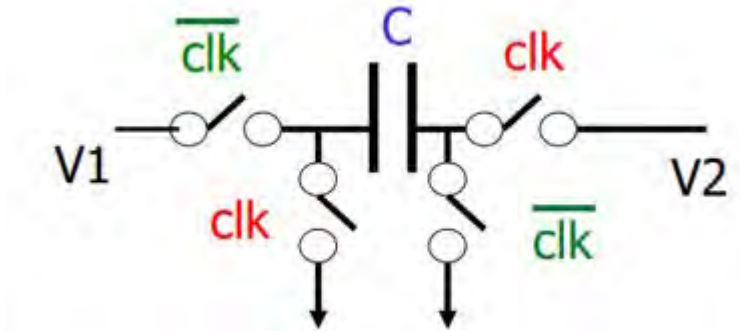
Comparators (inverters) in parallel

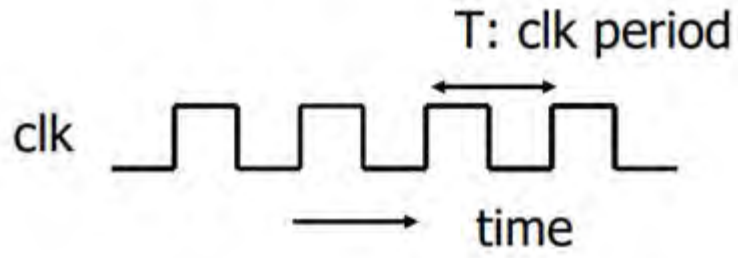
Hopfield Network ADC with Switched Capacitor Circuit

Huge resistor



Replacement



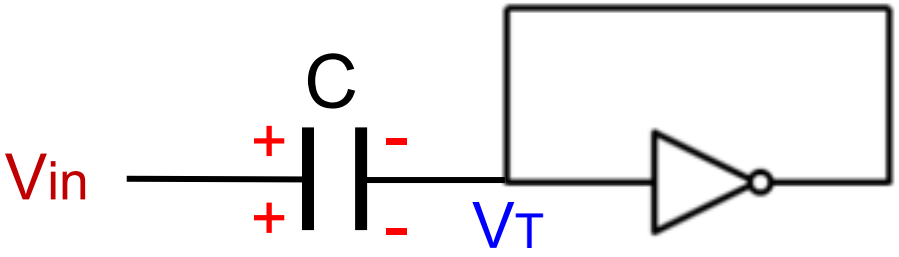


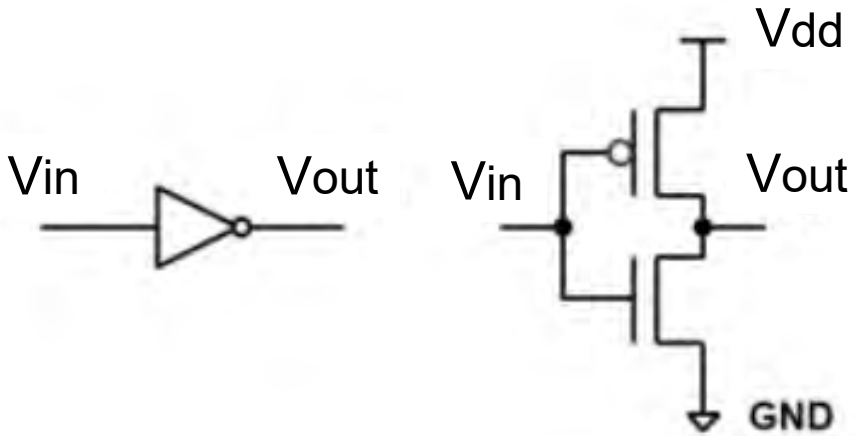
Hopfield Network ADC → Practical

[6] X. Bai, et. al., "Asynchronous Capacitive SAR ADC based on Hopfield Network", IEICE Electronics Express (Sept. 2022)

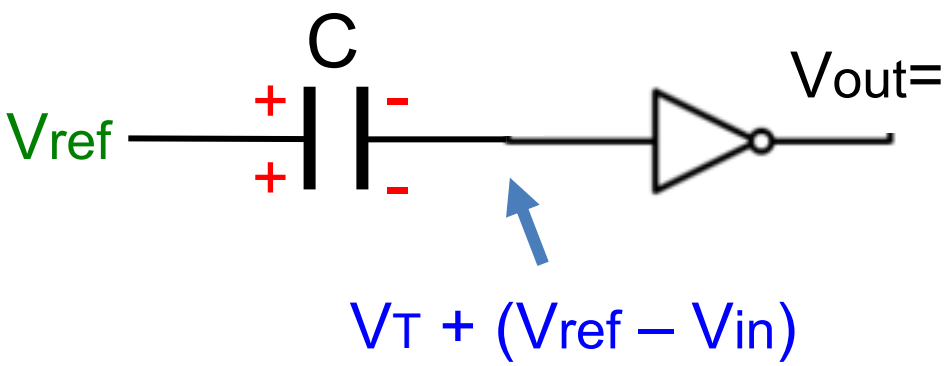
Chopper Comparator Usage

Phase I

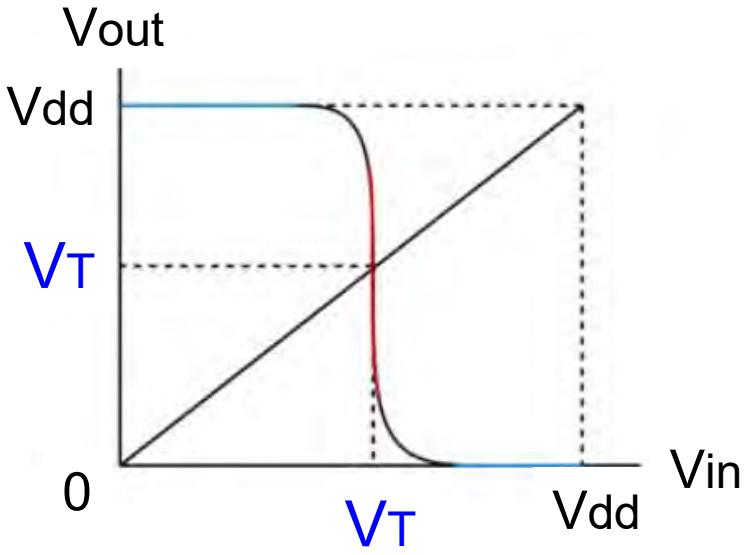




Phase II

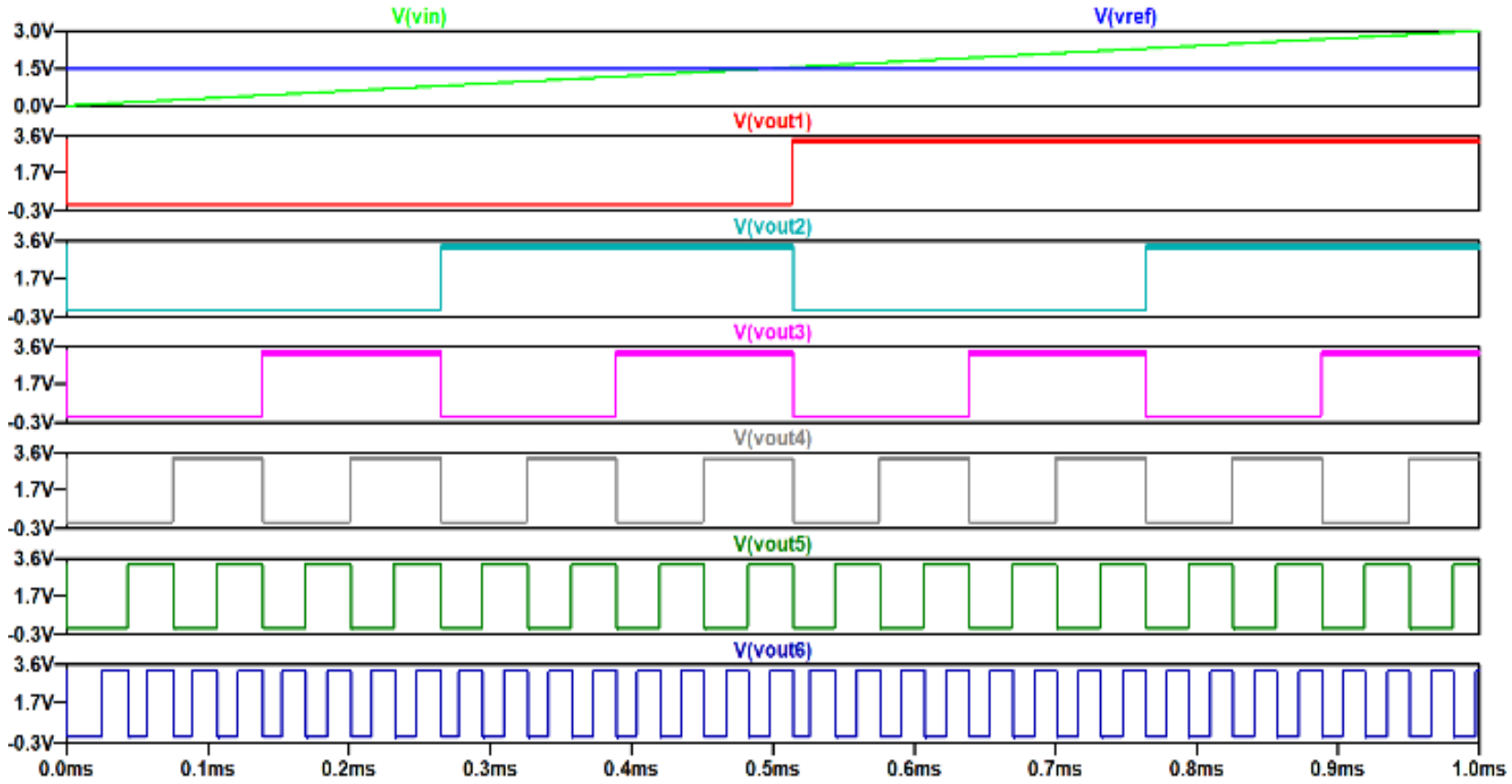


$$V_{out} = \begin{cases} V_{dd} & \text{(in case } V_{ref} < V_{in}\text{)} \\ 0 & \text{(in case } V_{ref} > V_{in}\text{)} \end{cases}$$



- Only digital circuit (inverter, CMOS switch) usage

Simulation Confirmation of Basic Operation



Detailed circuit design is underway

Summary of Hopfield Network ADC

- Asymmetric Hopfield network ADC with resistors works as very fast asynchronous SAR ADC

⇨ Huge resistors are required

- Chip area ⇨ Very big

- Their replacement with switched capacitors

- Chip area ⇨ Modest
- Asynchronous SAR ADC with N comparators in parallel
- Non-binary (redundant) configuration ⇨ Error tolerant for higher bits

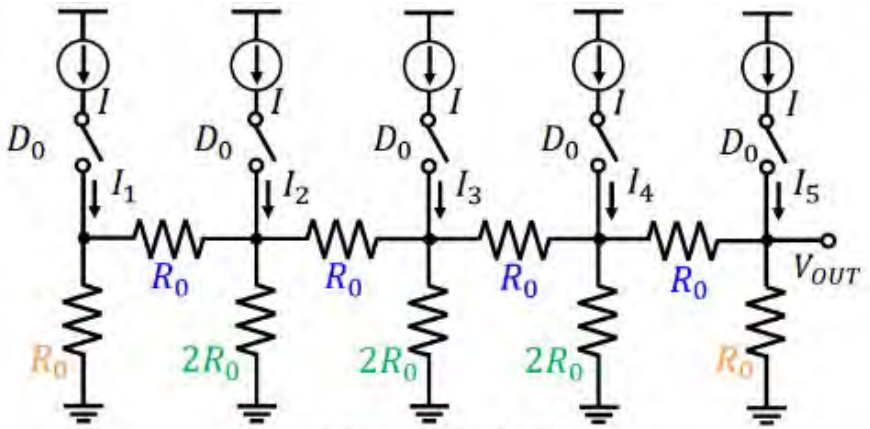
Under investigation

Outline

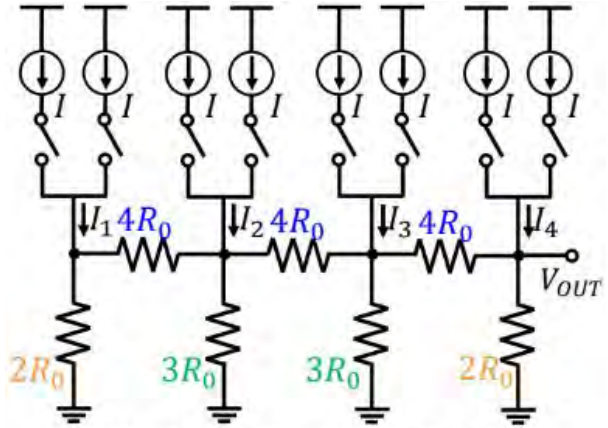
- Objective of This Paper
- Dynamics of Active Resistor Network in Vision Chip
- Switched Capacitor Network ADC
  Inspired by Hopfield Network
- Design and Analysis of Resistor Network DAC
- Conclusion

（1）Generalized Resistor Ladder DAC

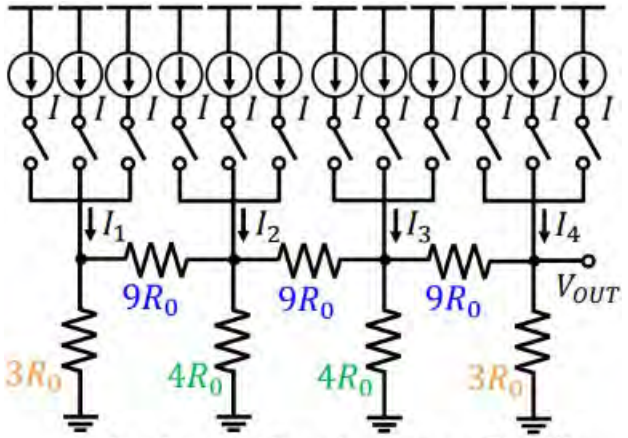
Systematic construction method for general resistor ladder DAC



R-2R DAC



Ternary DAC



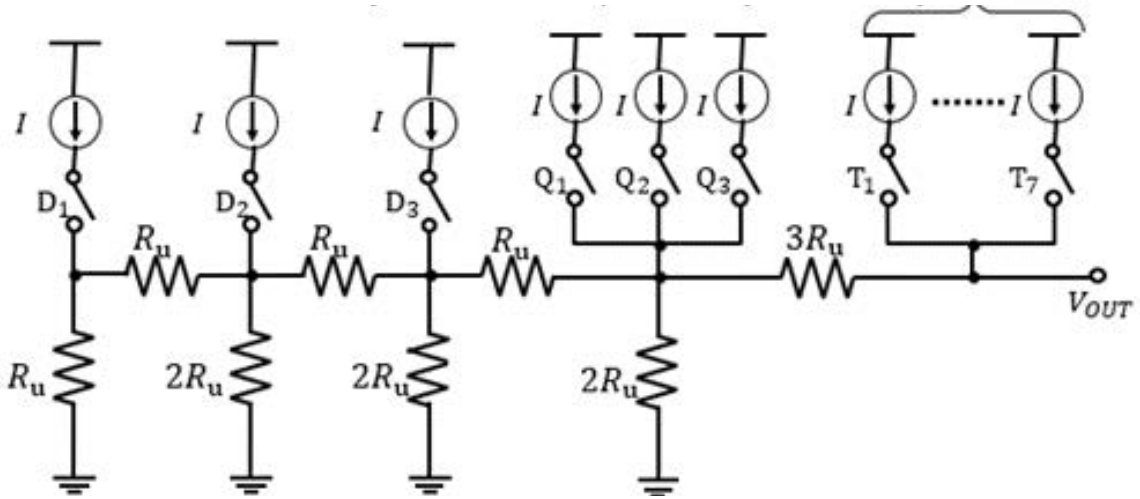
Quaternary DAC

[7] M. Hirai, et. al., "Systematic Construction of Resistor Ladder Network for N-ary DA s,"
IEEE International Conference on ASIC (Oct. 2019)

[8] M. Hirai, et. al.,
"Digital-to-Analog Converter Configuration Based on Non-uniform Current Division Resistive-Ladder,"
International Technical Conference on Circuits/Systems, Computers and Communications (June 2021)

(2) Proposed Resistor Ladder DAC

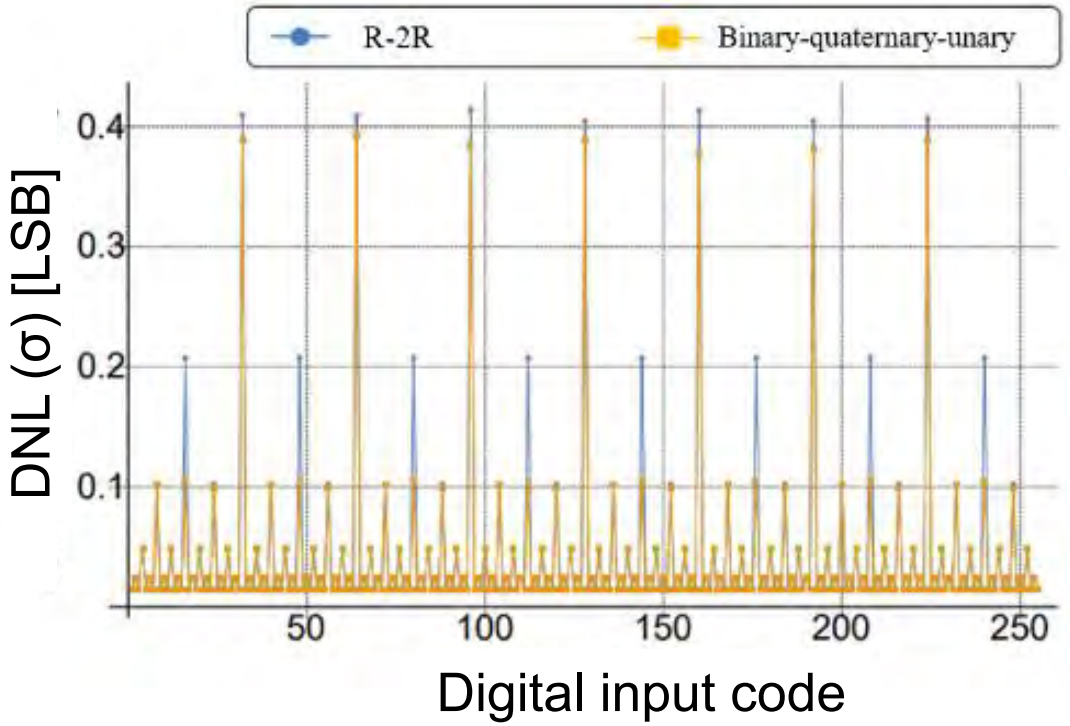
Binary quaternary unary 7



3 lower bits 2 middle bits 3 higher bits

8-bit binary-quaternary-unary connected resistor ladder DAC

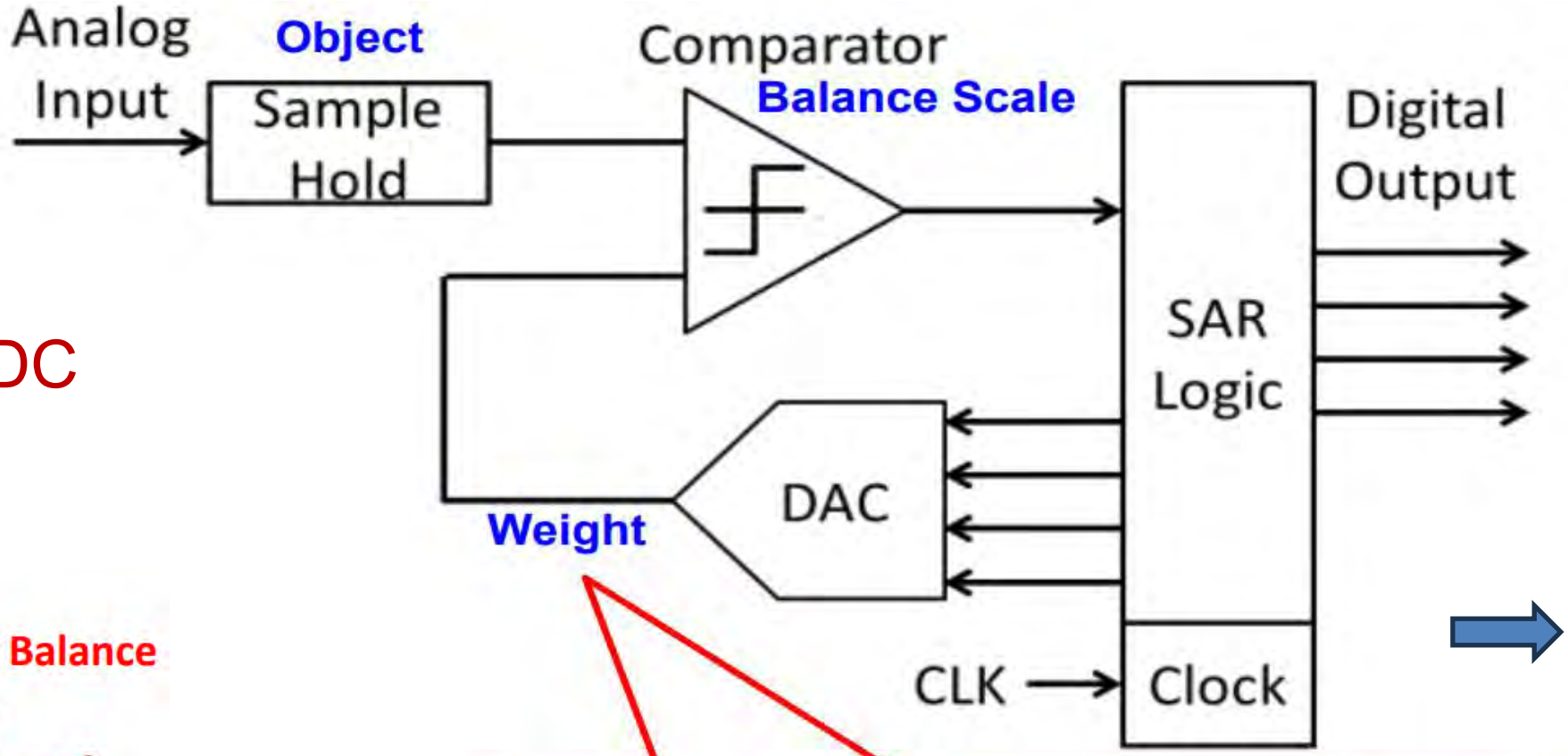
For the same total currents and total resistor values, 2x gain of R-2R DAC



Monte Carlo Simulation Results

For R, I variations, comparable DNL to R-2R DAC

(3) Fibonacci Sequence Weighted DAC



SAR ADC

Based on Principle of Balance

Error tolerant

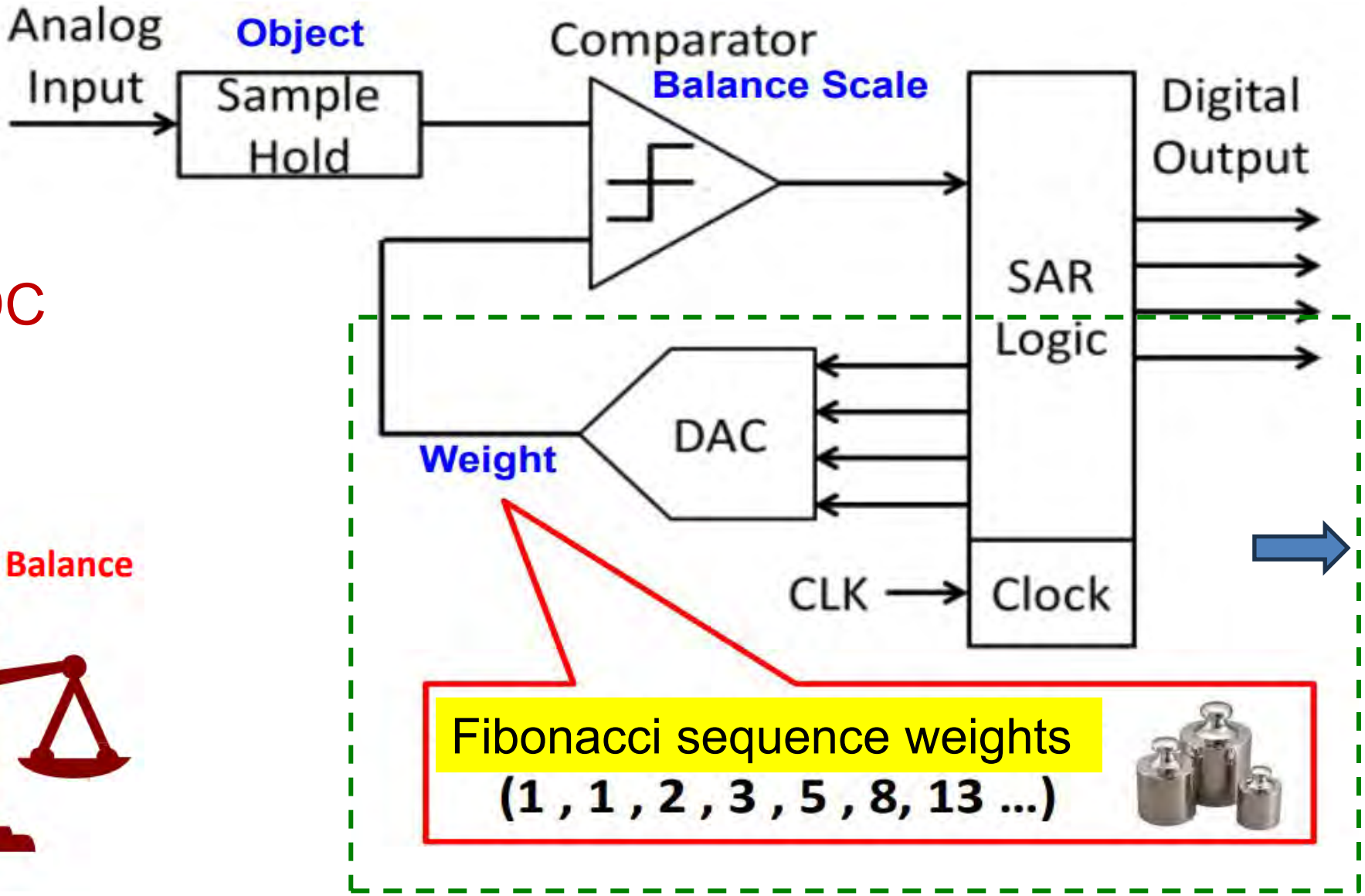
Fibonacci sequence weights

(1 , 1 , 2 , 3 , 5 , 8, 13 …)

Redundancy

Fibonacci Sequence Weighted DAC

SAR ADC



Based on Principle of Balance

Error tolerant

Fibonacci Sequence Number

Fibonacci Definition

$$F_0 = 0$$
$$F_1 = 1$$
$$F_{n+2} = F_n + F_{n+1} \qquad (n=0,1,2\ldots)$$

Example of Fibonacci number

$$0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55 \ldots$$

Leonardo Fibonacci
(Italy:1170-1250)

Property

The closest terms ratio : ***"Golden Ratio"***

(about 1.62 number)

$$\lim_{n\to\infty} \frac{F_n}{F_{n-1}} = 1.618033988749895$$

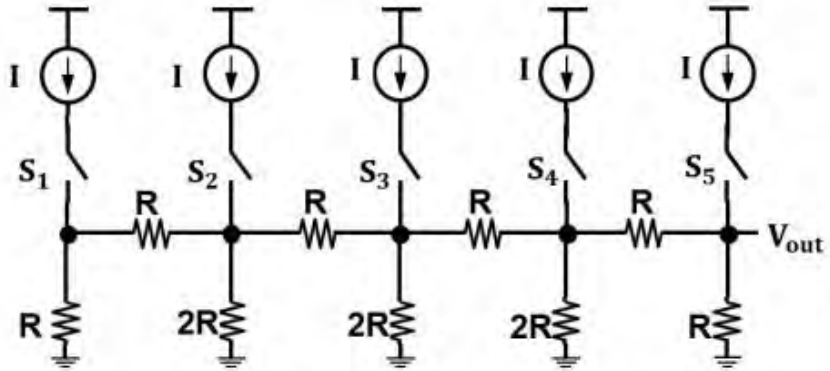
Radix 1.62 weighted DAC

R-R Resistor Ladder

Conventional

R-2R resistor ladder

⇒Generate **binary** voltage



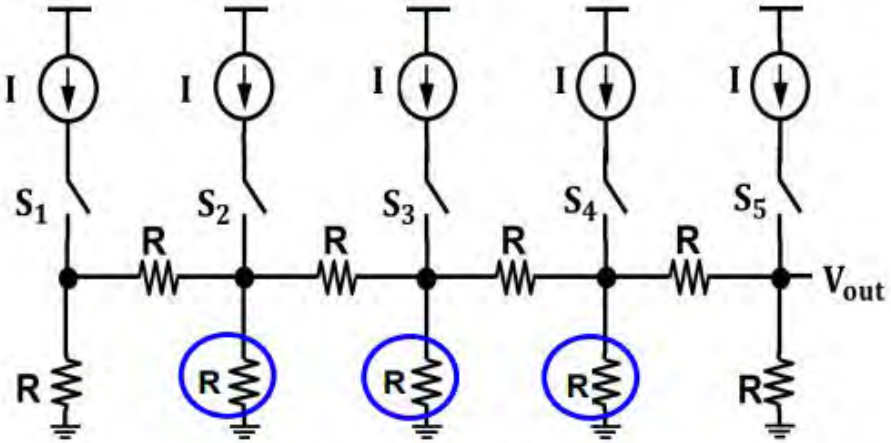
R-2R resistor ladder

Change all resistors to R

Proposal

R-R resistor ladder

⇒Generate **Fibonacci** voltage

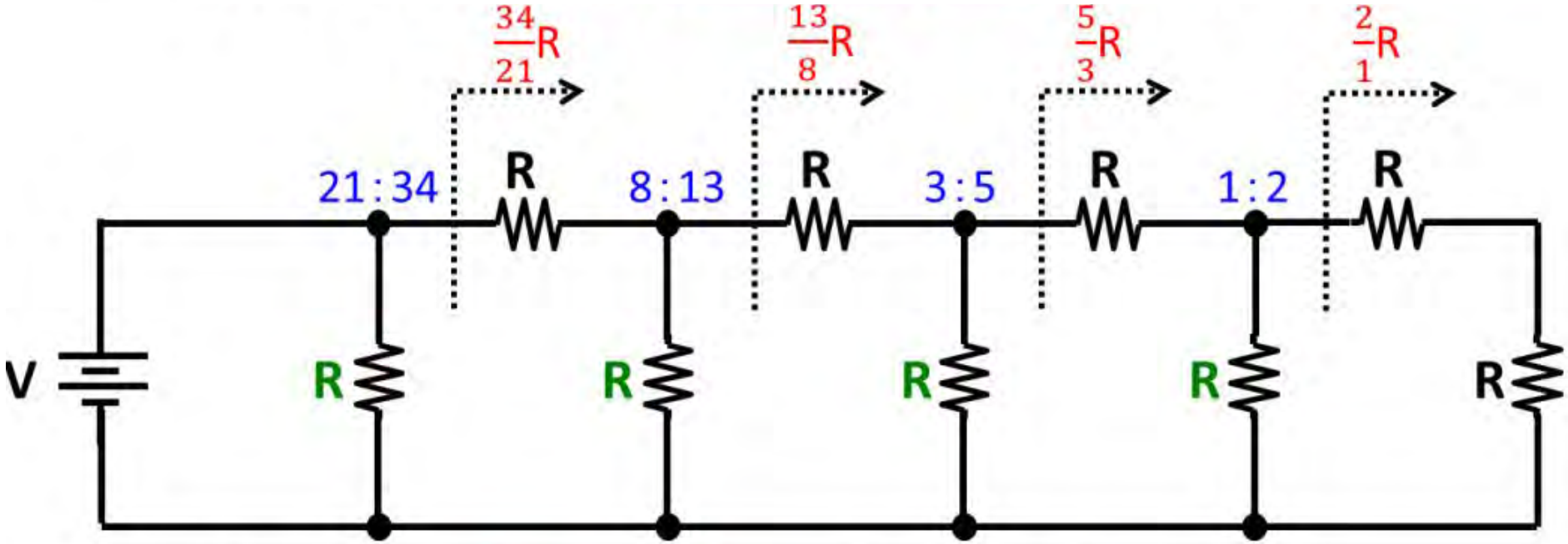


R-R resistor ladder

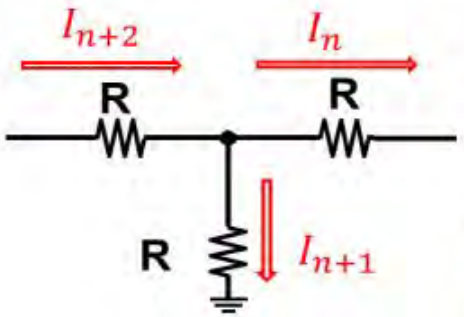
Realize Fibonacci DAC
by using simple circuit !

R-R Resistor Ladder and Fibonacci Ratio

Current division by Fibonacci ratio at each node



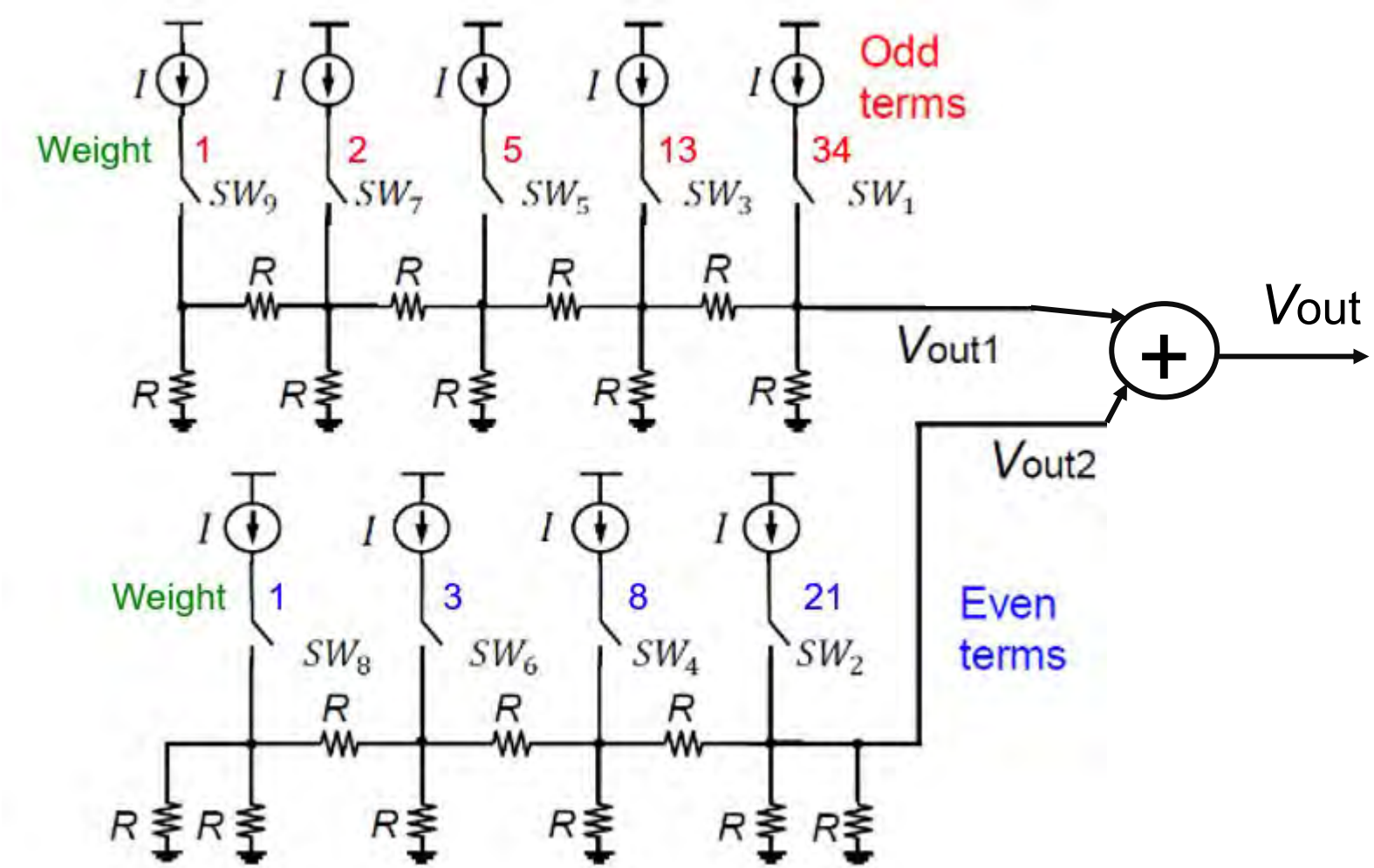
Principle



$$I_{n+2} = I_{n+1} + I_n$$

$$F_{n+2} = F_{n+1} + F_n$$

Fibonacci Sequence Weighted DAC



[9] T. Arafune, et. al., “Fibonacci Sequence Weighted SAR AD Algorithm and its DA Topology,” IEEE International Conference on ASIC (Nov. 2015).

Outline

- Objective of This Paper
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- Switched Capacitor Network ADC
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Conclusion

- Spatial and temporal dynamics of active resistor network in vision chip have close relationships.
- Hopfield Network ADC becomes practical using switched capacitor circuits
- Motivated by the above, new resistive ladder DACs have been investigated.

Legacy analog neural networks can explore new analog circuit.