第８７回FTC研究会（2023年７月１３日、１４日）

7月13日
14:30-14:40　オープニング

セッション１　セーフティ，セキュリティ，国際会議報告
座長　宮瀬紘平（九工大）
14:40-15:15　JR九州熊本総合車両所における新幹線レール振動測定
　〇向井準将，松原重喜，大竹哲史(大分大)
15:15-15:50　論理施錠に対するセンシティビティ攻撃について
　〇松永裕介（九州大）
15:50-16:25　国際会議報告：VTS2023
　〇畠山一実(EVALUTO/日本アクティブキャリア開発)

16:25-16:40　事務連絡

7月14日
セッション２　信頼性関連技法　座長　三宅庸資((株)プリバテック)
9:30-10:05　自己校正・デジタル誤差補正を用いたAD変換器の信頼性評価技術の研究提案
　〇小林春夫（群馬大），加藤健太郎（福岡大）
10:05-10:40　階層化メモリ方式において階層相互間の「相互通信手段によるFTC方式」
　古賀義亮(防衛大 名誉教授)，〇竹之上典昭((株)GSEC/防衛大非常勤講師)

10:40-10:50　休憩

セッション３　テスト技術　座長　吉村正義（京産大）
10:50-11:25　ベイズ深層学習を用いたLSIテスト結果予測
　〇中上輝一，賀川経夫，大竹哲史（大分大），井上美智子（奈良先端大）
11:25-12:00　DART技術を用いた遅延劣化検知の実チップ長期信頼性試験による劣化評価
　〇加藤隆明，三宅庸資，松永恵士，二見治司，麻生正雄（(株)プリバテック）

12:00-12:10　クロージング

自己校正･デジタル誤差補正を用いた AD 変換器の信頼性評価技術の研究提案

○小林 春夫　(群馬大学)
加藤健太郎 (福岡大学)

発表内容

- 問題提起
- ADCのデジタル自己校正技術
- ADCのデジタル誤差補正技術
- 研究提案
- まとめ

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問題意識

微細CMOSでのAD変換器

- デバイス特性のばらつき大　精度確保のため　自己校正
- 速度・信頼性向上のためデジタル誤差補正

↓

Fault　Tolerant なので　内部特性劣化を隠す

信頼性テストが難しい

↓

これらのテスト法を考察する

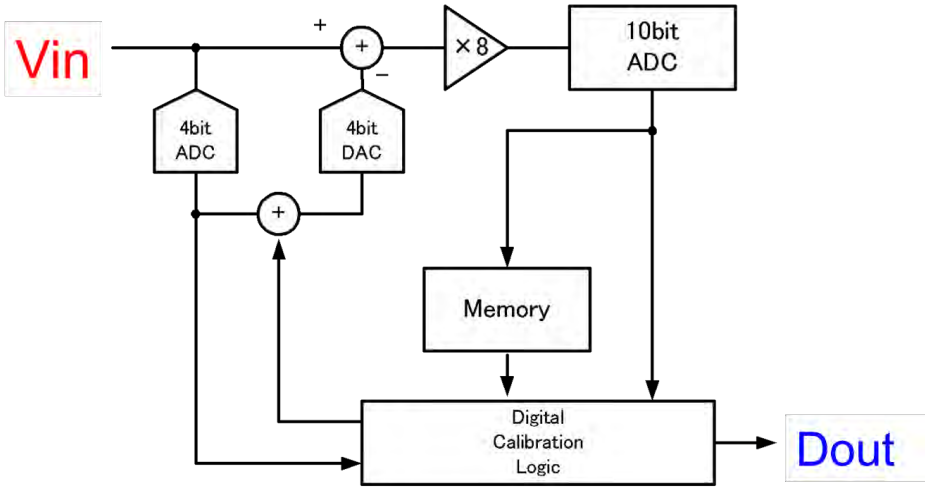
デジタル自己校正と誤差補正

デジタル自己校正

回路の非理想要因をデジタル値として測定

メモリに記憶、

その値をもとに通常動作のときに補正



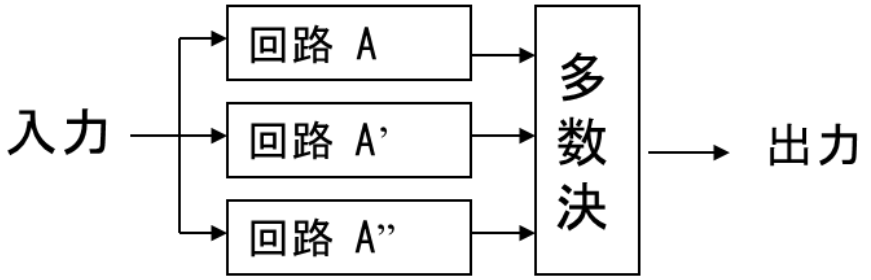
自己校正 ADC 例

デジタル誤差補正

冗長回路をもち、回路の非理想要因を

許容して正解を出力

非理想要因は計測しない。



冗長システム例

電子計測器での校正とADCの自己校正

電子計測器（大きなシステム）の自己校正

通常動作をストップし、自動的に校正を行う

LSIチップ内へ応用

AD変換器の自己校正（チップ内）

フォアグランド自己校正

通常動作をストップして

バックグランド自己校正

通常動作をストップしない

Fault Tolerant 回路のテストは難しくなる

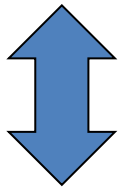
校正

内部特性劣化が生じても自己補正

冗長性

誤動作、故障が起こってもシステム全体は
正常に動作する

Fault Tolerant な回路



異なる思想

LSIテスト

特性劣化、故障がはいらないようにする検査

Fault Tolerant ADC のテストの問題

FT ADC (Fault Tolerant ADC デジタル自己校正・誤差補正 ADC)

➡ 設計パラメータ空間が広くなる

内部に不良箇所があっても　補正され
ADCテスト（出荷検査）の際に「良品」と判定。

その欠陥が補正できるぎりぎり(崖っぷち)のとき、
市場で補正範囲を超え
動作不良となることあり。

崖っぷち

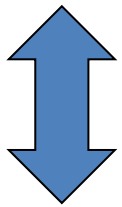
デジタル補正使用の計測器・センサの量産経験者

「高精度な湿度計測を実現するには、
温度係数の個体差のばらつきが小さく、
複雑な温度補正を必要とせず、
調整・校正誤差が小さい特性ばらつきしかない
湿度センサを選定することが重要。」
（田澤R&D技術士事務所　田澤勇夫氏）

「崖っぷち」は避けたい！

工業製品の量産の思想

製品ばらつきを抑える。
「均一な部品・材料を用いて均一な品質なものを作ること」
が重要



異なる思想か？

校正、調整では　ばらつきを許容する。
が、最終製品は特性は均一になる。

アナログの回路とテストの研究の接点

アナログの回路研究者とテスト研究者の学会は別。

⇒ 両者の交流は限定

「アナログ回路の自動調整、自己校正は
回路技術とテスト技術の接点である」
(Prof. A. Chatterjee, ジョージア工科大学)

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パイプラインADCの背景

- パイプラインADCの位置づけ

  CMOS ADCで高分解能、中高速で
  有力なアーキテクチャ。
  産業界で広く用いられている。

- ナノCMOSでの実現

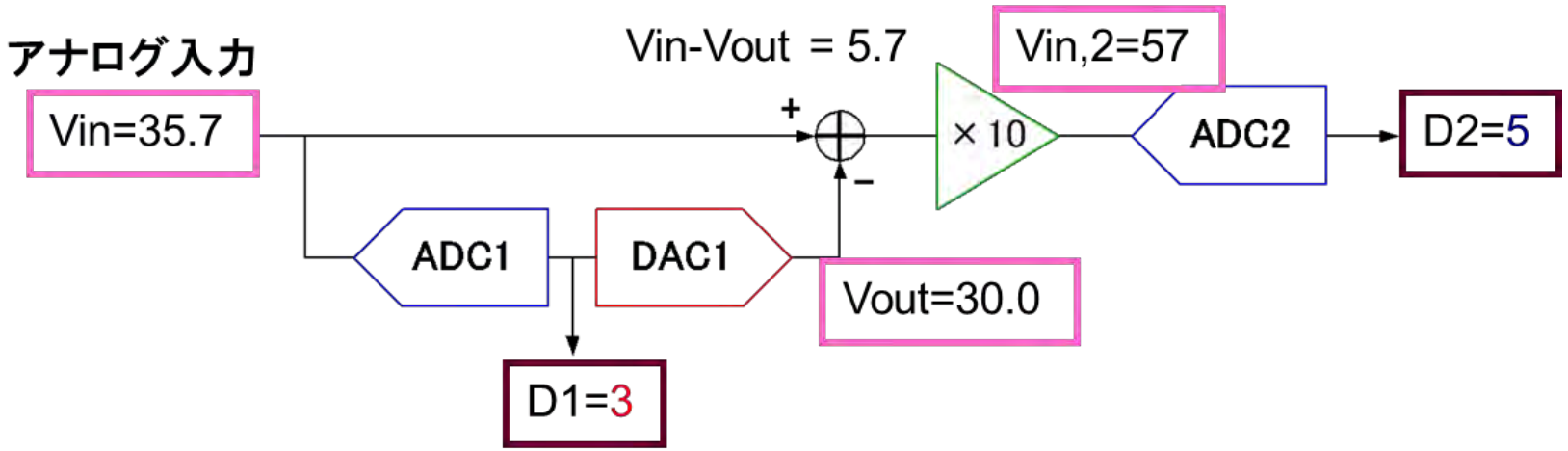
  ミスマッチによる精度劣化、
  オペアンプのゲインを得るのが難しい
  高精度化が難しい

パイプラインADCの高性能化

計測制御技術による

自己校正技術

- 内部回路（DA変換器、利得アンプ）の
  不正確さを計測して、
  その値をテーブルに記憶。
  デジタル演算で補正。
- 誤差計測回路は
  パイプラインADC自体を用いる。



パイプライン

⇩

バケツリレー

ADC1

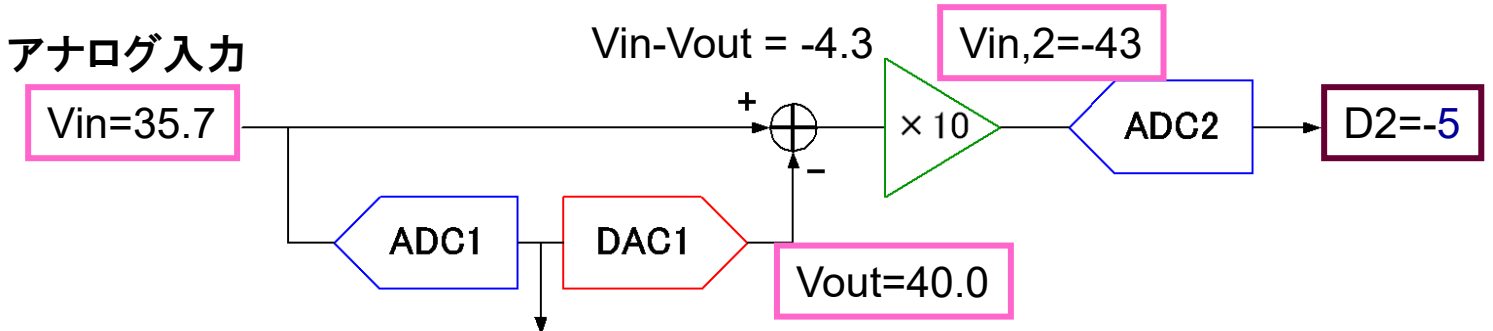
入力Vin	出力D1
30.0≦ Vin ＜40.0	3

ADC2

入力Vin,2	出力D2
50.0≦ Vin,2 ＜60.0	5

出力 Dout=3 × 10+5=35

ADC1 出力が不正解でもOK



不正解出力

ADC1

入力Vin	出力D1
40.0≦ Vin ＜50.0	3

ADC2

入力Vin,2	出力D2
-50.0 ≦ Vin,2 ＜-40.0	-5

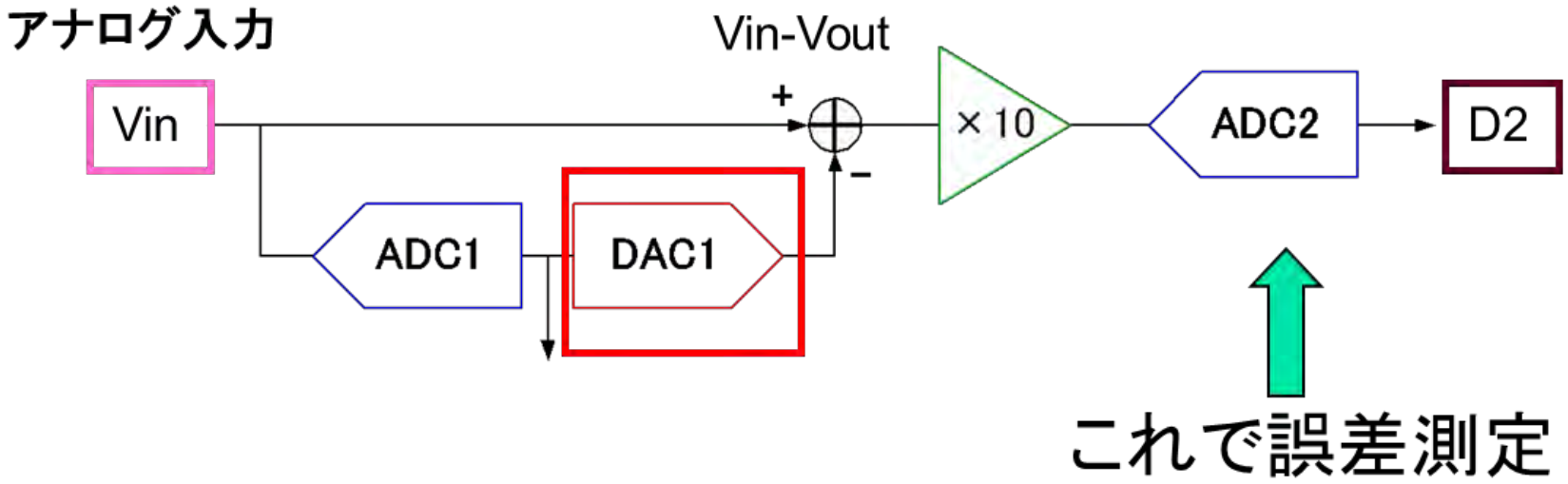
出力 Dout=4×10-5=35

ADC全体の出力は正しい

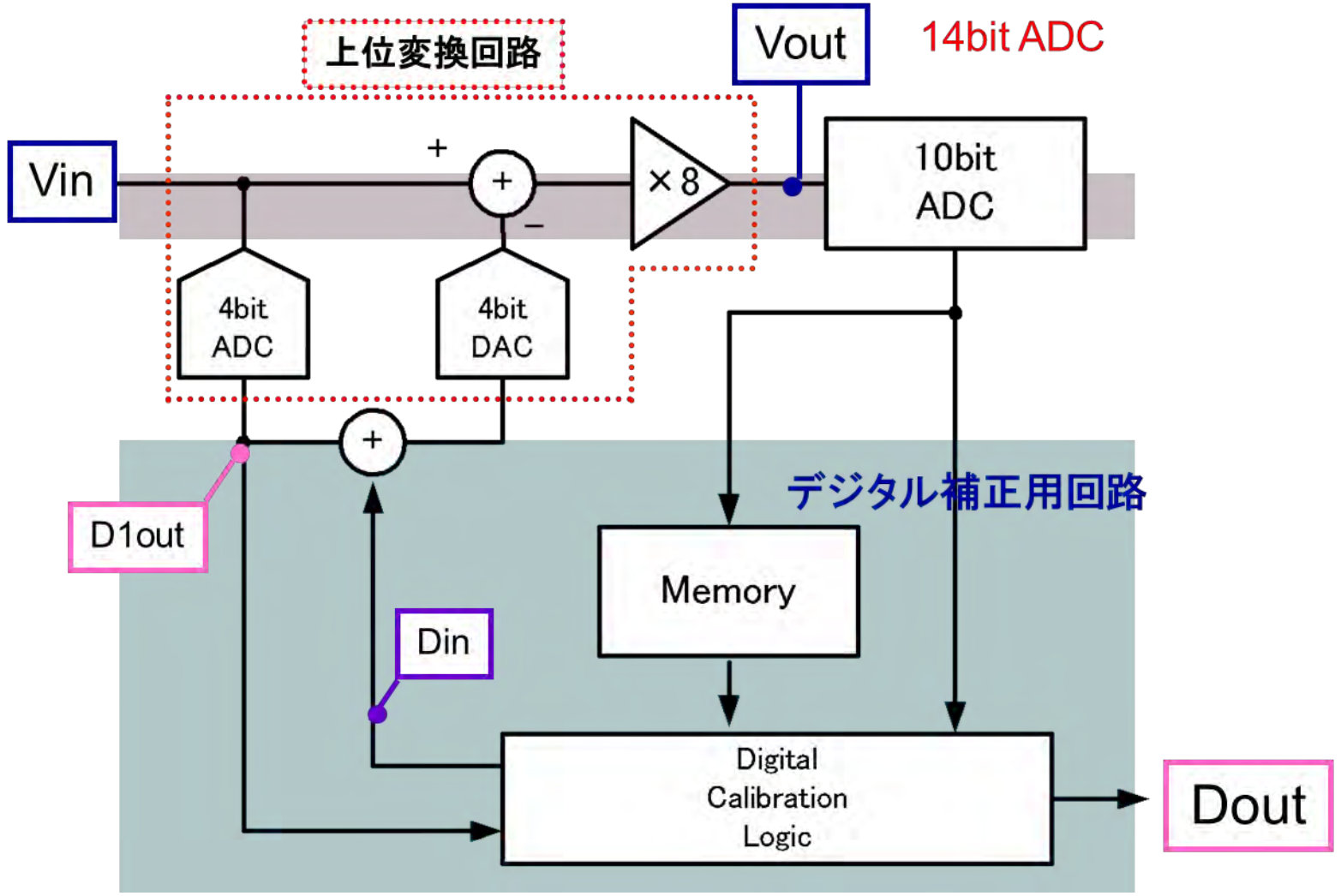
パイプラインADC全体の精度劣化要因

ADC1の非線形性の影響　　問題　小

DACの非線形性の影響　　問題　大

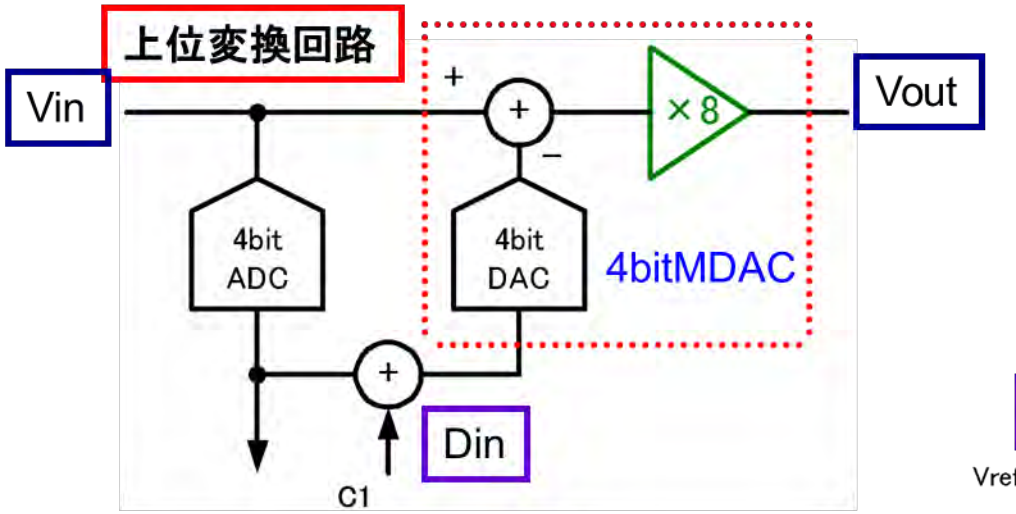


自己校正回路パイプラインADC全体回路

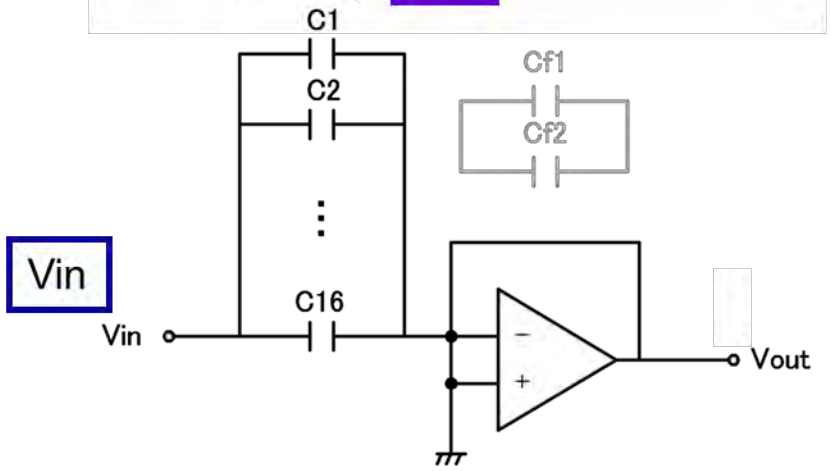


マルチプライDACのゲイン・非線形性測定

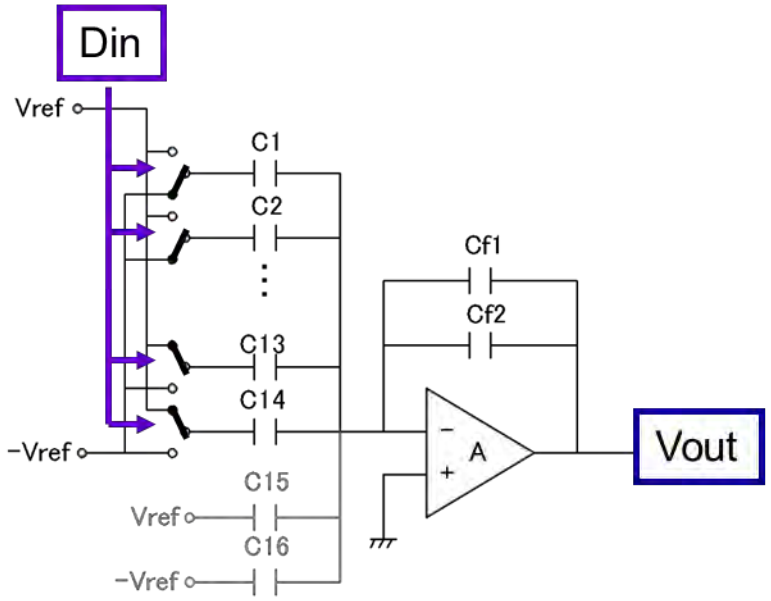
内部の容量を後段ADCで測定



$$Vout = 8\left(Vin - [D1+D2+\cdots+D14]\frac{Vref}{16}\right)$$



Sampling phase

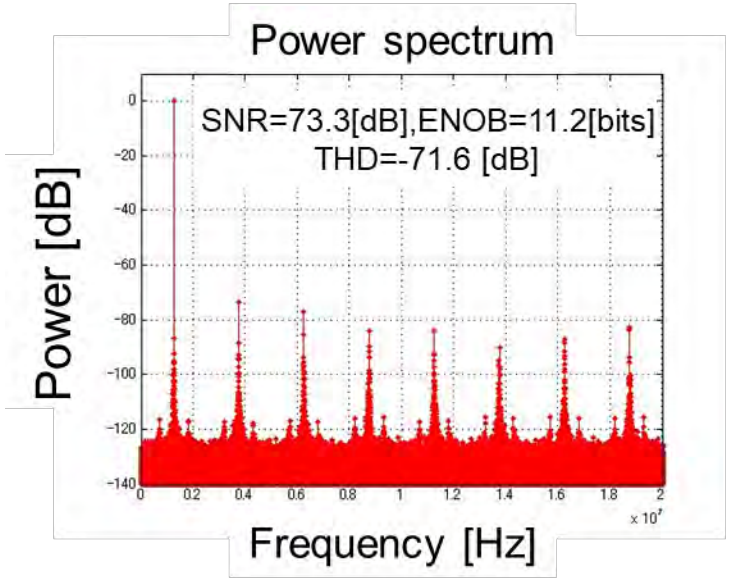


Hold phase

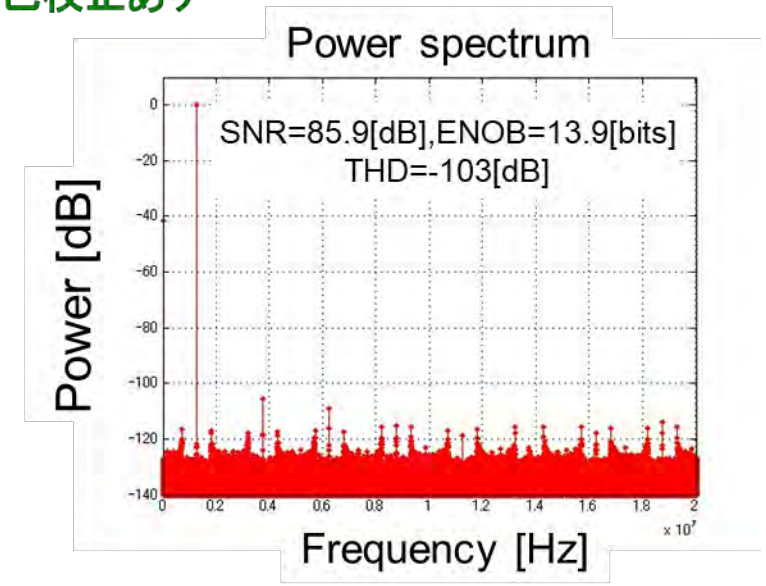
自己校正シミュレーション結果

単一正弦波入力の出力パワースペクトル

自己校正なし



自己校正あり



SNDR 12.7dB (有効ビット2.7bits) 向上

実測でも検証

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冗長性を用いたADC設計

ADC 内に 冗長性

↓

各回路構成要素への要求が緩和

↓

性能向上を達成

時間の冗長性

１人の人が、間違いなく　休みもとらずにやれば

６時間で終わる仕事

　　７時間を割り当てる。

➡途中で間違えても修正・回復できる。

➡適度に休息をとり　余裕をもって確実に

　　仕事を完了させることができる。

長い間には効率的。短い時間で大プロジェクトが完了できる。

ADCアーキテクチャ例：　冗長アルゴリズムSAR ADC

[1] T. Ogawa　et. al., “SAR ADC Algorithm with Redundancy and Digital Error Correction”,　IEICE Trans. Fundamentals (Feb. 2010).

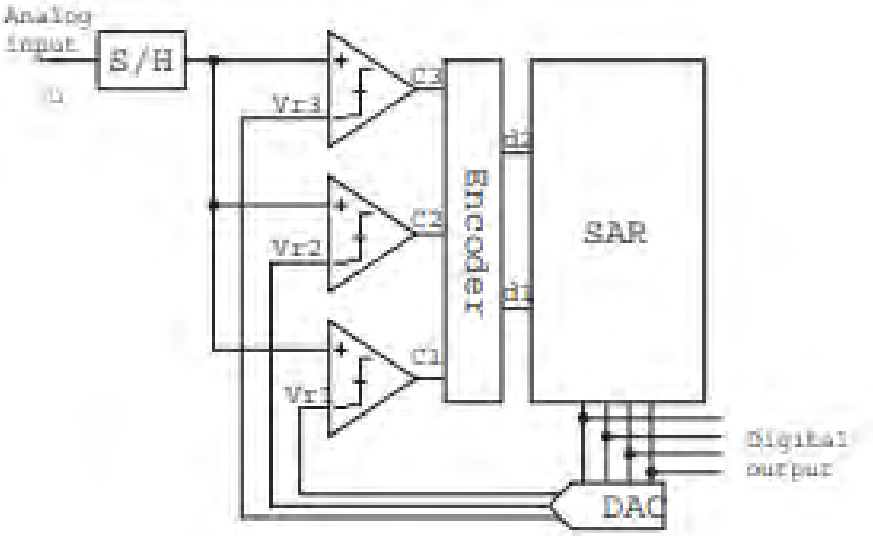
空間の冗長性

５人で7時間で終わる仕事に

６人を7時間で割り当てる。

➡ 休息をとれる。一人が風邪で休んでも
一人が間違えても周りが助ける。

➡ 各自の負担が大幅に軽減でき、
長期的には効率がよい。



対応するADCアーキテクチャ例： ３つの比較器を使用するSAR ADC

[3] M.Hotta, “SAR ADC Architecture with Digital Error Correction”,
IEEJ Transactions on Electrical and Electronic Engineering (Nov. 2010).

冗長性によるデジタル誤差補正

- 空間の冗長性と時間の冗長性
- 回路の非理想要因を許容して正解を出力。
- 非理想要因は計測しない。
- デジタル誤差補正技術により
  - 高信頼性化
  - 高速化
- ここで紹介するのは
  時間の冗長性を用いた
  逐次比較近似ADC

逐次比較近似AD変換器の背景

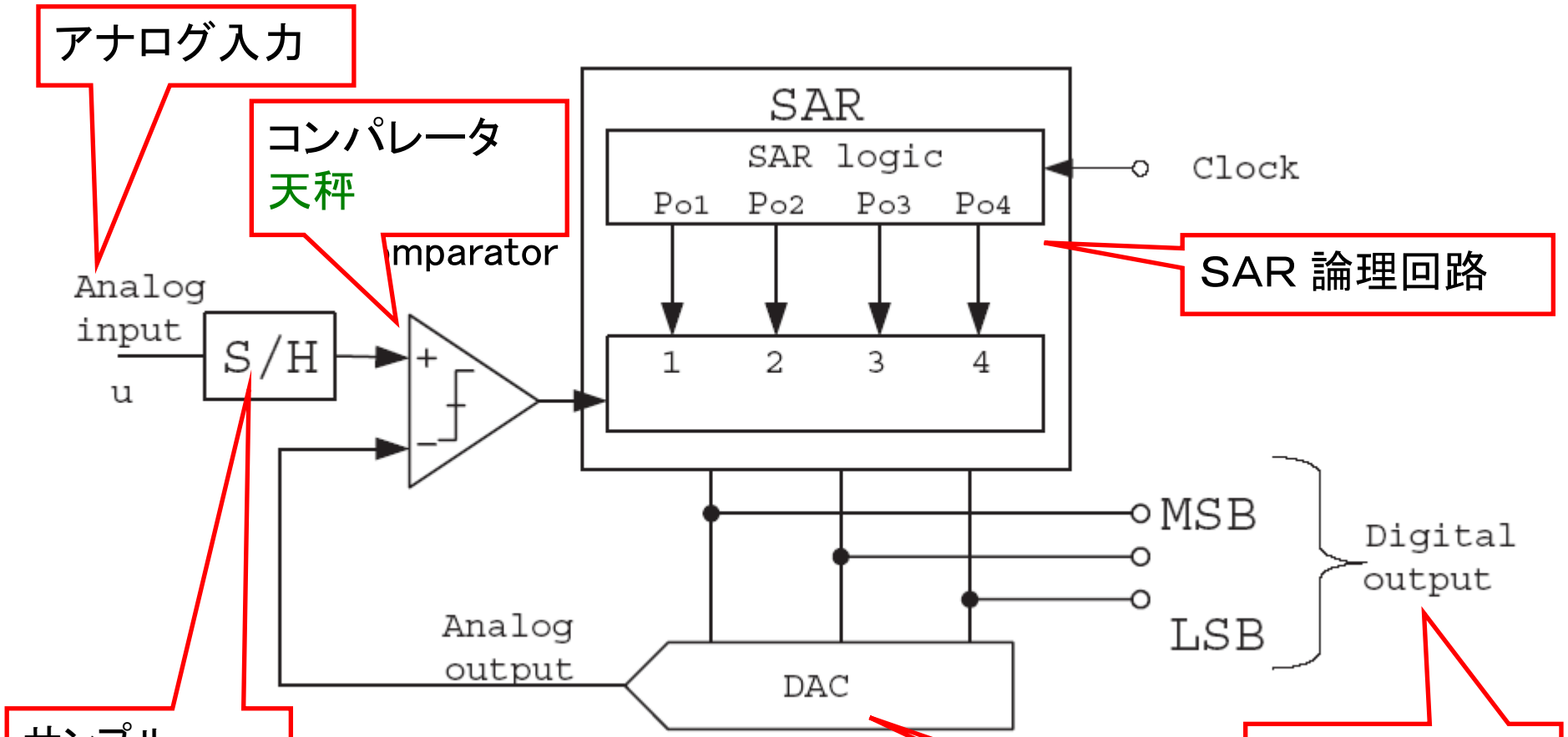
- 高分解能
- 中速
- 低消費電力
- 小型・小チップ面積

産業界で広く使用

- 車載用マイコンに混載
- ペンデジタイザ
- 工業用制御機器

- 大部分がデジタル回路で構成
  ナノＣＭＯＳでの実現に適す

逐次比較近似ADCの構成と動作



アナログ入力

コンパレータ
天秤

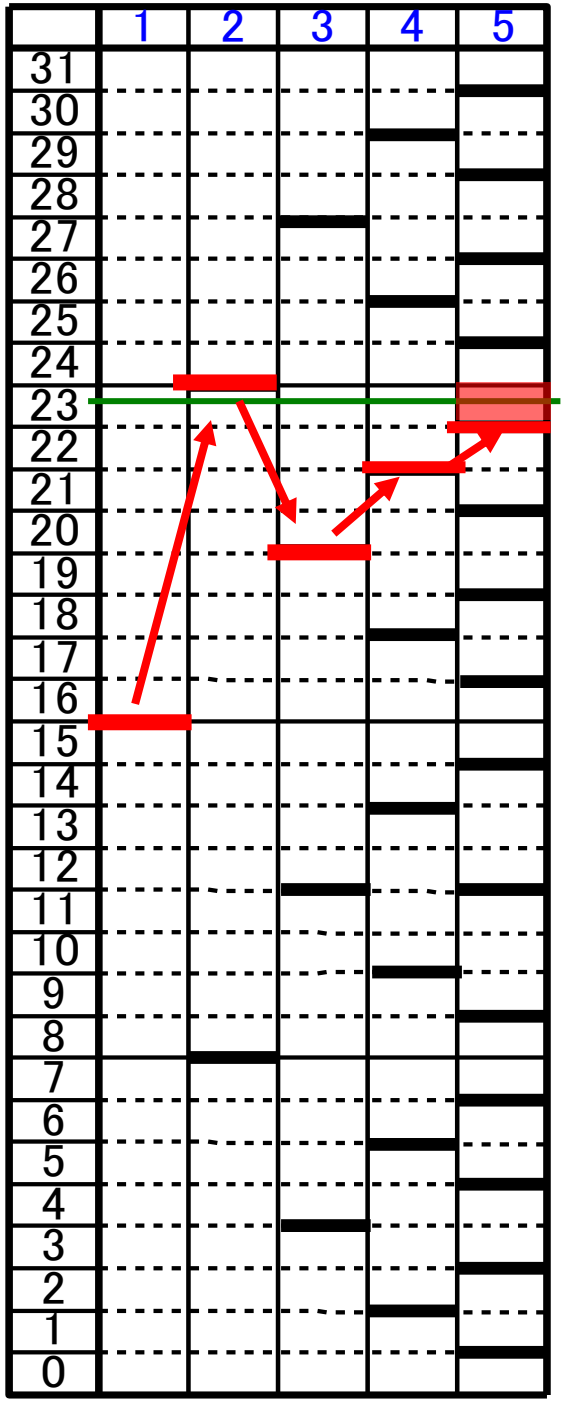
SAR 論理回路

サンプル
ホールド回路

天秤の原理で動作
天秤がコンパレータ
分銅がDAC

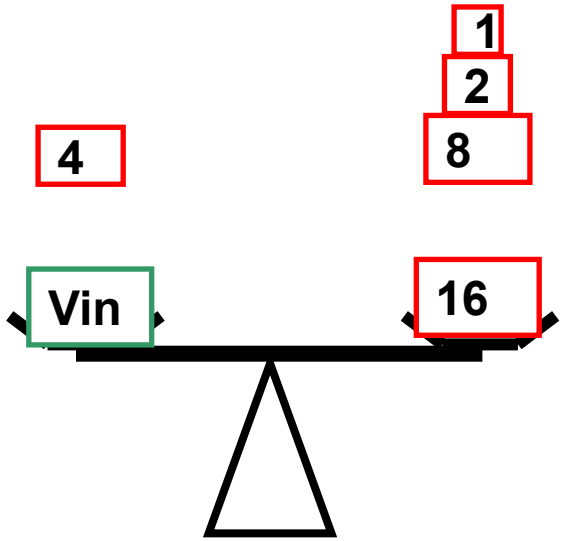
デジタル出力

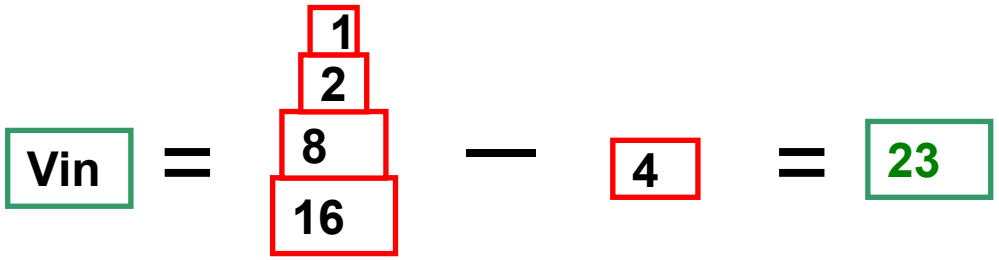
DA変換器
分銅



5ビット　逐次比較近似ADC
2進探索アルゴリズム動作

動作例：アナログ入力　23.5のとき





2進探索アルゴリズム
コンパレータ誤判定時の動作

Vin=23.5　動作例：アナログ入力　23.5のとき

1ステップ目で誤判定したとき

誤差大

デジタル出力15

Vref(1)=16

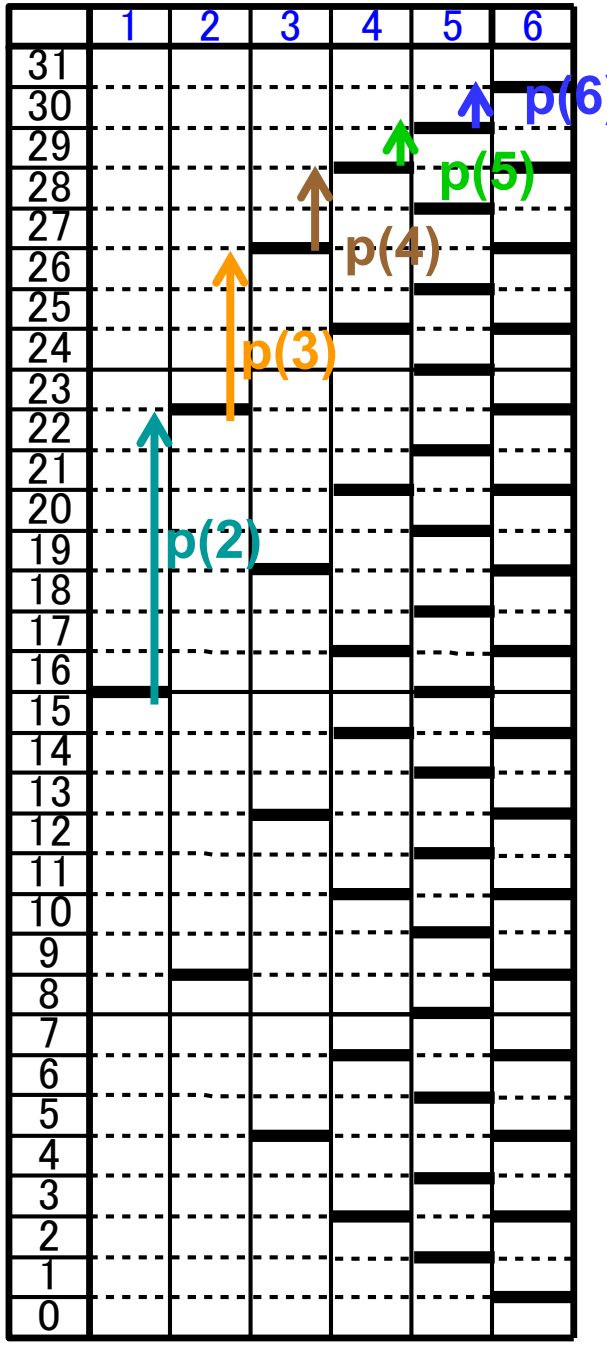
Vref(2)=8

Vref(3)=12

Vref(4)=14

Vref(5)=15

デジタル出力　15



非2進探索アルゴリズム

5ビット分解能(32レベル)

6ステップ(k=1,…,6)の場合

p(2)=7

p(3)=4

p(4)=2

p(5)=1

p(6)=1

分銅の重さに対応

と設計する。

$2^{5-1}=1+p(2)+p(3)+p(4)+p(5)+p(6)$

$2^4=1+7+4+2+1+1=16$

$$2^{N-1}=1+\sum_{i=2}^{M}p(i)$$

を満たしている

非2進探索 冗長アルゴリズム

kステップ目の判定　d(k) ：+1　or　-1

2進探索アルゴリズム
$Dout=2^4+d(1)2^3+d(2)2^2+d(3)2^1+d(4)+d(5)0.5-0.5$

非2進アルゴリズム：5ビット分解能を6ステップで実現。

従来の非2進探索アルゴリズム
$Dout=2^4+d(1)\gamma^4+d(2)\gamma^3+d(3)\gamma^2+d(4)\gamma^1+d(5)+d(6)0.5-0.5$
$1<\gamma<2$
アルゴリズムが一意的に決まる。

$$\gamma = 2^{\frac{5}{6}}$$

非2進探索アルゴリズムの一般化
$Dout=2^4+d(1)p(2)+d(2)p(3)+d(3)p(4)+d(4)p(5)+d(5)p(6)+d(6)0.5-0.5$
p(k)を自由に決める。　　p(k):分銅の重さ

非2進探索アルゴリズムのデジタル誤差補正原理

入力5のとき

2進探索

判定出力 :101

$Dout = 4 + 2 - 1 + 0.5 - 0.5 = 5$

非2進探索

2通り

判定出力 :1101

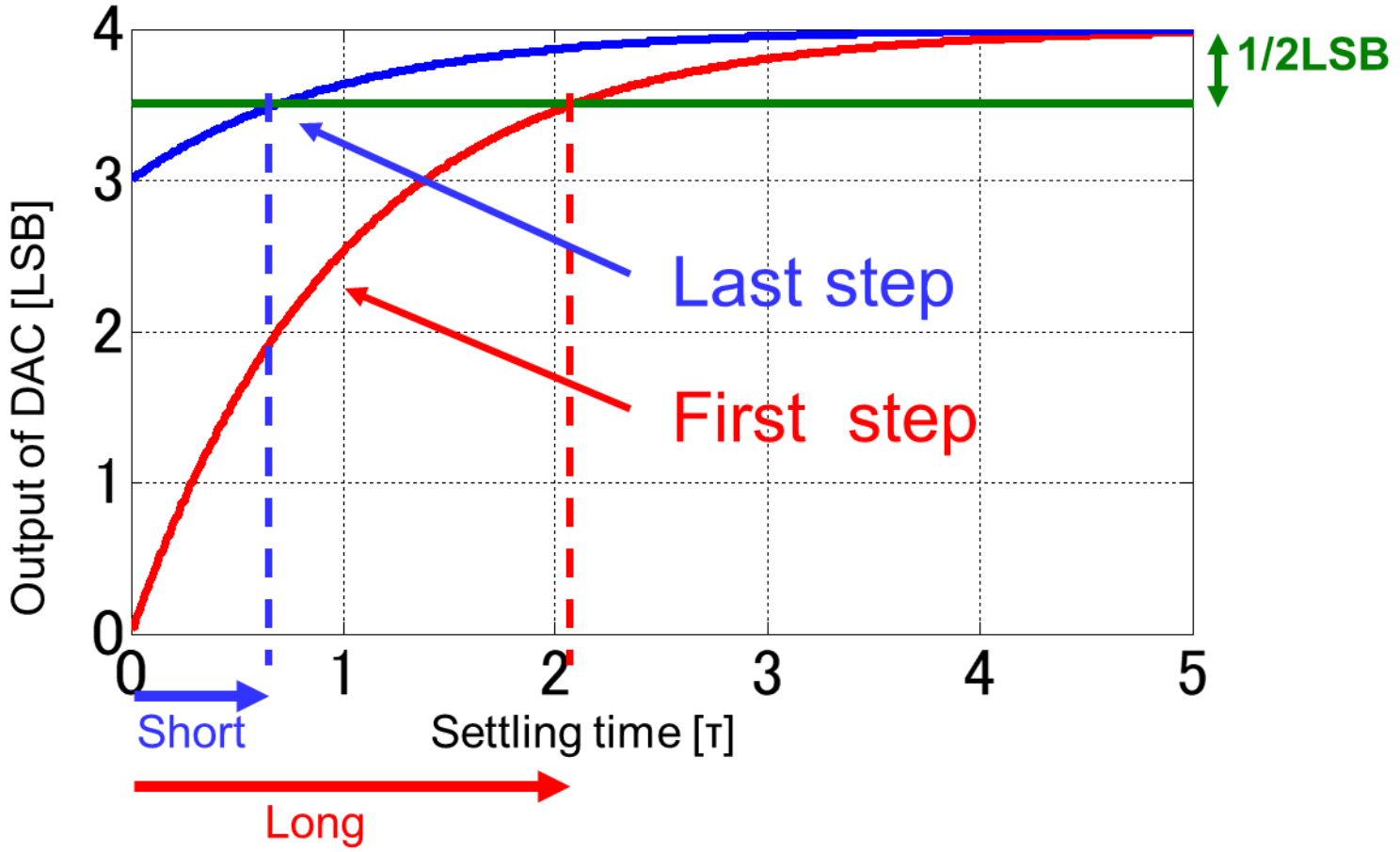
$Dout = 4 + 1 + 1 - 1 + 0.5 - 0.5 = 5$

判定出力 :0111

$Dout = 4 - 1 + 1 + 1 + 0.5 - 0.5 = 5$

1ステップ目で判定誤りをしても補正できる

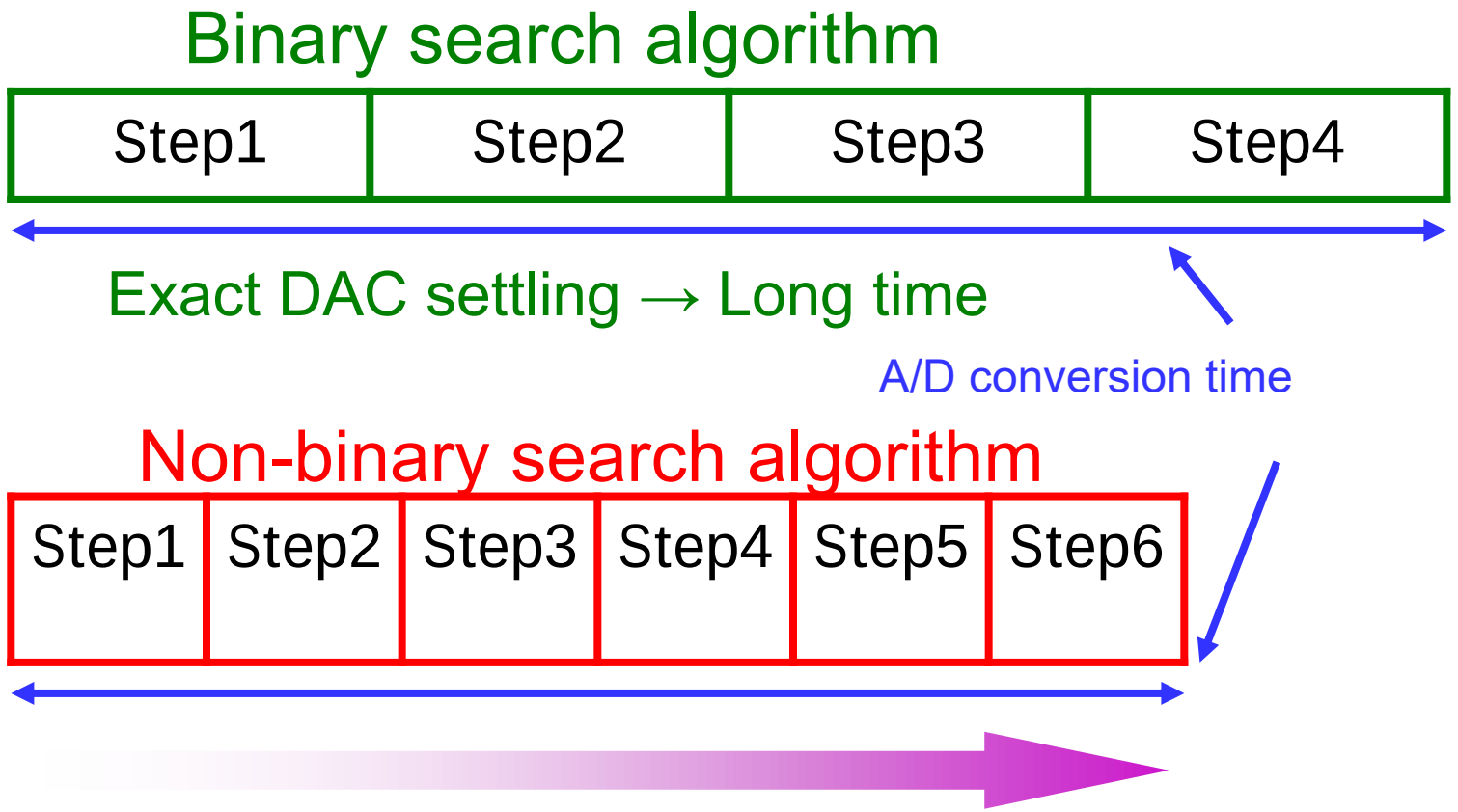
参照電圧発生用の内部DA変換器の整定時間



最悪ケースで
最初のステップでは
要求されるDA変換器
整定時間が長い

非2進探索アルゴリズムによるAD変換 高速化

冗長による高速化
原理説明

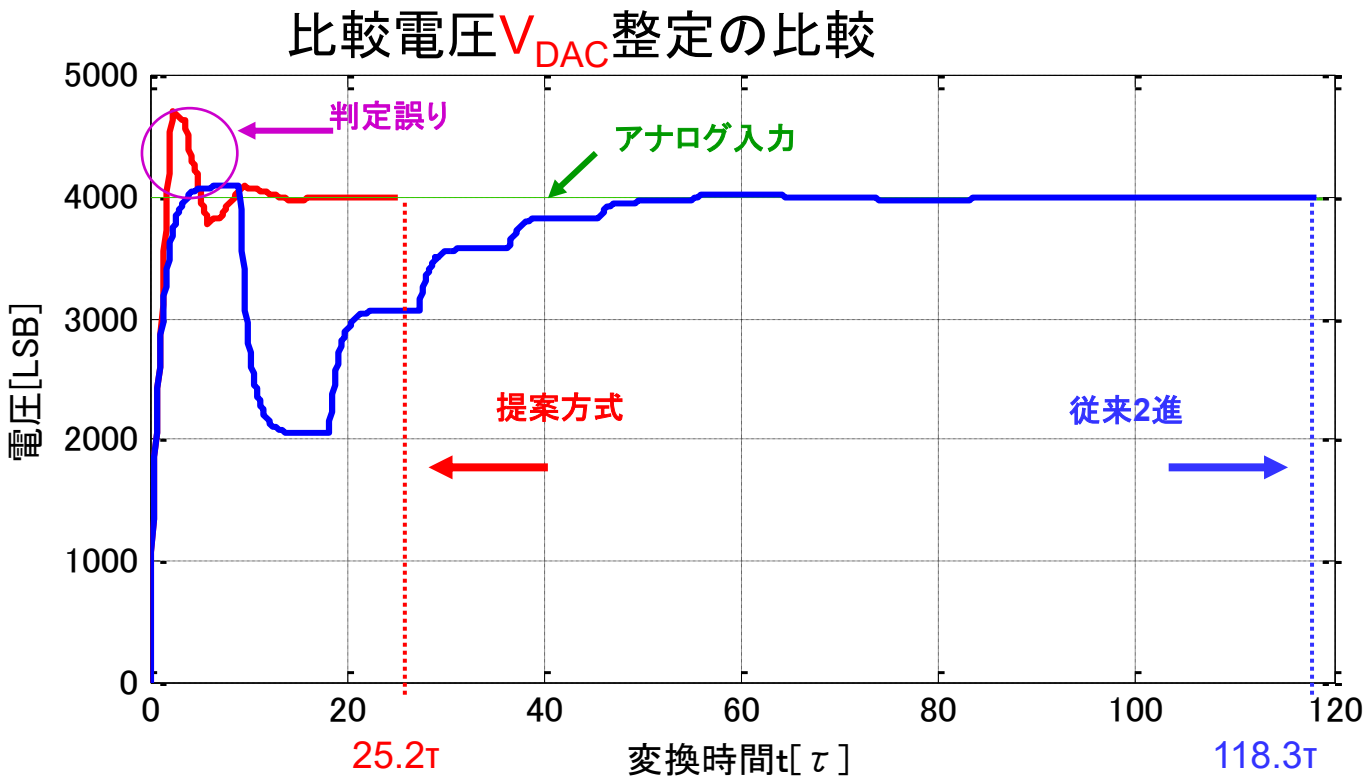


非2進探索アルゴリズムによるAD変換 高速化

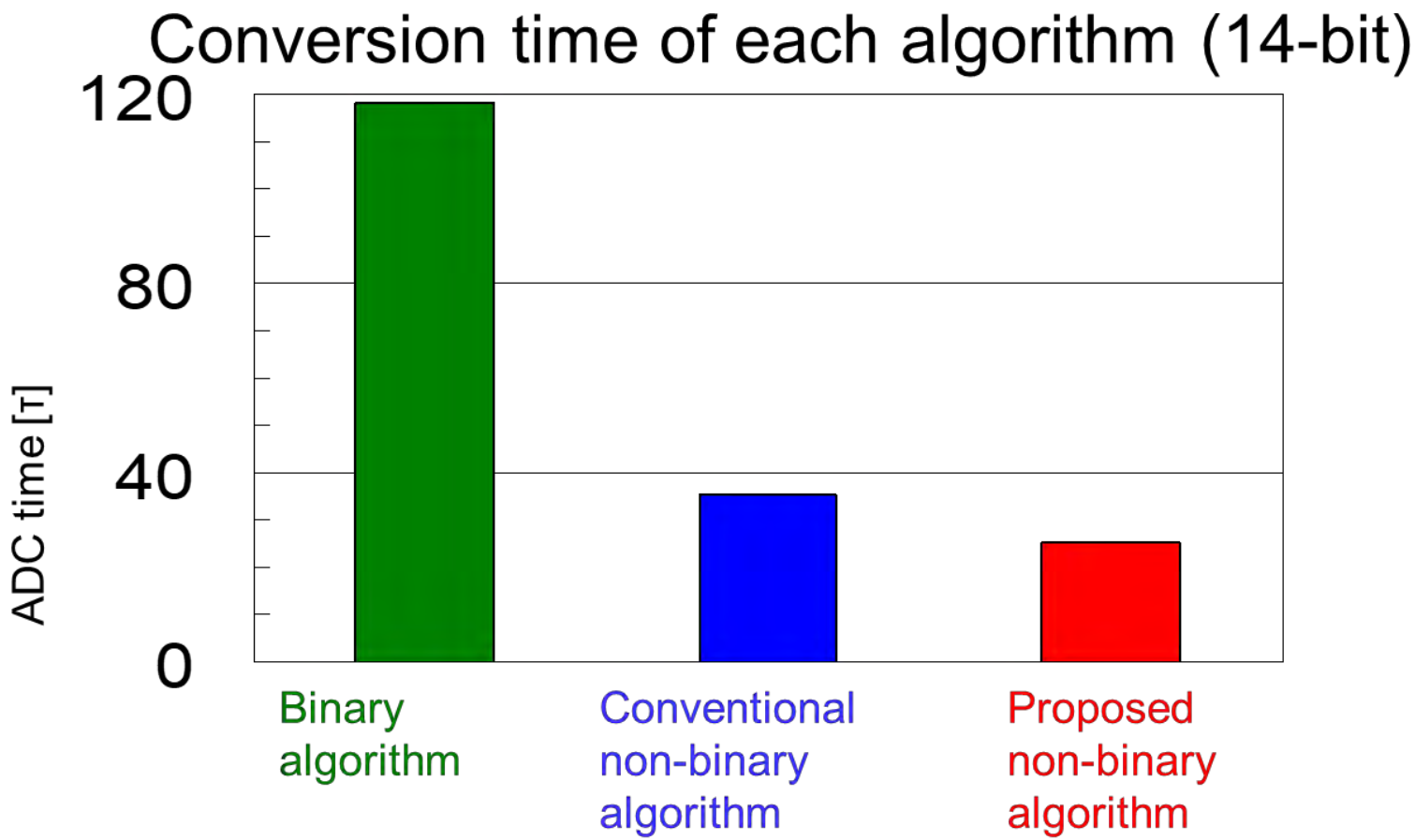
従来2進：　14ビット14ステップ　1サイクル9.1τ

提案非2進：　14ビット22ステップ　1サイクル1.2τ

冗長による高速化
シミュレーション確認



AD変換スピードの比較



発表内容

- 問題提起
- ADCのデジタル自己校正技術
- ADCのデジタル誤差補正技術
- 研究提案
- まとめ

研究提案1: 自己校正ADCのテスト技術

- デジタル自己校正用メモリの
  値を観測してテストに利用
  値を書き換えてテストに利用　（例　Fault Injection)

:

テストピンを設ける等で
テストの際には積極的に内部状態を「観測」「制御」する。
➡ ADC内部の可観測性、可制御性の向上

- 自己校正用メモリデータは
  チップ使用時ユーザからは見えない。

研究提案2: 自己校正技術理論的基礎の確立

ADC内部回路の誤差

ADC内回路自体を用いて測定

→ 測定自体に誤差

→ 測定内容も制限

どの条件で、なぜ自己校正で精度がでるのか？

結果としてADC精度確保。

個別技術では解決。

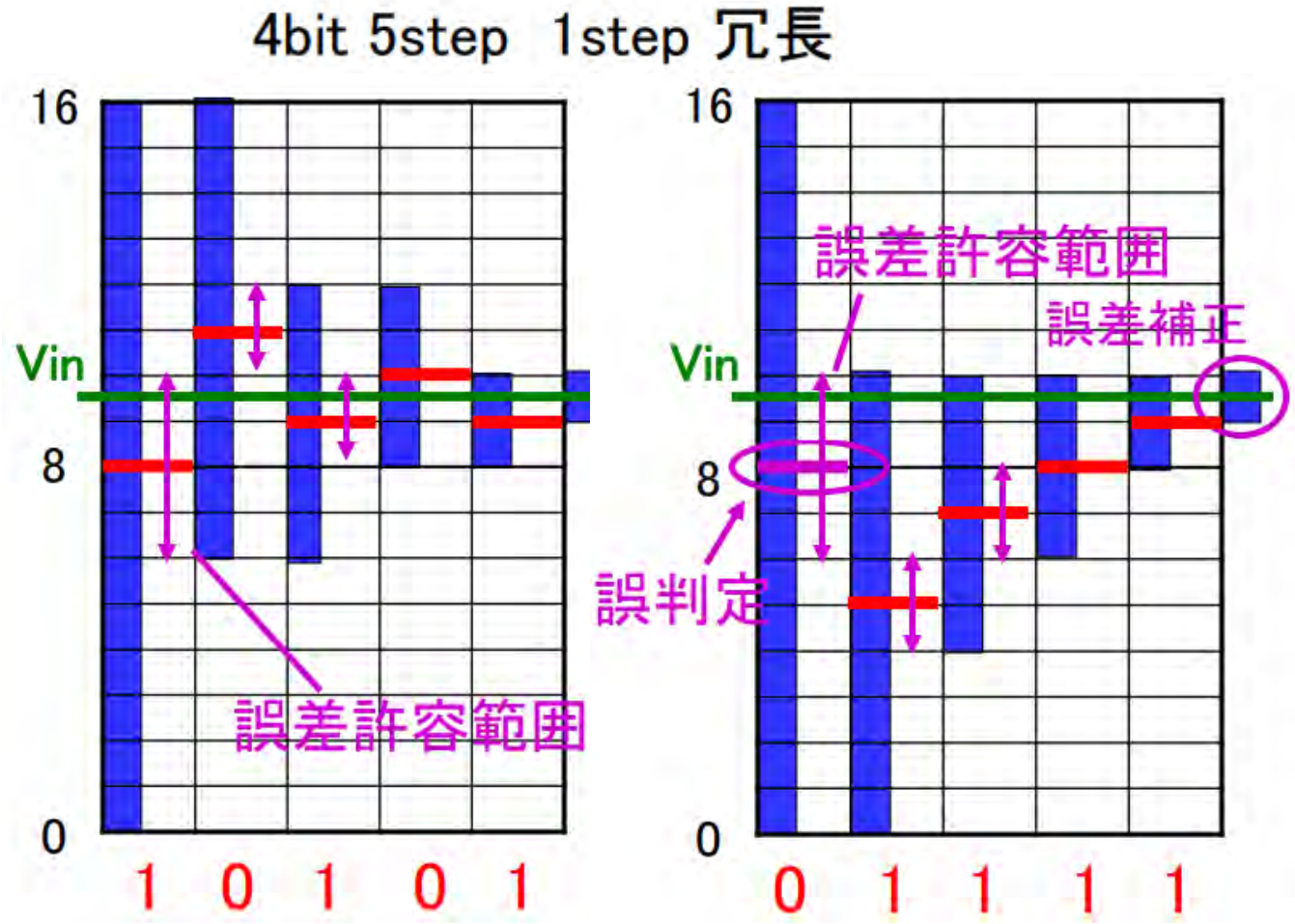
一般論では未解決。

限界も明らかにする

研究提案3: デジタル誤差補正SAR ADC テスト技術

- 補正後の出力データだけでなく
  コンパレータ出力系列値も観測
- 途中でFault Injection

ADC信頼性評価に利用できないか



8+3-2+1-1+0.5-0.5 =9

8-3+2+1+1+0.5-0.5=9

両方とも正解出力9

発表内容

- 問題提起
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- ADCのデジタル誤差補正技術
- 研究提案
- まとめ

まとめ

- デジタル自己校正・誤差補正ADC
  - ⇒ Fault Tolerant なアナログ・デジタル混載回路
  - ⇒ 内部の性能不良を隠す
  - ⇒ テストが難しくなる

- 3つの研究提案
  - ① 自己校正ADC内のテーブルの観測・制御
  - ② 自己校正ADCの基礎理論
  - ③ 冗長構成の誤差補正ADCの内部状態遷移の観測・制御

さらなる展開

量子コンピュータ

　誤差補正技術が重要

　冗長構成になっている

この観点から　量子コンピュータの試験技術　を調べていく

関連発表 (1)

[1] 小林春夫
「デジタルアシスト・アナログ技術 – 微細CMOSの強みを生かす回路設計」
大阪大学 高度人材育成センター 先端アナログ技術セミナー
(2012年1月23日)

[2] 高橋洋介、趙楠、傘昊、三田大介、八木拓哉、小林春夫
「パイプラインADCデジタル自己校正アルゴリズム」
FTC研究会、長崎(2008年1月).

[3] 早川晃, 趙楠, 堀田正生, 小林春夫
「高性能逐次比較AD変換器アーキテクチャ」
スライド 電気学会、電子回路研究会、桐生(2006年3月).

関連発表 (2)

[4] 小林春夫
「計測技術者が知っておくべきアナログ回路の基礎（チュートリアル）
- 電子計測技術者のためのアナログ技術再入門 -
AD変換器のデジタル誤差補正・自己校正技術」
計測展 東京, 日本電気計測器工業会主催, 日経BP社共催（2009年11月）

[5] Y. Kobayashi, T. Arafune, S. Shibuya, H. Kobayashi, H. Arai,
"Redundant SAR ADC Algorithms for Reliability Based on Number Theory",
First IEEE International Workshop on Automotive Reliability &
Test- ART Workshop, Fort Worth, TX (Nov. 17-18, 2016)

関連発表 (3)

[6] T. Ogawa, H. Kobayashi, Y. Tan, S. Ito, S. U. Takai, K. Niitsu,
T. Yamaguchi, T. Matsuura, N. Ishikawa
“SAR ADC That is Configurable to Optimize Yield,”
IEEE Asia Pacific Conference on Circuits and Systems,
Kuala Lumpur, Malaysia (Dec. 2010).

APCCAS 2010 Session :Hang Jebat 1 & 2 ADC / DAC II

Paper ID : 1569334445

SAR ADC That is Configurable to Optimize Yield

T. Ogawa, H. Kobayashi, Y. Tan, S. Ito, S. Uemori, N. Takai, K. Niitsu, T. J. Yamaguchi, T. Matsuura, N. Ishikawa

Gunma University

Supported by STARC

Outline

- Research purpose
- Background
- Configurable non-binary algorithm SAR ADC
- Production-time configuration SAR ADC
- Test chip design & measurement Results
- Conclusion

Research purpose

- **Non-binary SAR ADC can achieve …**
  - **High-speed operation** ☺
  - **Power consumption increased** ☹
- **This work introduces the solution for the speed-power trade-off for yield improvement.** ☺
  - **Propose the method of estimating the "DAC output settling time and speed margin" at production test.**
  - **Test chip fabrication & its measurements demonstrate the effectiveness of our approach.** ☺

Outline

- Research purpose
- **Background**
  - **Successive approximation algorithm**
  - DAC incomplete settling
  - SA algorithm selection
- Configurable non-binary algorithm SAR ADC
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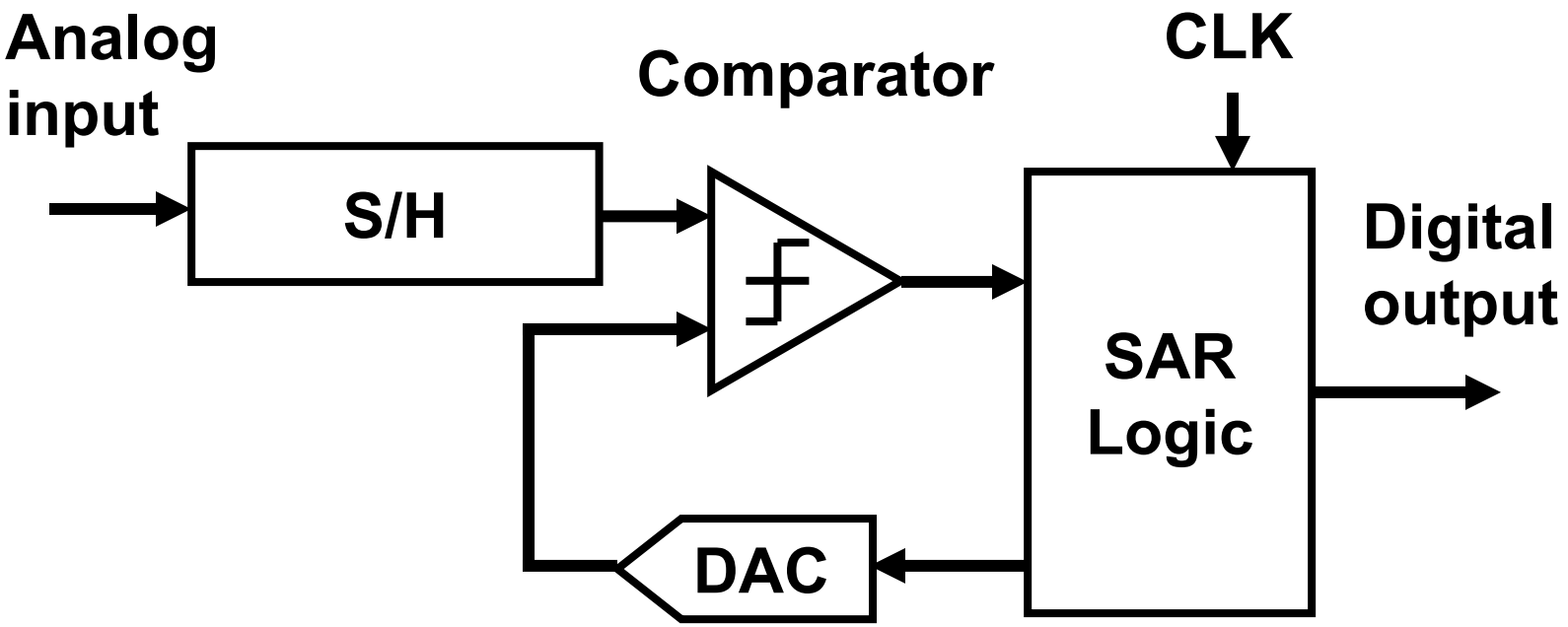
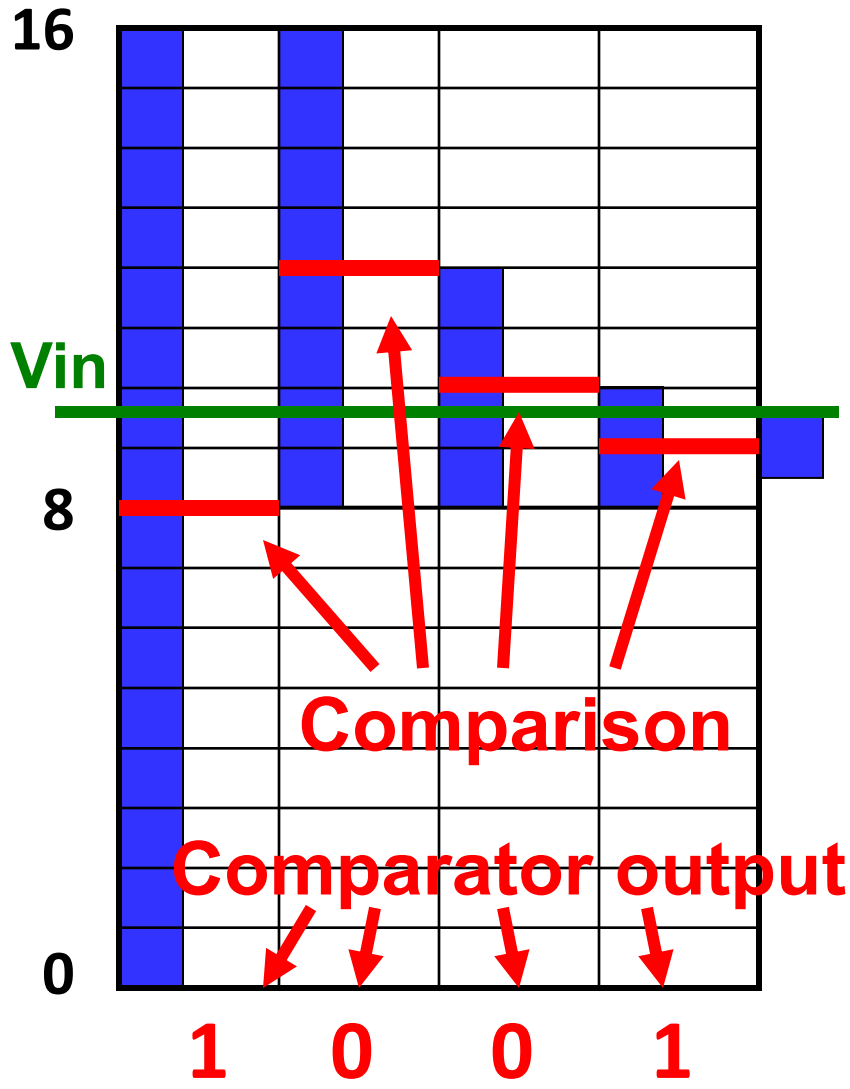
SAR ADC Block



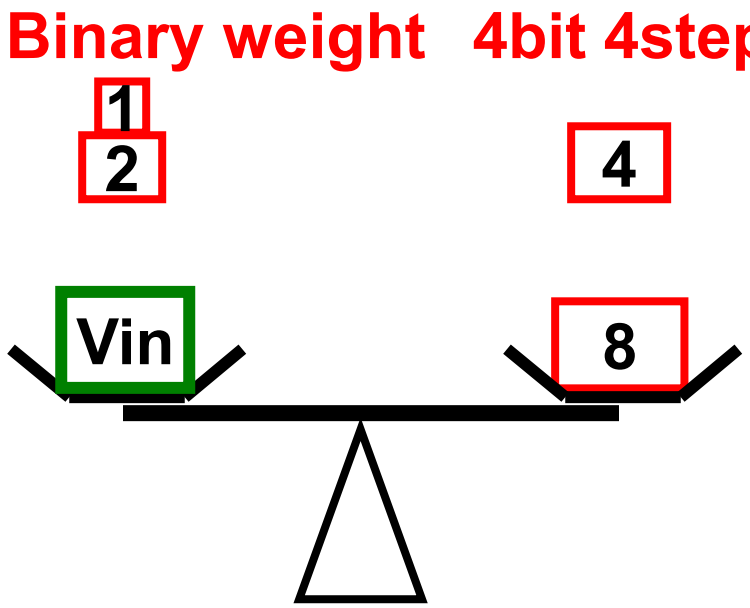
SAR ADC is “digital rich” approach.

→ Suitable for fine CMOS implementation.

Binary search algorithm

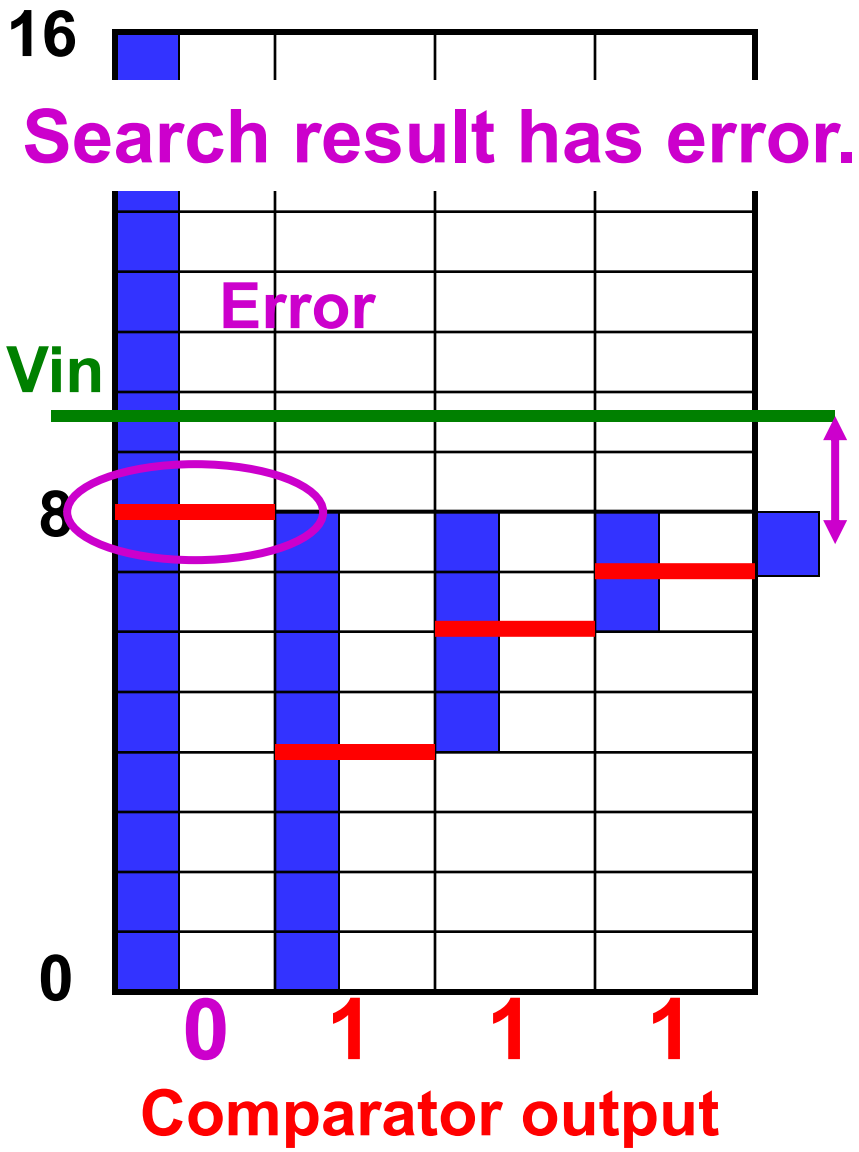


“Principle of a balance”



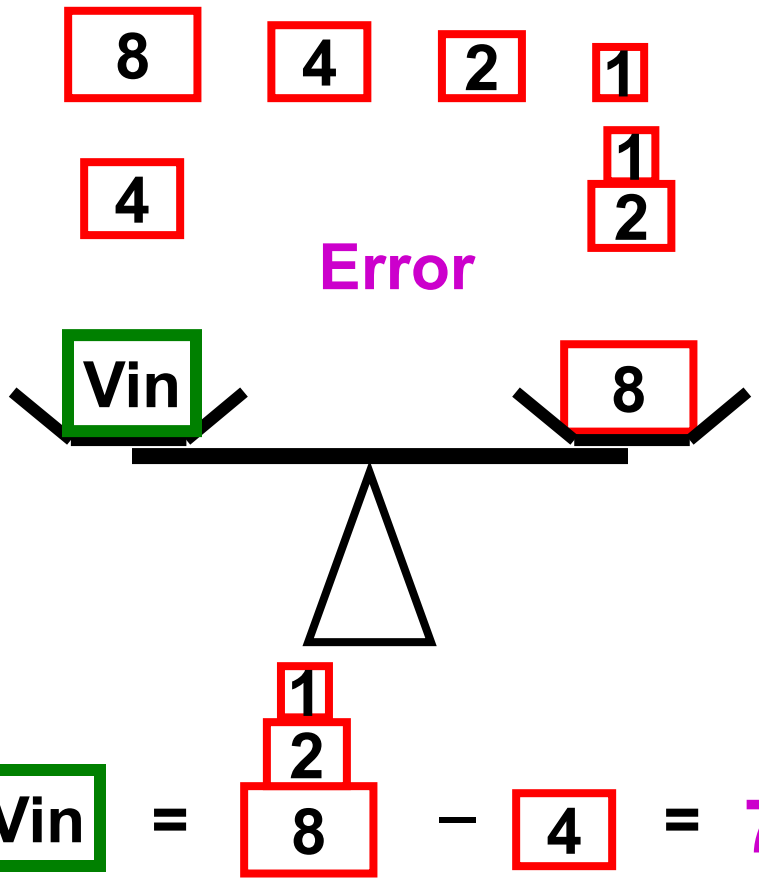
Vin = 4 8 − 1 2 = 9

Problem of binary search algorithm



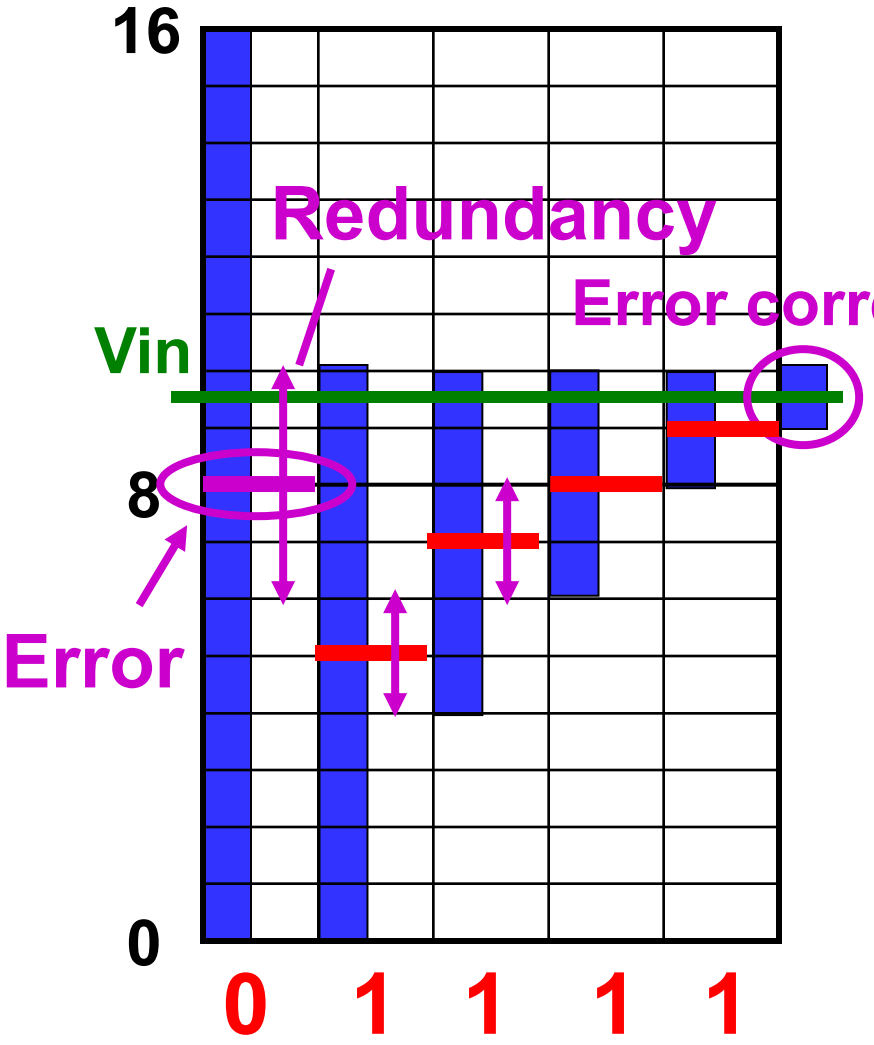
“Principle of a balance”

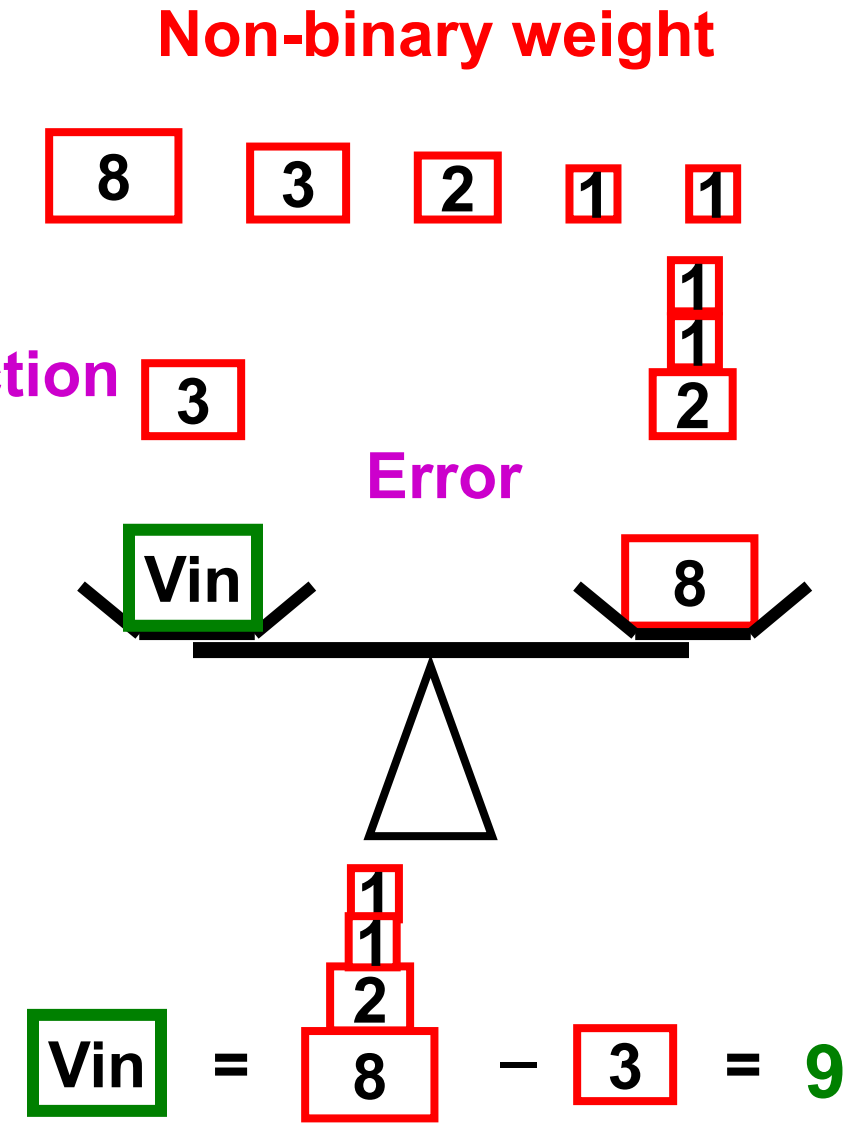
Binary weight 4bit 4step



Digital output has error.

Error correction with non-binary





4bit 5step Redundancy:1step

Digital error correction principle of non-binary algorithm

Digital output "9" case

Binary search algorithm

Error Correction : Not Available

Comparator output: 1 0 0 1

Dout = 8 + 4 – 2 – 1 + 0.5 – 0.5 = 9 ← Only one

Non-binary search algorithm

Error Correction : Available

Comparator output: 1 0 1 0 1

Dout = 8 + 3 – 2 + 1 – 1 + 0.5 – 0.5 = 9 ← Multiple

Comparator output: 0 1 1 1 1

Dout = 8 – 3 + 2 + 1 + 1 + 0.5 – 0.5 = 9

Outline

- Research purpose
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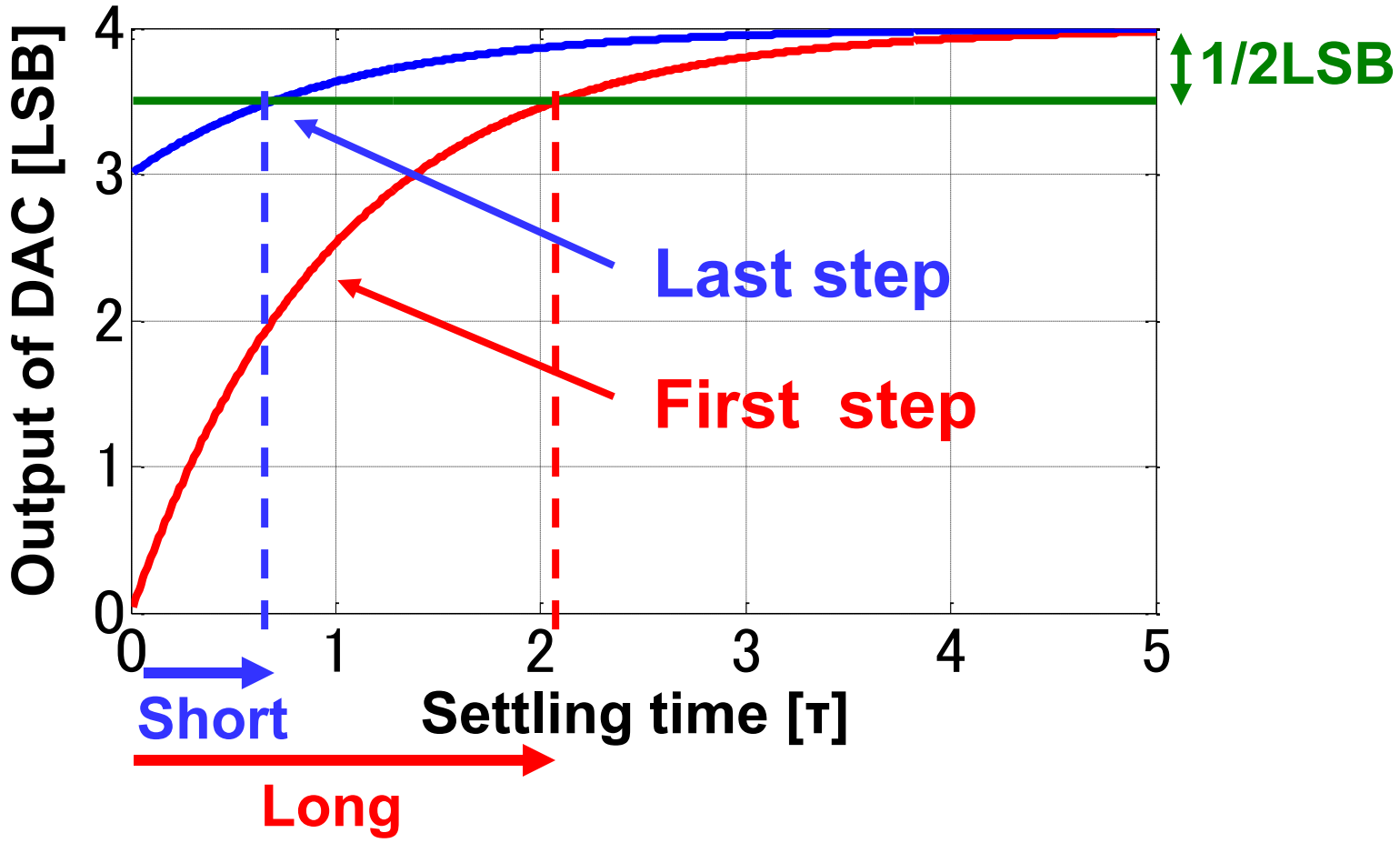
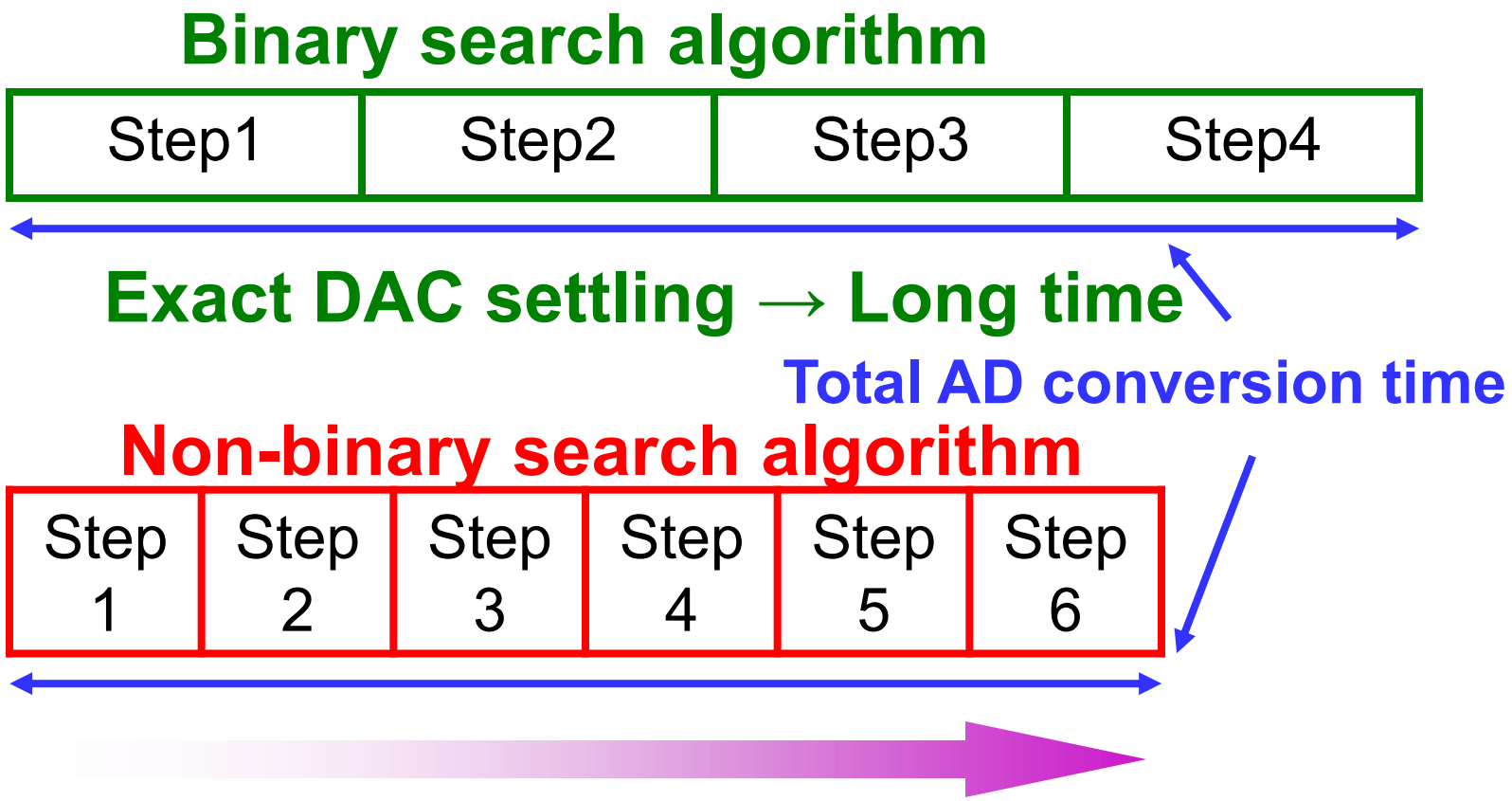
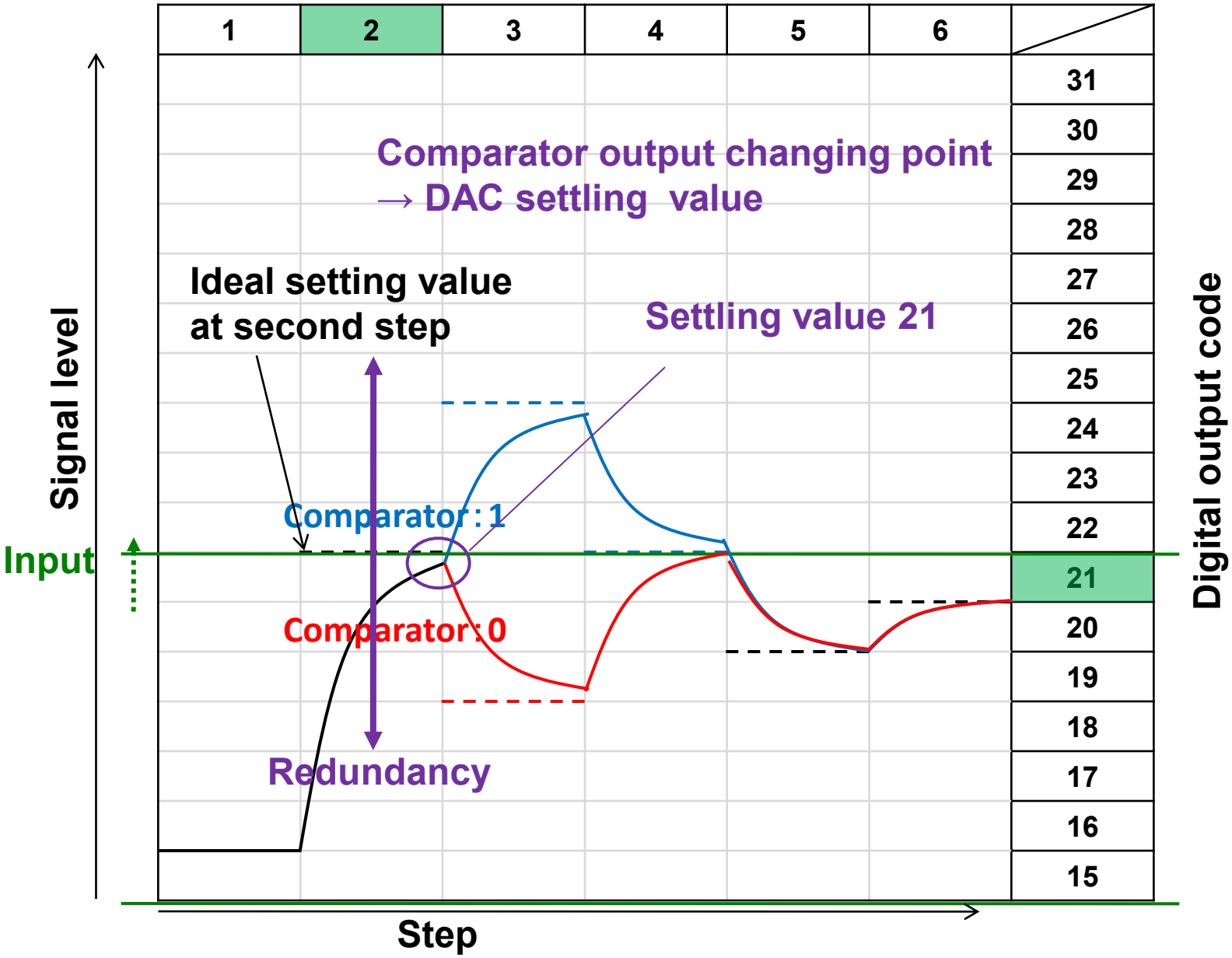
Settling of DAC output



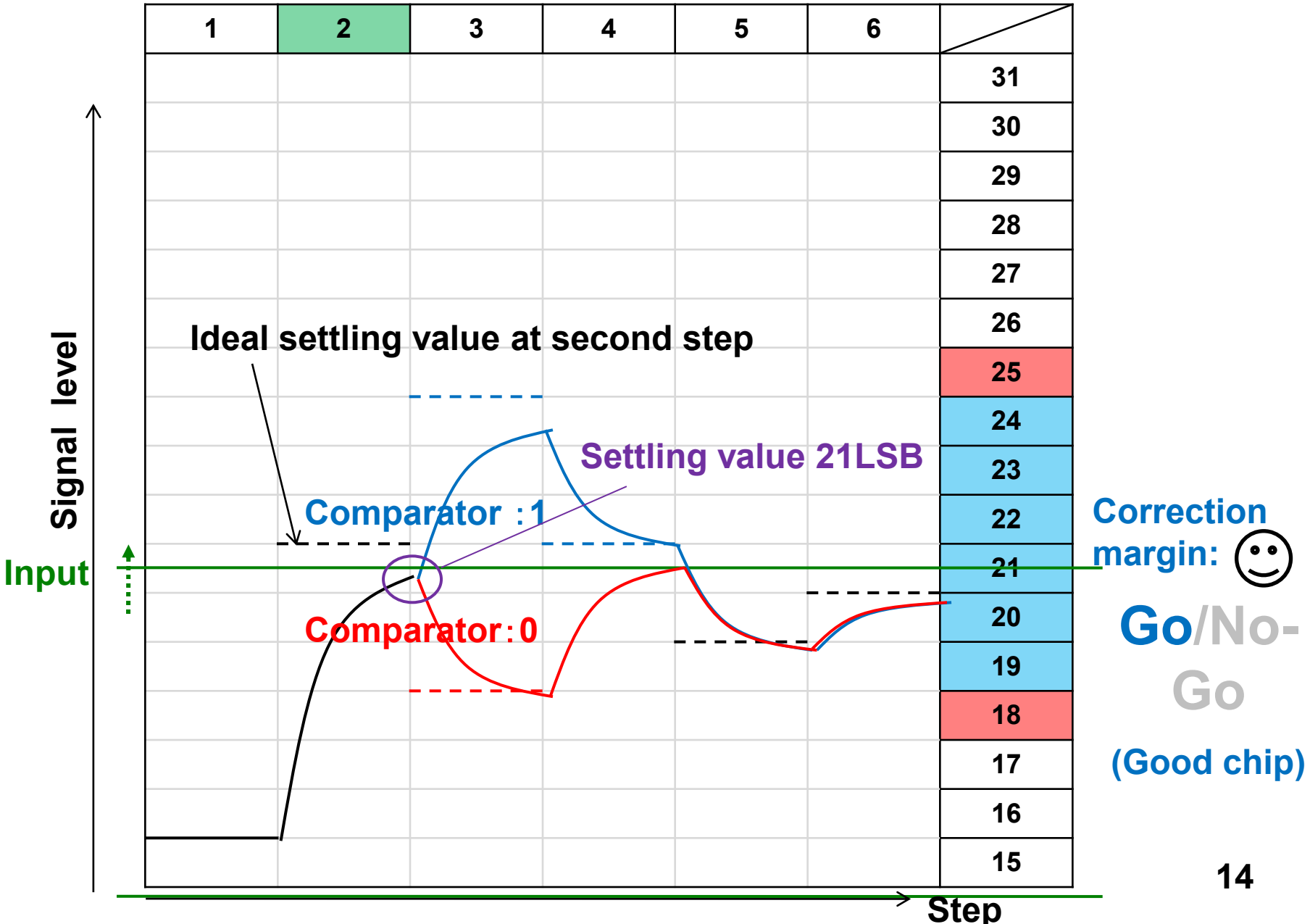
AD conversion time for both algorithms



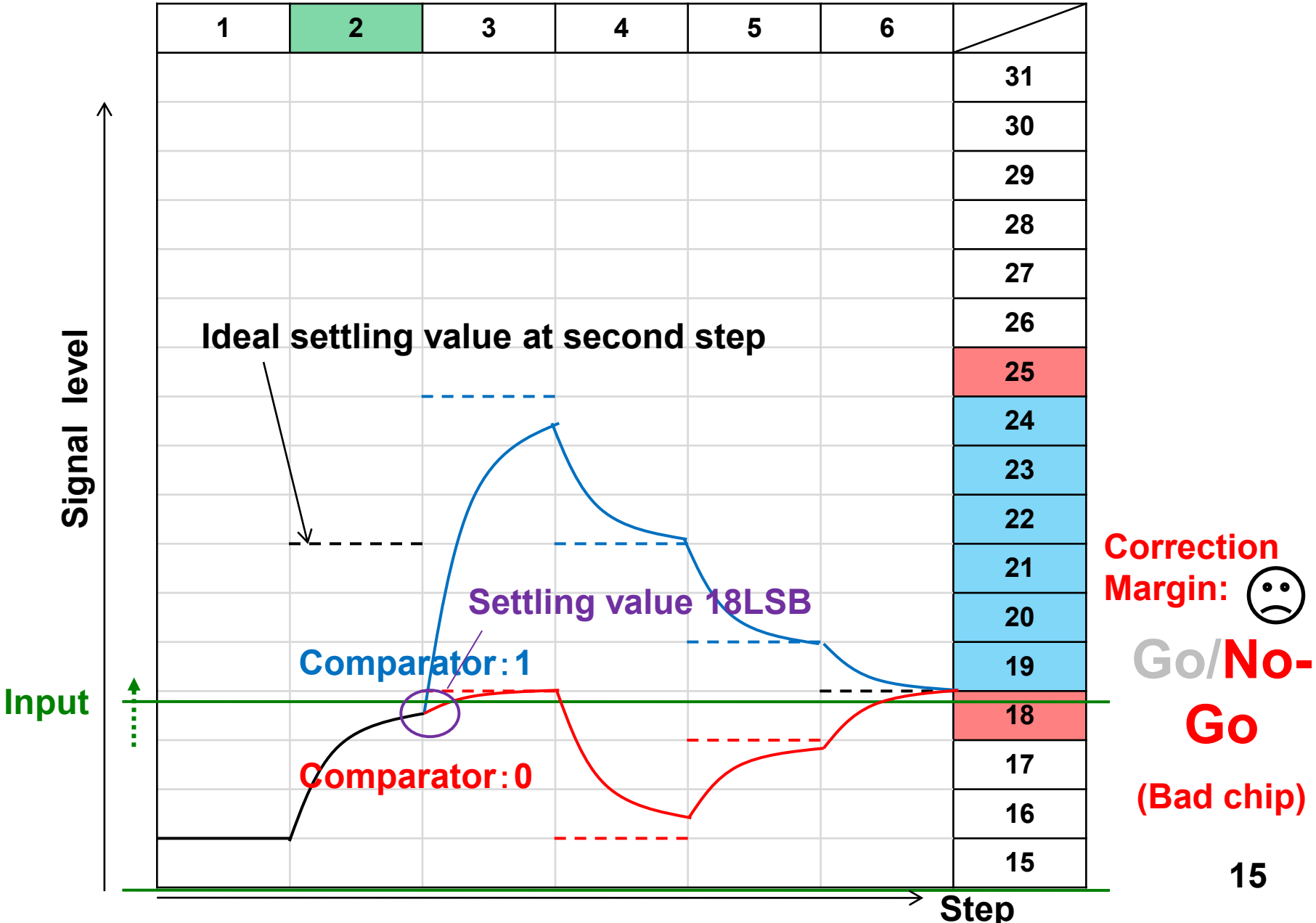
DAC settling estimation algorithm



Setting test at second step (5bit 6step)



Setting test at second step (5bit 6step)



Settling value at second step

$$V_{DAC}(k+1) = V_{DAC}(k) + DAC(k+1) * (1 - e^{-\frac{t}{\tau_{TP}}})$$

$$512 + 246(1 - e^{-\frac{2.3\tau_{TP}}{\tau_{TP}}}) = 733.3LSB$$

DAC Settling estimation

Step →

Comparator output

1	2	3	4	5	6	7	8	9	10	11	12	ADC output
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	0	1	1	733
1	1	0	0	0	0	0	1	1	0	1	1	**733**
1	0	1	1	0	1	0	1	0	0	1	1	**733**
1	0	1	1	0	1	0	1	0	0	1	1	733
1	0	1	1	0	1	0	1	0	0	1	0	732
1	0	1	1	0	1	0	0	1	1	1	0	732
1	0	1	1	0	1	0	0	1	1	1	0	732
1	0	1	1	0	1	0	0	1	1	1	0	732
1	0	1	1	0	1	0	0	1	1	0	1	731
1	0	1	1	0	1	0	0	1	1	0	1	731

Outline

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SA algorithm selection for 10bit non-binary SAR ADC

Fast chip (τ=3.5 ns)
10bit 11step
Low-power

Step	P(k)
1	512
2	256
3	115
4	63
5	35
6	19
7	11
8	6
9	3
10	2
11	1

Middle chip (τ=4.0 ns)
10bit 12step
Middle-power

Step	P(k)
1	512
2	256
3	109
4	62
5	36
6	21
7	12
8	7
9	4
10	2
11	1
12	1

Slow chip (τ=4.5 ns)
10bit 13step
High-power

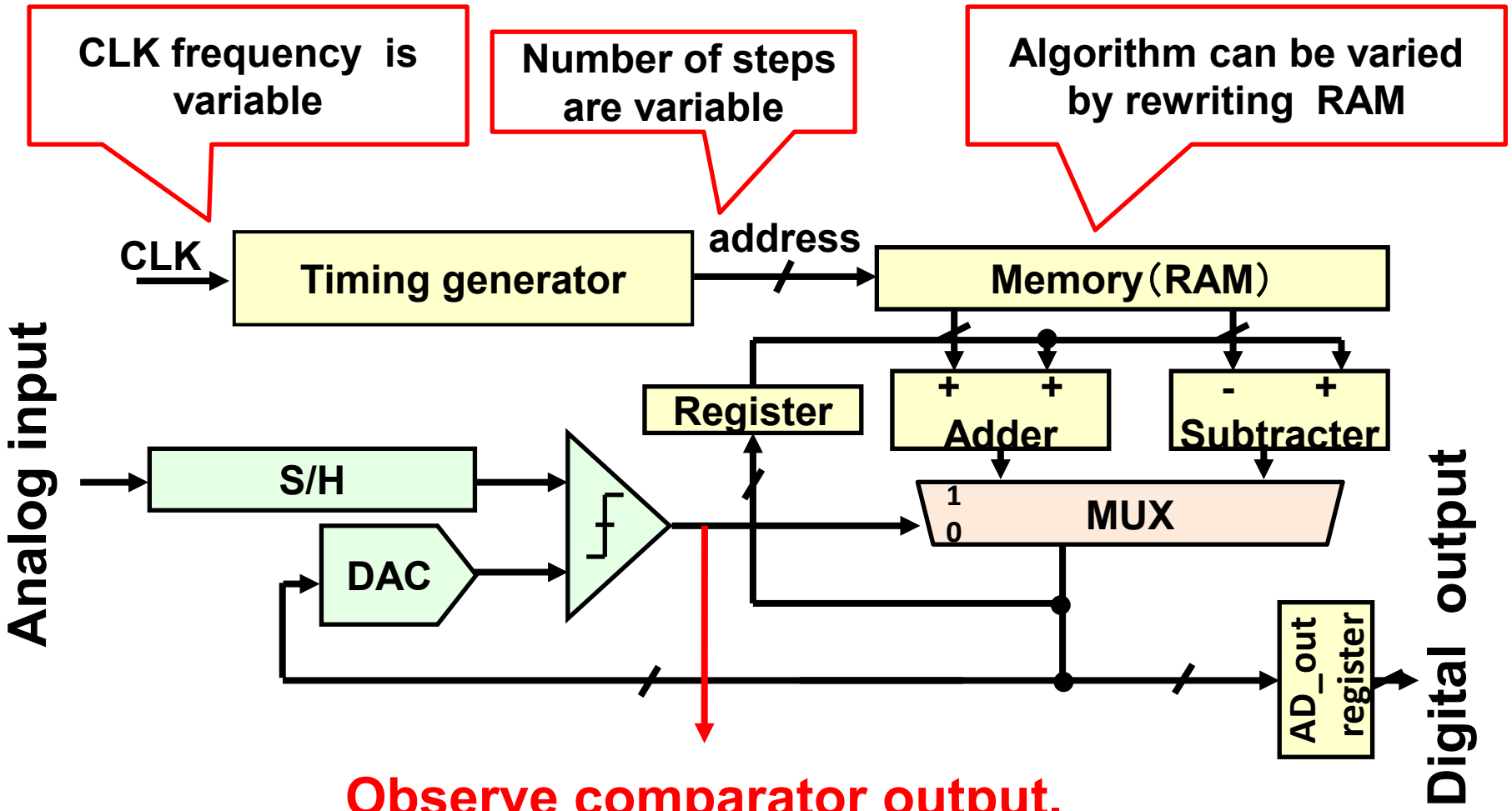
Step	P(k)
1	512
2	256
3	102
4	61
5	37
6	22
7	13
8	8
9	5
10	3
11	2
12	1
13	1

Even slow chips can meet the spec. (10MS/s) with additional power requirement.

Outline

- Research purpose
- Background
- **Configurable non-binary algorithm SAR ADC**
- Production-time configuration SAR ADC
- Test chip design & measurement Results
- Conclusion

Configurable non-binary SAR ADC diagram



Outline

- Research purpose
- Background
- Configurable non-binary algorithm SAR ADC
- **Production-time configuration SAR ADC**
- Test chip design & measurement Results
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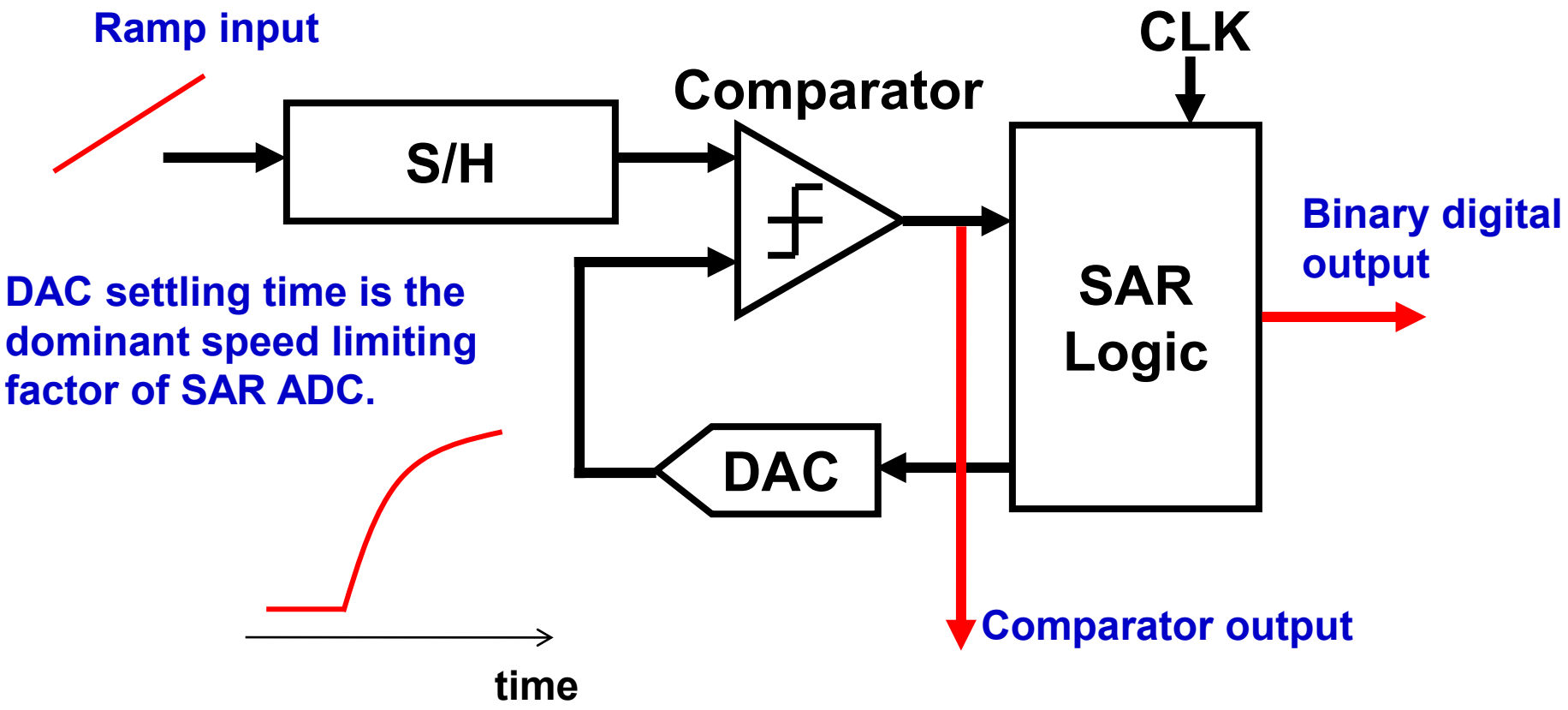
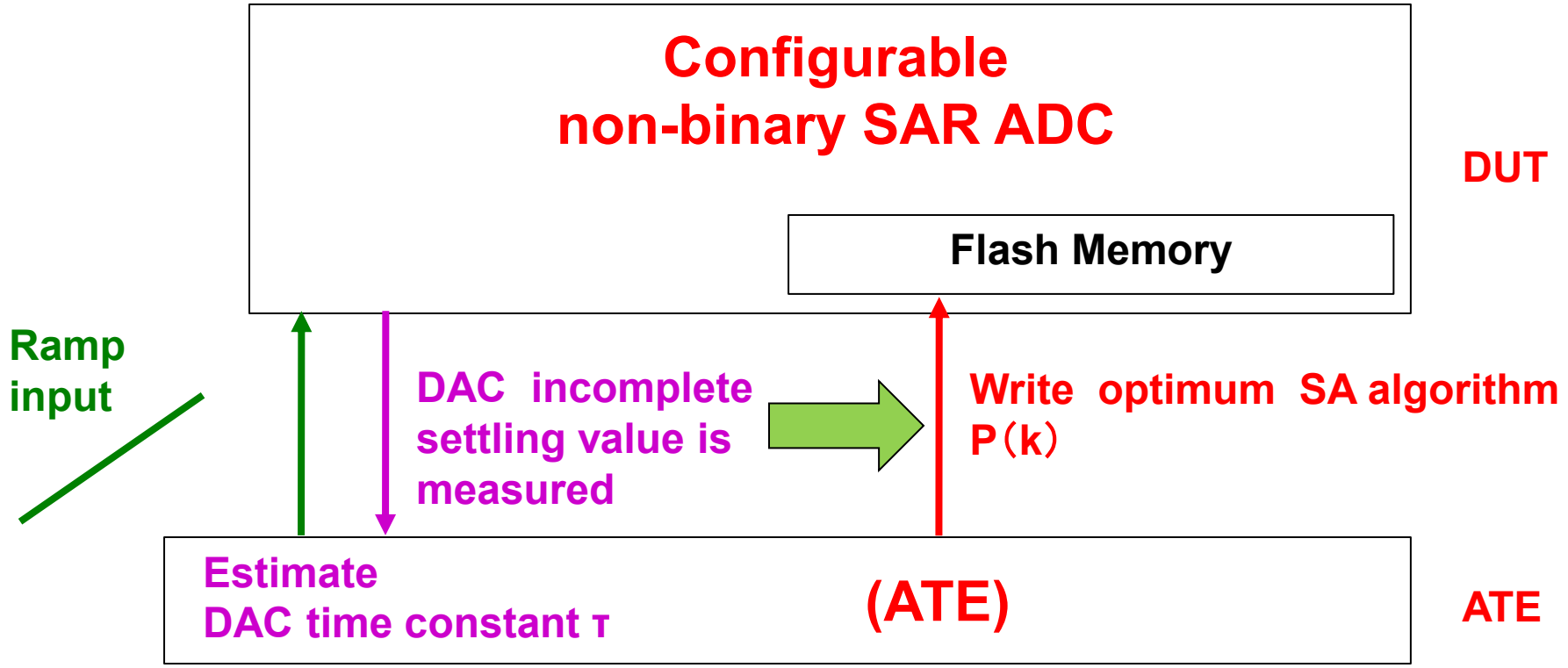
Test of the reconfigurable non-binary SAR ADC



Cooperation with ATE



τ is large ⇒ Satisfy speed spec. with large # of steps

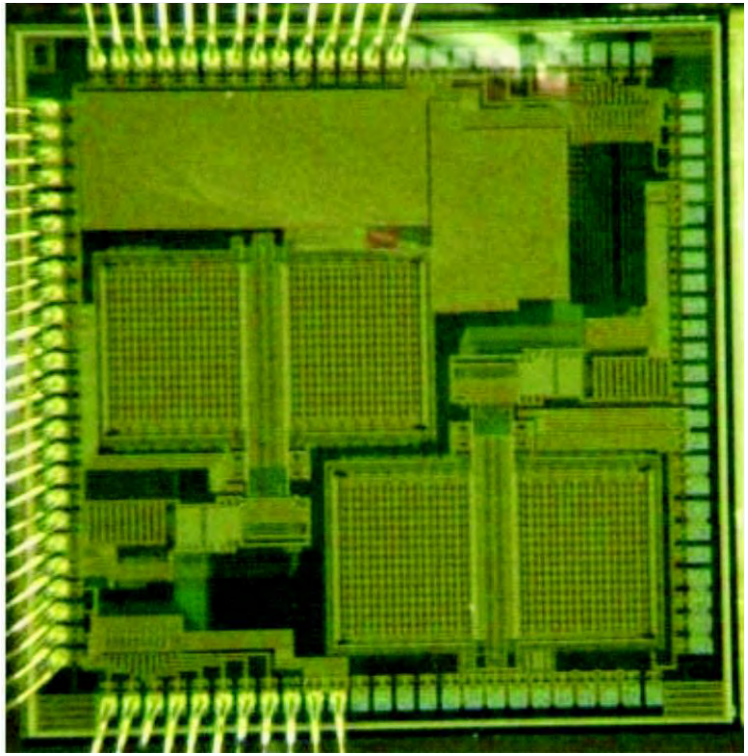
τ is small ⇒ Decrease power with small # of steps

※ATE: Automatic Test Equipment

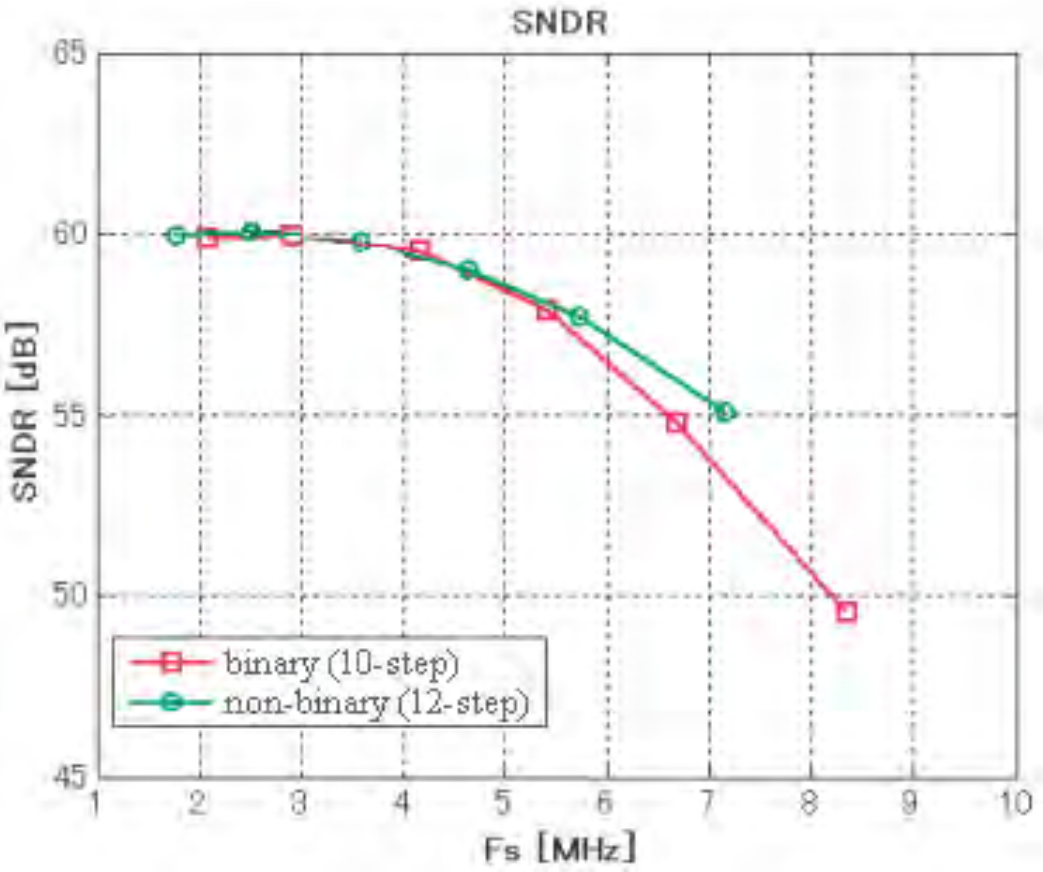
Outline

- Research purpose
- Background
- Configurable non-binary algorithm SAR ADC
- Production-time configuration SAR ADC
- **Test chip design & measurement Results**
- Conclusion

Reconfigurable Non-Binary SAR ADC Implementation and Measurement Results



0.18um CMOS
2.5mm x 2.5mm
with two SAR ADCs



SNDR comparison of
10step (binary) and 12step (non-binary)
F_{in}:100kHz

Verification with prototype chip

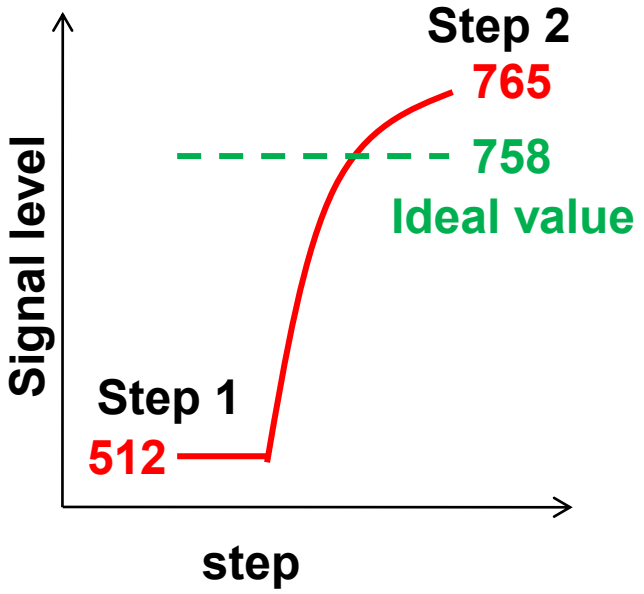
- **DAC settling value estimation by prototype**
  - **DAC output ringing case（ADC_A）**
  - **DAC output no-ringing case（ADC_B）**

→ Verify difference of settling values

※ADC_A：without bias capacitance

DAC settling estimation in ringing case

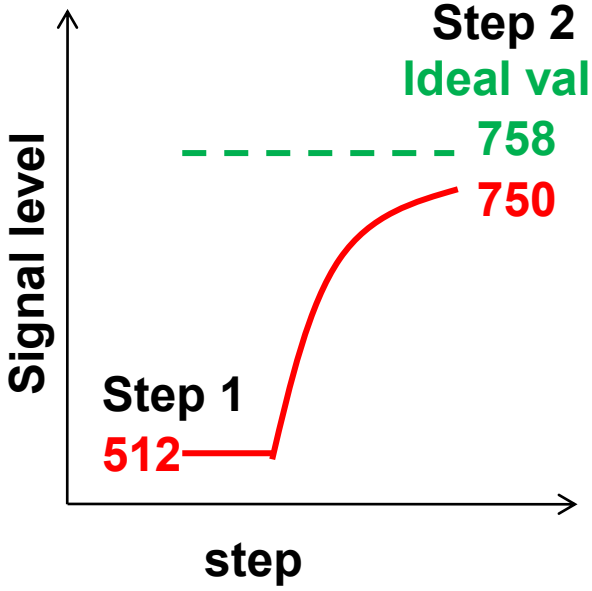
DAC settling value overshoots.



step1	step2	step3	step4	Comparator opinion
Ideal:512	Ideal:758 Estimate:765	Ideal:871 Estimate:876	Ideal:936 Estimate:939	1111
			Ideal:806 Estimate:809	1110
		Ideal:645 Estimate:647	Ideal:710 Estimate:712	1101
			Ideal:580 Estimate:580	1100
	Ideal:266 Estimate:258	Ideal:379 Estimate:377	Ideal:444 Estimate:443	1011
			Ideal:314 Estimate:311	1010
		Ideal:153 Estimate:146	Ideal:218 Estimate:214	1001
			Ideal:88 Estimate:84	1000

DAC settling estimation in no-ringing case

DAC settling is incomplete.



step1	step2	step3	step4	Comparator opinion
Ideal:512 Estimate:511	Ideal:758 Estimate:750	Ideal:871 Estimate:864	Ideal:936 Estimate:931	1111
			Ideal:806 Estimate:802	1110
		Ideal:645 Estimate:642	Ideal:710 Estimate:707	1101
			Ideal:580 Estimate:579	1100
	Ideal:266 Estimate:273	Ideal:379 Estimate:381	Ideal:444 Estimate:444	1011
			Ideal:314 Estimate:315	1010
		Ideal:153 Estimate:160	Ideal:218 Estimate:221	1001
			Ideal:88 Estimate:92	1000

Outline

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- **Conclusion**

Conclusion

- Propose a configurable non-binary SAR ADC.
  - Optimal yield

- DAC output settling margin is estimated by checking comparator output at each step and ADC output at final step.

- Measurement and simulation results validate the effectiveness of our proposed SAR ADC.

SAR ADC That is Configurable to Optimize Yield

Tomohiko Ogawa, Haruo Kobayashi, Yohei Tan, Satoshi Ito, Satoshi Uemori,
Nobukazu Takai, Kiichi Niitsu, Takahiro J. Yamaguchi, Tatsuji Matsuura, Nobuyoshi Ishikawa
Electronic Engineering Department, Gunma University, Japan email: k_haruo@el.gunma-u.ac.jp

***Abstract*— This paper describes a non-binary SAR ADC architecture that is reconfigurable at production testing time to increase the number of chips that meet a given sampling speed specification, i.e. to improve yield. A non-binary SAR ADC can realize higher sampling rates than a comparable conventional binary SAR ADC, by using overlapping SA ranges so that any errors due to incomplete settling of the internal DAC can be corrected in later steps of the successive approximation. In general, using more of the overlapping successive- approximation (SA) steps (and faster steps) permits faster SAR ADC sampling rates but increases power consumption. Thus this power-speed tradeoff can be utilized to compensate for CMOS process variations of each ADC chip; if the chip is slow, we can use more-rapid SA steps and more overlapping steps to satisfy the sampling speed specification (at the cost of increasing power consumption); if the chip is fast, we can use fewer (and slower) steps to satisfy the sampling speed specification and also achieve lower power consumption. We use automatic test equipment (ATE) for production testing and to store the appropriate algorithm data that enables the sampling rate specification to be met in flash memory on the chip. The DAC output settling margin is determined by checking comparator output at each step and confirming that ADC final output is correct. Our measurements demonstrate the effectiveness of this approach.**

Keywords: SAR ADC, Redundancy, Reconfigurable, Yield, Low Power, ADC Testing

I. Introduction

This paper describes a non-binary SAR ADC architecture whose successive-approximation algorithm can be configured at production testing time to optimize both yield and power consumption. The proposed architecture enables a too-slow SAR ADC chip to be reconfigured as a faster in-spec chip that uses relatively high power; a fast SAR ADC chip can be reconfigured to use lower power yet still meet the sampling rate specification [1], [2]. Our proposed architecture uses this trade-off between power and speed to choose the optimal algorithm that compensates for CMOS process variations between chips. An ATE is used to determine speed margin and set the optimal algorithm. DAC output settling margin is determined by checking comparator output at each step and confirming that ADC final output is correct.

We present these principles and algorithms in the following sections, and show measurement and simulation data that validates this approach.

II. Successive Approximation Algorithm

A. Binary search algorithm

We here describe the conventional binary search algorithm that realizes an N-bit resolution SAR ADC with N steps (Fig.1), and we assume that the analog input range is normalized from 0 to $2^N - 1$. The comparator compares the analog input (V_{in}) and the reference voltage (DAC output), and its output $s(k)$ at k-th step is defined by

$$s(k) = \begin{cases} 1 & \text{(when } V_{in} > V_{ref}(k)\text{)} \\ -1 & \text{(otherwise).} \end{cases}$$

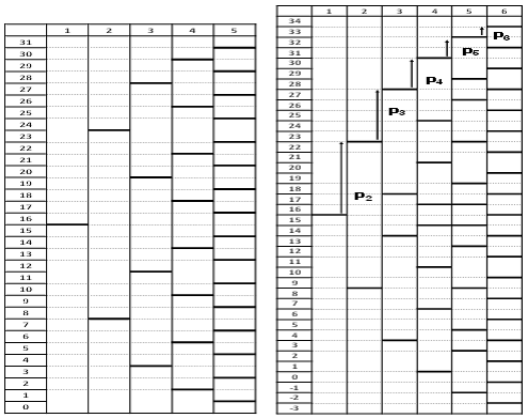

Fig. 1. Binary search algorithm of a 5-bit SAR ADC with 5 steps (Left). Non-binary search algorithm of a 5-bit SAR ADC with 6 steps (Right).

The reference voltage in the k-th step ($V_{ref}(k)$) is given by

$$V_{ref}(k) \quad = \quad 2^N \cdot \big(2^{-1} + \sum_{i=2}^{k} s(i-1)2^{-i}\big).$$

Also the ADC output D_{out} is given by

$$D_{out} \quad = \quad 2^{N-1} + \big(\sum_{i=2}^{N} s(i-1)2^{N-i}\big) + \frac{1}{2}(s(N)-1).$$

B. Non-binary Algorithm

We here describe our generalized non-binary algorithm that realizes N-bit resolution SAR ADC in M steps (N $\leq$ M) (Fig.1) [1], [2]. We give the reference voltage in k-th step($V_{ref}(k)$) as follows:

$$V_{ref}(k) \quad = \quad 2^{N-1} + \sum_{i=2}^{k} s(i-1)p(i). \qquad (1)$$

Here $k = 1, 2, .., M$, and $p(k)$ is the value for addition to (or subtraction from) the reference voltage in the previous step. Then we have the following ADC digital output :

$$D_{out} \quad = \quad 2^{N-1} + \sum_{i=2}^{M} s(i-1)p(i) + \frac{1}{2}(s(M)-1). \quad (2)$$

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We have derived that $p(i)$ must satisfy the following:

$$p(1) \quad = \quad 2^{N-1}, \quad \sum_{i=1}^{M} p(i) = 2^N - 1 + 2 \cdot (\text{over-range}).$$

For the non-binary search algorithm using eq.(2), we see that there are 2^M comparison patterns (possible comparator output combinations for all M steps) and 2^N output patterns (output codes in binary format), and since M is bigger than N, 2^M is bigger than 2^N. In other words, for a given output level D_{out}, there can be multiple comparison patterns, which means that there is some redundancy. Thus even if the comparator decision in a given step is wrong, correct ADC output may be obtained in the following step.

III. DAC Incomplete Settling

A. SAR ADC Sampling Speed & DAC Incomplete Settling

We consider the incomplete settling effects of the DAC for generating the reference voltage inside the SAR ADC. We assume that the DAC is a first-order system with a time constant of τ, and the actual reference voltage (DAC output) $V_{ref}^{act}(k)$ at k-th step is given by

$$V_{ref}^{act}(k) = \\ V_{ref}^{act}(k-1) \quad + \quad [V_{ref}(k) - V_{ref}^{act}(k)][1 - e^{-\frac{T_{step}}{\tau}}]. \quad (3)$$

Here T_{step} is the time slot for each step, The reference voltage error at k-th step due to the DAC output incomplete settling is given by

$$V_{ref,er}(k) = V_{ref}^{act}(k) - V_{ref}(k).$$

If time slot "T_{step}" is long enough, the error becomes small. Note also that the error is smaller in later steps because the change in the reference voltage between steps is smaller, and that the SAR ADC with the binary algorithm has to wait for the DAC to settle within 1/2 LSB in each step (Fig.2 (a)). The non-binary search algorithm can correct for error due to incomplete DAC settling in the previous step, and we do not have to wait for the DAC to settle within 1/2 LSB (Fig.2 (b)).

B. Estimating DAC output settling value

Now we discuss the algorithm for estimating the DAC output settling value at each SA conversion step. Let us consider two values of the ADC input V_{in1}, V_{in2}. The DAC output settling value $V_{DAC}(k)$ at the k-th step is between V_{in1} and V_{in2} when, for the inputs V_{in1} and V_{in2}, the comparator decision results are the same from the first to the k-th steps but they are different at the (k+1)-th step.

In other words, we can determine the DAC output settling value $V_{DAC}(k)$ at the k-th step from the measured values V_{in1} and V_{in2} in this case (Fig.3 (a)) .

$$V_{in1} \leq V_{DAC}(k) \leq V_{in2}.$$

Now we have the following algorithm for estimating DAC output settling value from the above observation:

1) We apply a ramp input signal to the SAR ADC during its test and obtain the comparator decision results for all steps, as well as the final ADC output.

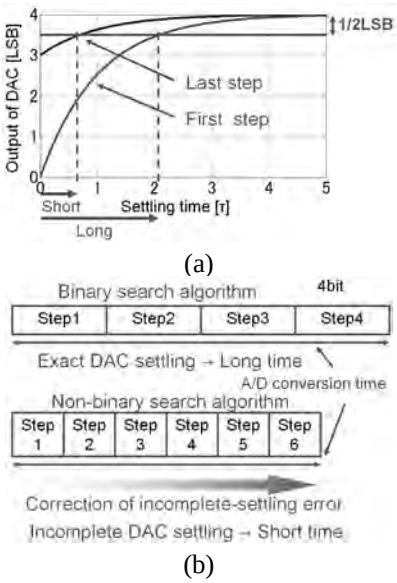


Fig. 2. (a) Settling of the DAC output to generate a reference voltage at each stage. (b) AD conversion-time explanation for the binary and non-binary algorithms.

2) At the early steps (where comparator decision errors are allowable to some extent, due to overlapping steps), we find the values of V_{in1} and V_{in2} for which comparator decisions are different.
3) Let the ADC output for V_{in1} be ADC_{out1} and that for V_{in2} be ADC_{out2}. If ADC_{out1} and ADC_{out2} are equal, then the DAC output settling value is the reference voltage multiplied by ADC_{out1} (= ADC_{out2}). Else if they are different, the DAC output settling value is between the reference voltage multiplied by ADC_{out1} and that multiplied by ADC_{out2} (Fig.3 (b)).

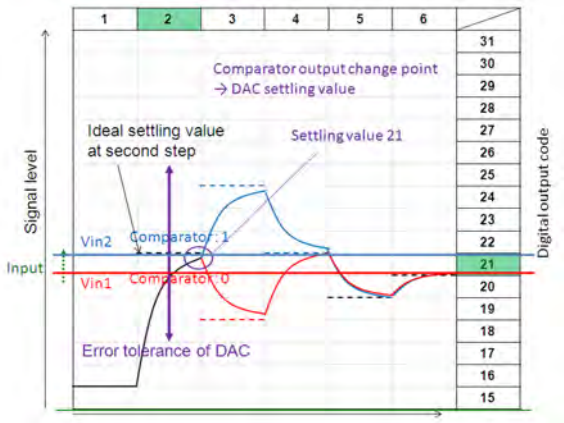
IV. SA Algorithm Selection

After estimating the DAC settling value, we can estimate the DAC time constant τ using eq.(3). As an example, we have derived the SA algorithms using simulation to meet 10b 10MS/s specification in cases of DAC time constant $\tau = 3.5ns, 4.0ns, 4.5ns$, as shown in Tables I, II, III. The number of SA steps is minimized for low power. We see that even the slow chip ($\tau = 4.5ns$) can operate at 10MS/s with appropriate choice of non-binary algorithm; if a binary algorithm is used, a slow chip cannot operate at 10MS/s and is rejected at production testing time.

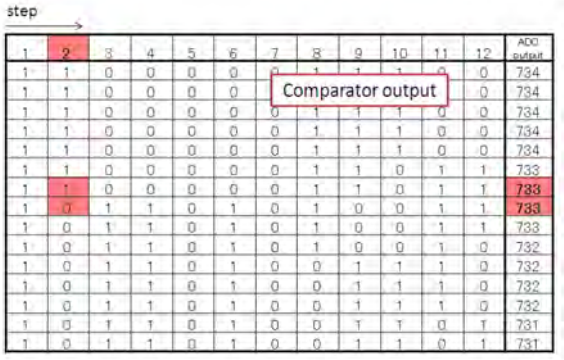
In general, using more of the overlapping SA steps (and faster steps) permits faster SAR ADC sampling rates but increases power consumption.

V. Configurable Non-binary Algorithm SAR ADC

Fig.4 shows a block diagram of our proposed configurable SAR ADC; it consists of a clock generator, a timing generator (a ring counter and associated logic circuits), a comparator, a DAC for the reference voltage generation and SAR logic with a coefficient RAM (an array of DFFs) and an adder/subtracter. The coefficient RAM stores the non-binary (or binary) steps to choose the next reference level. When the comparator output is



(a)



(b)

Fig. 3. DAC settling estimation algorithm. (a) DAC output waveform. (b) Comparator output pattern.

TABLE I
FAST CHIP (ESTIMATED DAC TIME CONSTANT τ = 3.5NS), 10-BIT 11-STEP (LOW POWER)

step	p(k)
1	512
2	256
3	115
4	63
5	35
6	19
7	11
8	6
9	3
10	2
11	1

TABLE II
MIDDLE SPEED CHIP (τ=4.0NS), 10-BIT 12-STEP (MIDDLE POWER)

step	p(k)
1	512
2	256
3	109
4	62
5	36
6	21
7	12
8	7
9	4
10	2
11	1
12	1

TABLE III
SLOW CHIP (τ=4.5NS), 10-BIT 13-STEP (LARGE POWER)

step	p(k)
1	512
2	256
3	102
4	61
5	37
6	22
7	13
8	8
9	5
10	3
11	2
12	1
13	1

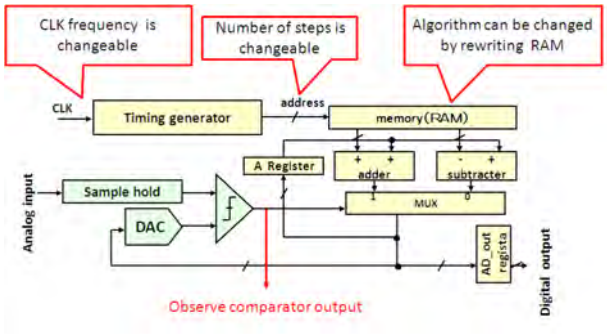


Fig. 4. Block diagram of the reconfigurable nonbinary SAR ADC.

"1", the RAM data is read and added to the current reference level with the adder; when it is "0", the data is subtracted with the subtracter. The result is applied to the DAC as its digital input.

The clock generator and timing generator are programmable so that we can select the number of steps. This configurable SAR ADC architecture allows us to set a binary or non-binary search algorithm by changing the algorithm in RAM and choosing the number of steps. .

VI. PRODUCTION-TIME CONFIGURATION OF SAR ADC

We here assume the following (Fig.5 (a)):

- The ADC output at the final step is observable from an ATE.
- The comparator output at each step is observable from an ATE.
- DAC settling time is the speed bottleneck of the SAR ADC.

During production testing (Fig.5 (b)):,

- the ATE applies a ramp input to the SAR ADC, and estimates the DAC settling time (time constant) by observing the comparator output at each step and the final ADC output.
- Based on the estimated DAC settling value, we use the ATE to calculate the optimal non-binary SA algorithm and store its parameters in flash memory. (Fig.5).

As described above, we estimate the DAC output settling value (and hence the DAC time constant) in the non-binary-algorithm SAR ADC. Settling values may vary among chips due to CMOS process variations, hence the optimal non-binary algorithm can differ from chip to chip; the algorithm is selected to correct for error due to incomplete settling of DAC output.

The choice of optimal non-binary SA algorithm is a trade-off between power and speed: if the chip is slow, we can use more-rapid SA steps and more overlapping steps to satisfy the sampling speed specification (at the cost of increasing power consumption); if the chip is fast, we can use fewer (and slower) steps to satisfy the sampling speed specification and also achieve lower power consumption.

VII. MEASUREMENT RESULTS

We have implemented our 10-bit reconfigurable SAR ADCs two times with a TSMC 0.18μm CMOS process to validate the effectiveness of our proposed architecture.

A. DAC Settling Estimation

Fig.6 shows ideal DAC output values (in the completely settled case) and the estimated values (in actual incomplete settled case) for the first, second, third and fourth SA conversion steps.

The first prototype SAR ADC did not have good SNDR, and we consider that this was due to DAC output ringing,

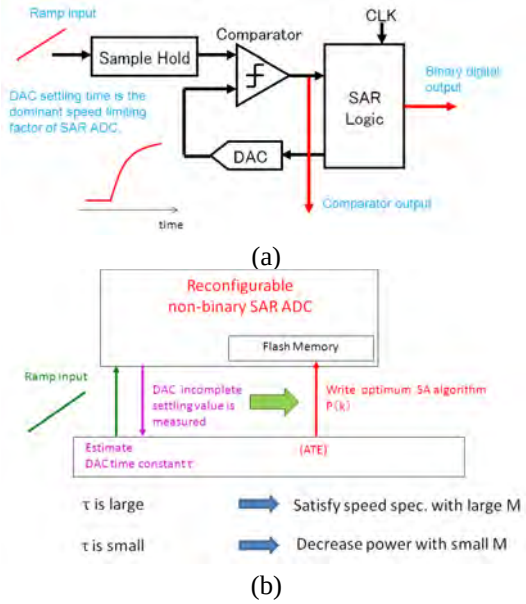


Fig. 5. Reconfiguration of the non-binary SAR ADC. (a) Test of the reconfigurable nonbinary SAR ADC. (b) Cooperation with ATE.

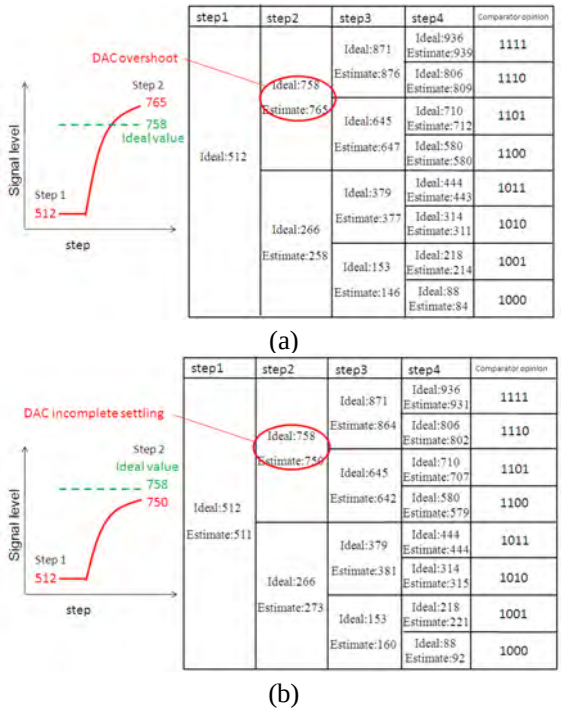


Fig. 6. Measurement result of 10bit 12step SAR ADC. (a) DAC output ringing case. (b) No ringing case.

with overshoot and undershoot. The problem was fixed in the second prototype SAR ADC.

Fig.6 (a) shows measurement results from the first prototype chip. We see that the estimated DAC output shows overshoot/undershoot, which is probably due to DAC output ringing.

Fig.6 (b) shows measurement results for the second prototype chip which fixes the DAC output ringing problem. We see that the estimated DAC output shows the incomplete settling of a first-order system approximation, and this SAR ADC shows better performance.

We see from these measurements that our DAC settling estimation method is effective.

B. Speed Improvement by using faster SA Algorithm

Fig.7 shows a SNDR comparison of 10-step (binary) and 12-step (non-binary), algorithms for an input frequency of 100kHz, using the second prototype. We see that the 12-step non-binary algorithm achieves better speed performance than the 10-step binary algorithm.

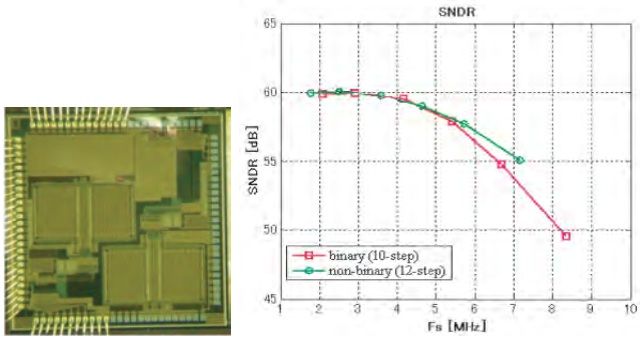


Fig. 7. (Left) Photo of the second chip (2.5mm x 2.5mm) with two SAR ADCs. (Right) SNDR comparison of 10-step (binary) and 12-step (non-binary), with respect to sampling frequency F_s.

VIII. Conclusion

We have proposed a non-binary SAR ADC whose algorithm can be configured at production test time to compensate for CMOS process variation between ADC chips and thus to improve yield (number of chips that satisfy the sampling-rate specification). An ATE is used to determine estimated speed margin and set the optimal algorithm. We have shown measurements and simulations of our SAR ADC design that validate the effectiveness of the proposed architecture.

We conclude this paper by remarking that most of the reconfigurable ADCs proposed by several researchers are reconfigurable to satisfy different specifications, but our reconfigurable ADC proposed here is reconfigurable to meet one sampling-rate specification and save slow chips that would otherwise be rejected – a new concept, we believe.

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References

[1] T. Ogawa, H. Kobayashi, M. Hotta, Y. Takahashi, H. San, N. Takai, "SAR ADC Algorithm with Redundancy," *IEEE Asia Pacific Conference on Circuits and Systems*, Macao, China, pp.268-271 (Dec. 2008).

[2] T. Ogawa, H. Kobayashi, Y. Takahashi, N. Takai, M. Hotta, H. San, T. Matsuura, A. Abe, K. Yagi, T. Mori, "SAR ADC Algorithm with Redundancy and Digital Error Correction," *IEICE Trans. Fundamentals*, vol.E93-A, no.2, pp.415-423 (Feb. 2010).

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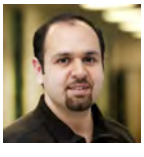

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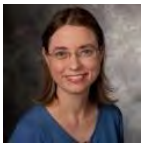

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