Track 1: Analog/Mixed-Signal Circuit Design and Related Technologies

Invited

Revisit to RC Linear Circuit Theory

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Outline

- Objective of This Paper
- Active Resistor Network
  - Spatial and Temporal Dynamics
  - Three New Property Findings
- ReDAC with RC Filter
  - Conventional ReDAC with LPF
  - Proposed ReDAC with HPF
- Conclusion

ReDAC: Relaxation Digital-to-Analog Converter

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Objective of This Paper

To show research for RC linear circuit has not ended yet.

[RC Network Theory]

Spatial and temporal dynamics of active resistor network.

Active resistor network: positive and negative resistors

[Application of RC Circuit]

Relaxation DAC with RC high-pass filter
for positive and negative polarity output

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Research Outline of Active Network Dynamics

Our previous theorem:

Spatial and temporal stability conditions are equivalent for uniform active resistor network

⇩

This paper:

Investigation of spatial and temporal dynamics for non-uniform active resistor network

⇨ Three new findings

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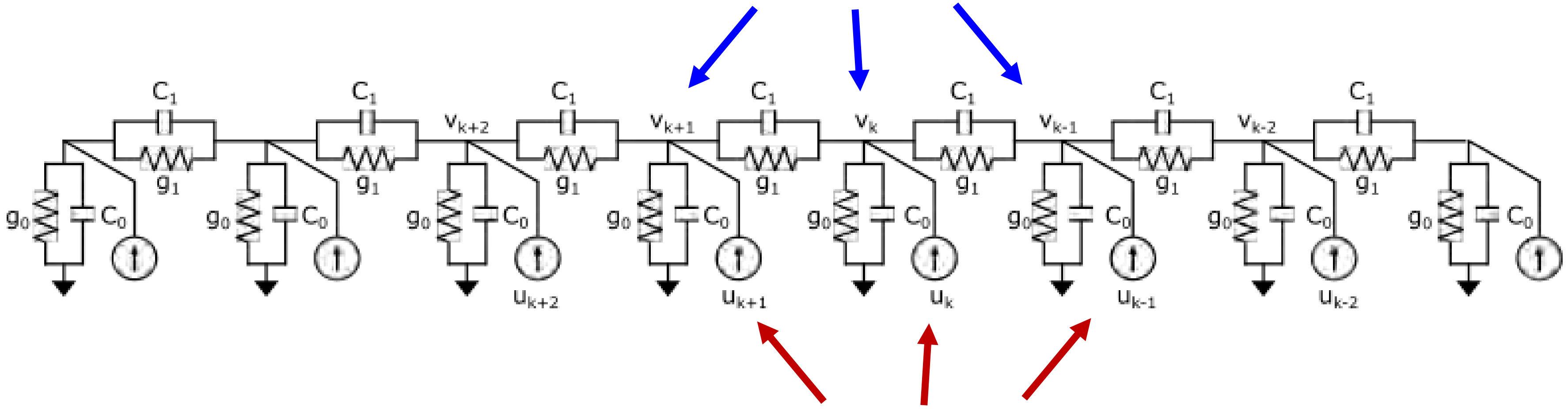
Retina Chip with Positive Resistor Network

High-speed analog image-smoothing processor

1D image case

$g_0 = 1/R_0$
$g_1 = 1/R_1$

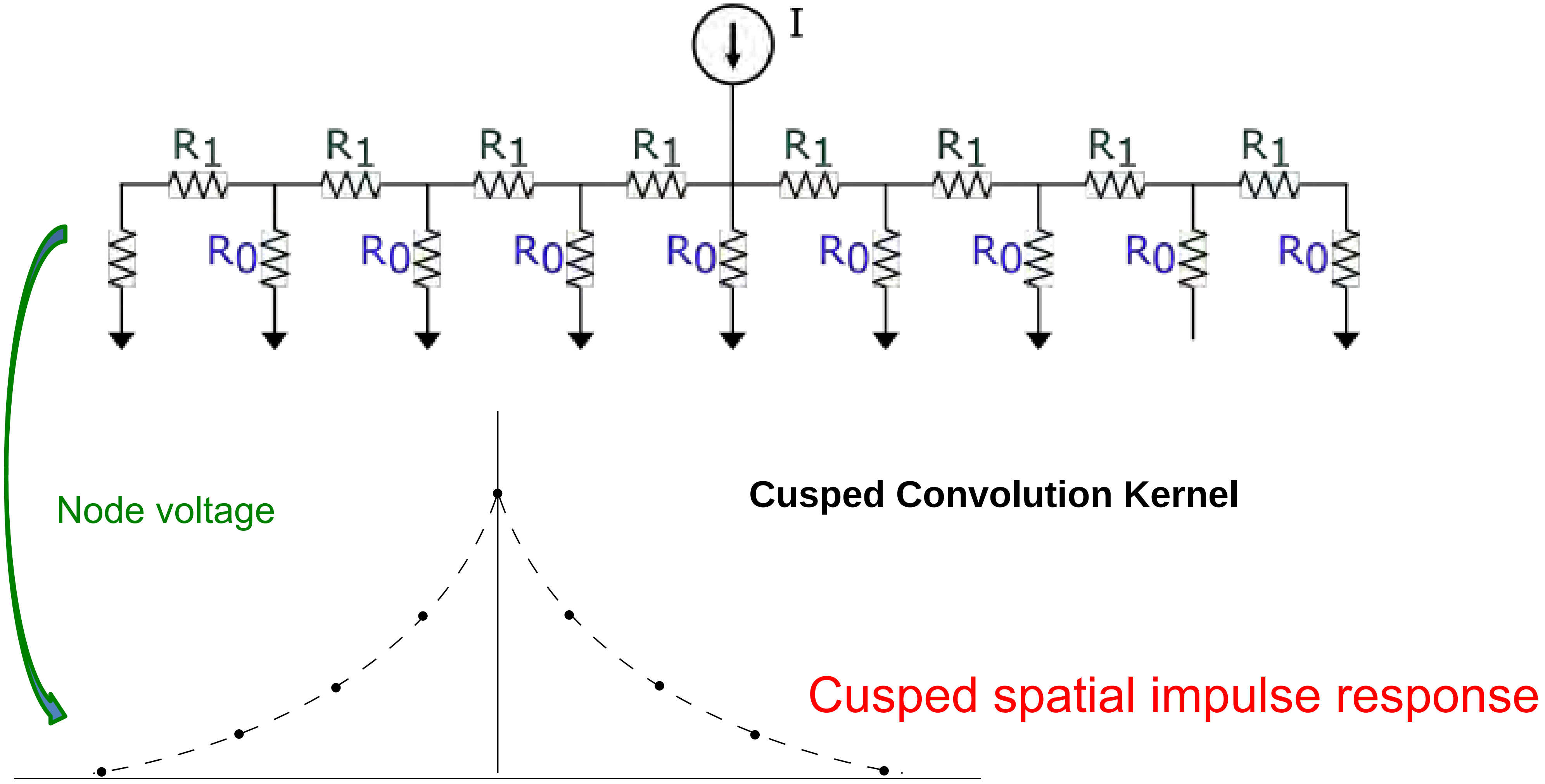
Node voltages： Output image



Injected currents at nodes： Input image

[1] C. A. Mead, Analog VLSI and Neural Systems, Addison Wesley, 1989

Spatial Impulse Response of Retina Chip



Gaussian Chip with Active Resistor Network

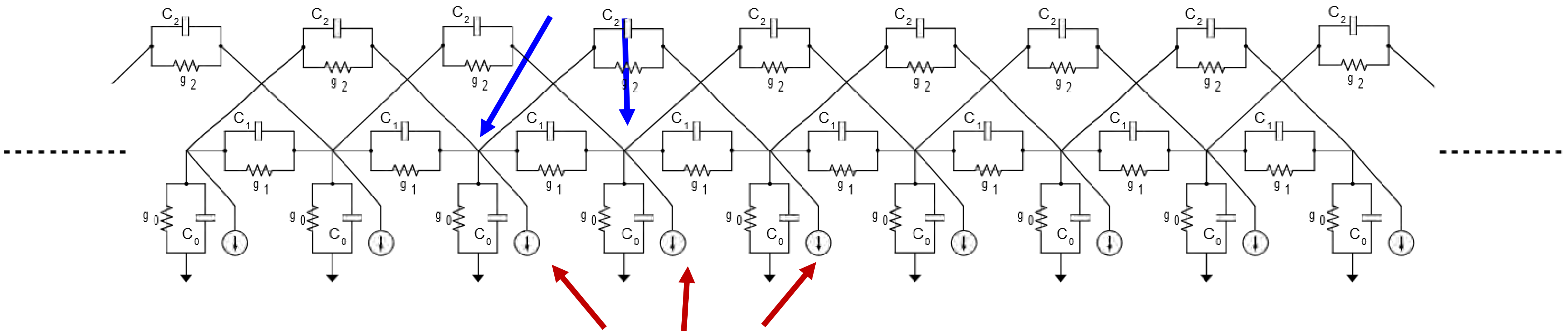
High-speed analog image processor

$g_0 = 1/R_0$
$g_1 = 1/R_1$
$g_2 = 1/R_2$

1D image case

Negative resistor $R2 = -4R1 < 0$

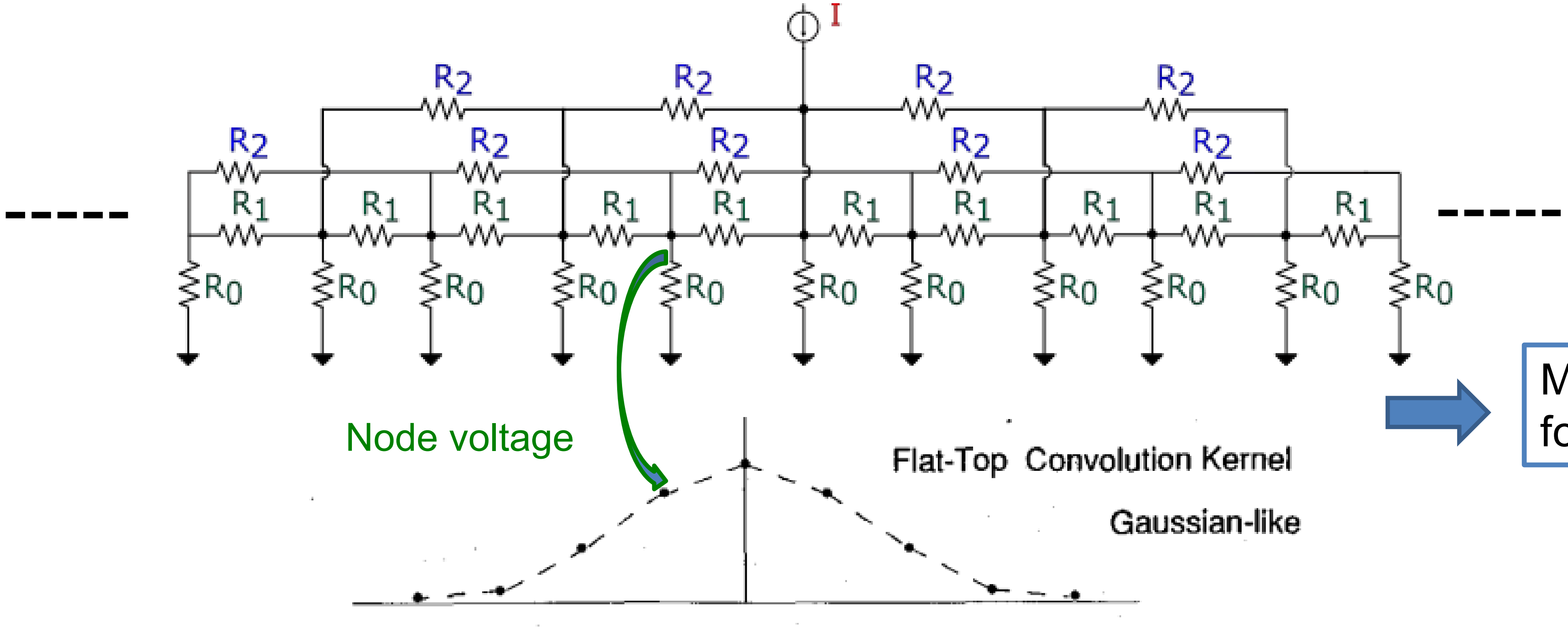
Node voltages : Output image



Injected currents at nodes : Input image

[2] H. Kobayashi, J. L. White, A. A. Abidi, “An Active Resistor Network for Gaussian Filtering of Images", IEEE Journal of Solid-State Circuits (May 1991)

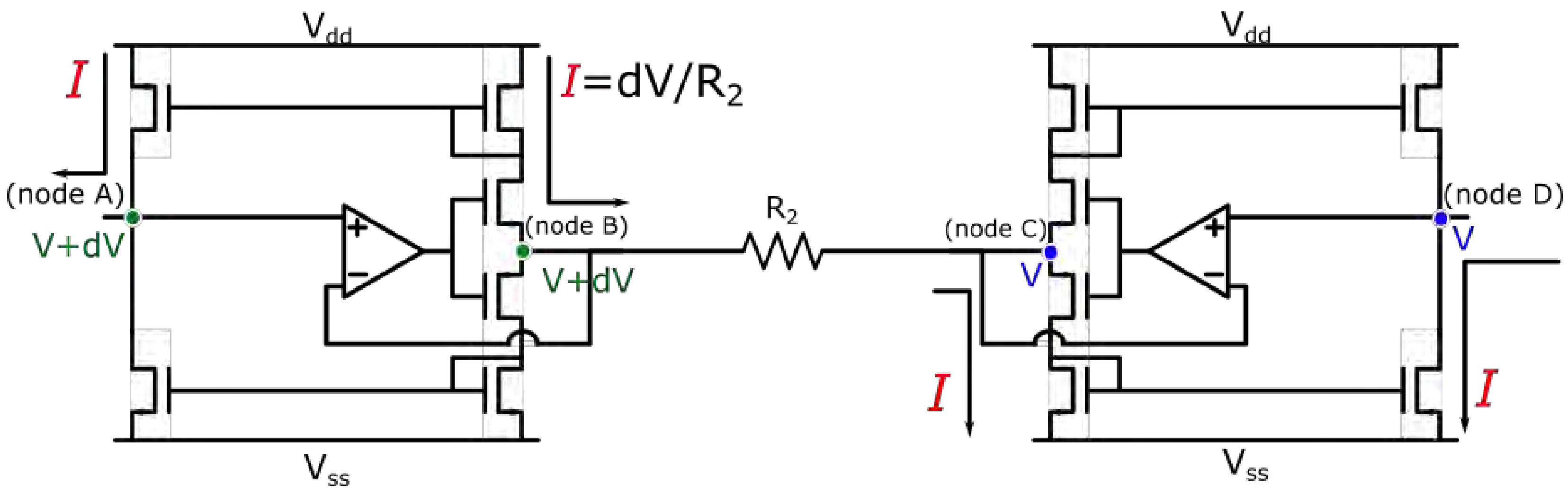
Spatial Impulse Response of Gaussian Chip

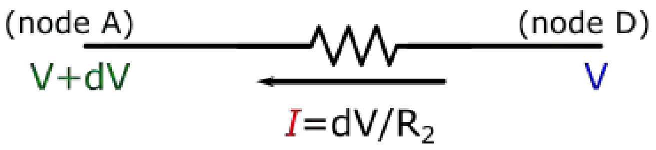


More desirable for image processing

Flat-top spatial impulse response

Negative Resistor with Standard CMOS

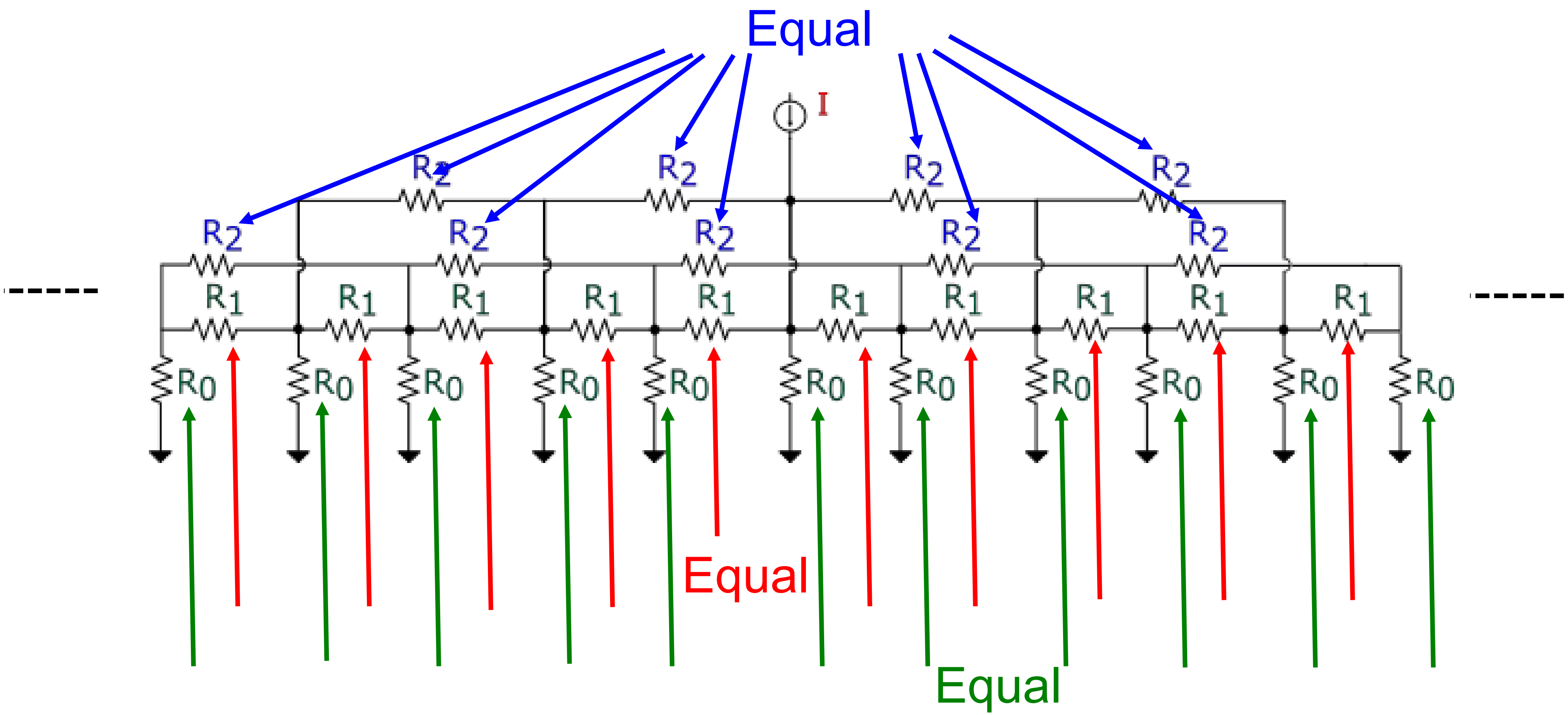




V+dV @ Node A > V @ Node B

Current $I = \frac{dV}{R_2}$

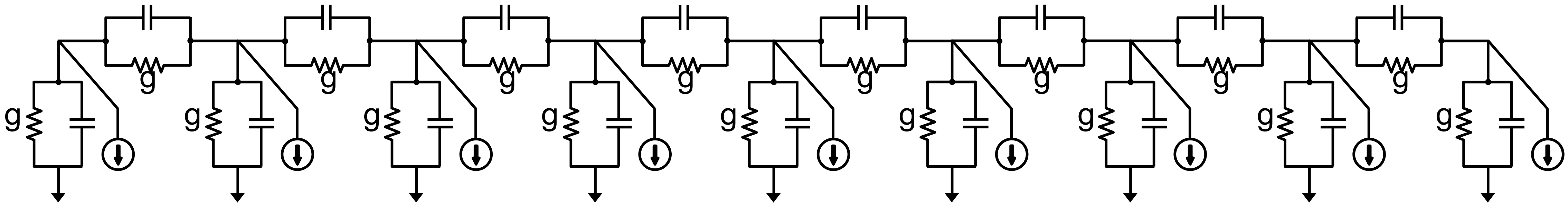
Uniform Resistor Network for Spatial Dynamics

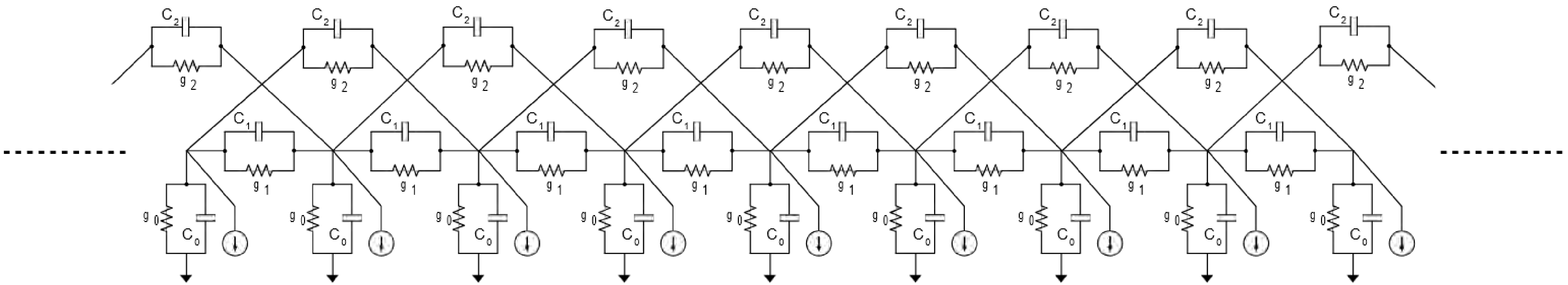


- Shift invariant
- Spatial transfer function can be defined

Temporal Dynamics with R, C

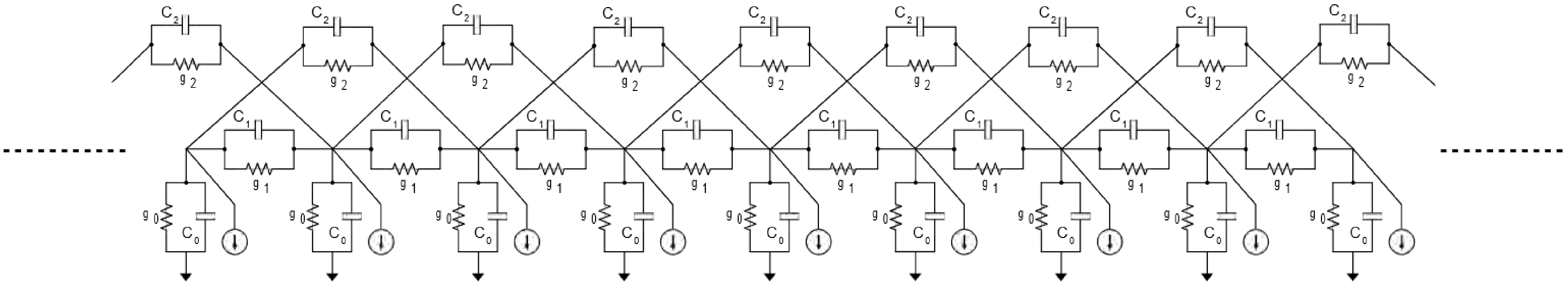
Capacitances are considered for temporal dynamics





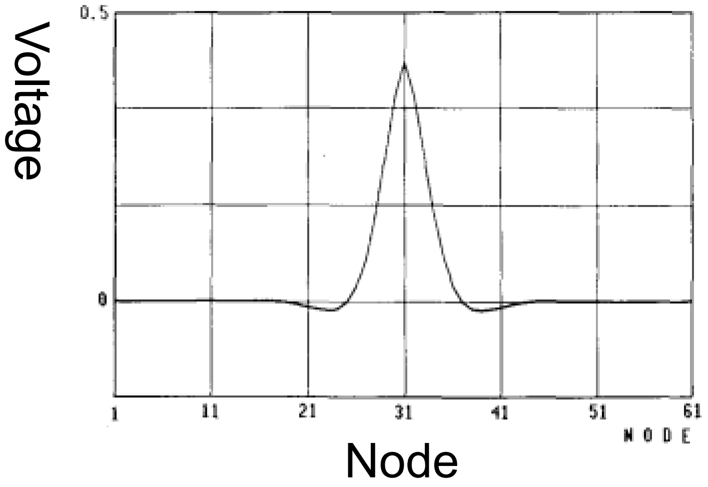
Simulation Results: Spatial Temporal Stabilities

$R_0 = 1/g_0 = 200\text{k}\Omega, \quad R_1 = 1/g_1 = 5\text{k}\Omega, \quad R_2 = 1/g_2 = -20\text{k}\Omega$

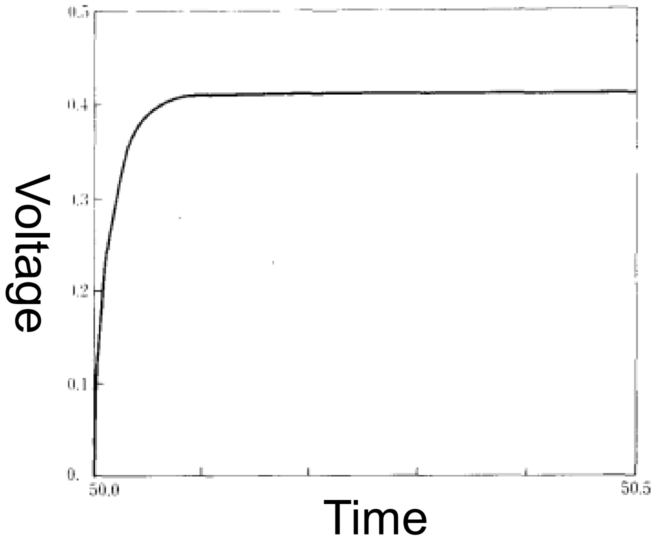


Spatially stable

Spatial impulse response



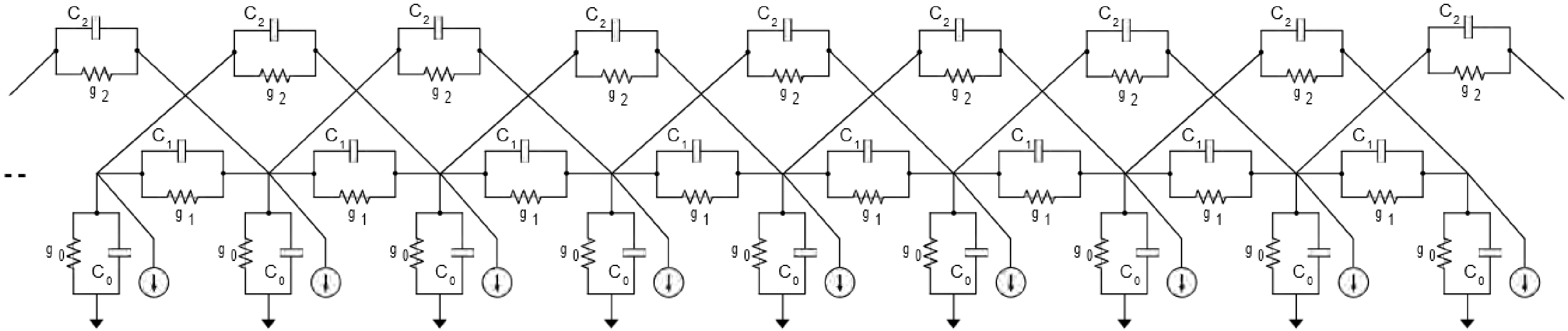
Temporally stable



Temporal step response

Simulation Results: Spatial Temporal Instabilities

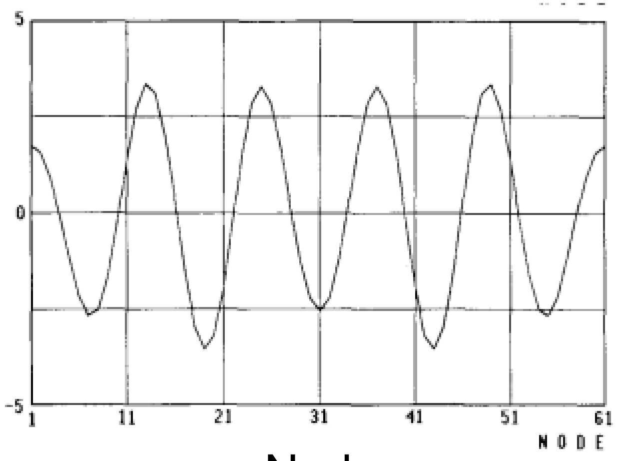
$R_0 = 1/g_0 = 200\text{k}\Omega, \quad R_1 = 1/g_1 = 5\text{k}\Omega, \quad R_2 = 1/g_2 = -17\text{k}\Omega$



Spatially unstable

Spatial impulse response

Voltage

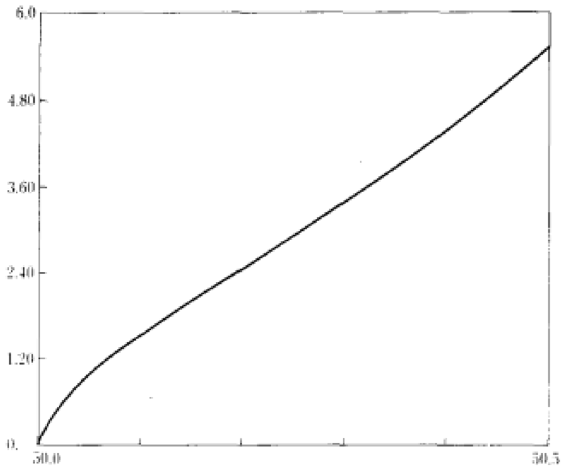


Node

Temporally unstable

Temporal step response

Voltage



Time

Circuit Network Theorem

For uniform network with positive and negative resistors, spatial and temporal stability conditions are equivalent.

[3] T. Matsumoto, H. Kobayashi, Y. Togawa,
"Spatial Versus Temporal Stability Issues in Image Processing Neuro hips ",
IEEE Trans. Neural Networks, (July 1992).

[4] H. Kobayashi, T. Matsumoto, J. Sanekata,
"Two-Dimensional Spatio-Temporal Dynamics of Analog Image Processing Neural Networks",
IEEE Trans. Neural Networks (Oct. 1995).

How about non-uniform network ?

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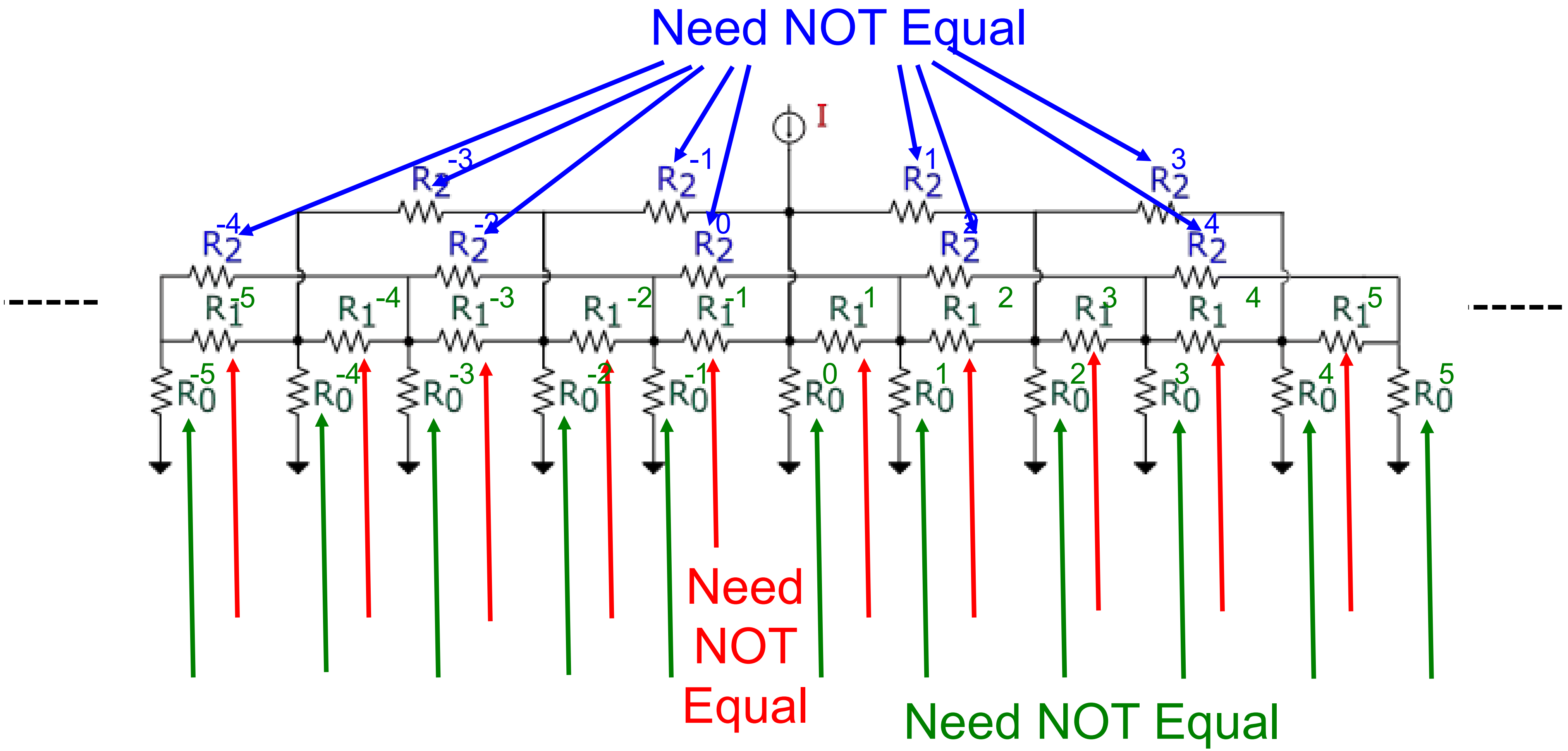
Non-Uniform Resistor Network

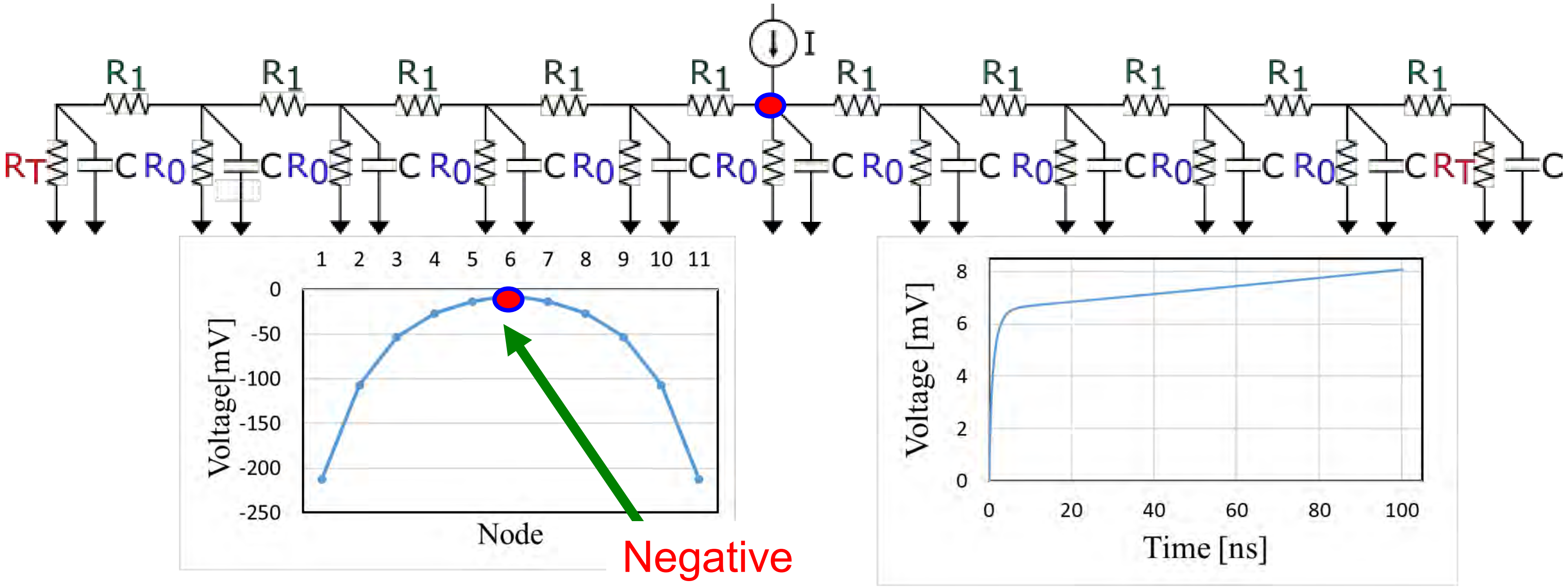


- Shift variant
- Spatial transfer function CANNOT be defined

Finding 1

If there is a node where the input current is injected and its node voltage as the spatial impulse response is negative,

⇒ the network is temporally unstable



$R_0 = 2\text{k}\Omega$

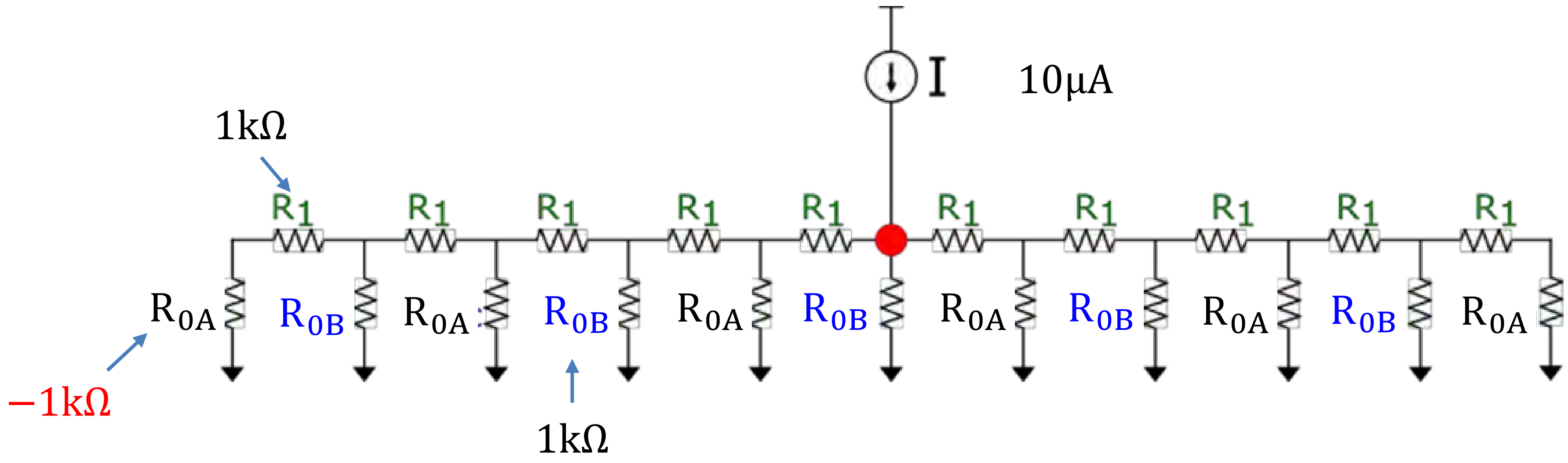
$R_1 = 1\text{k}\Omega$

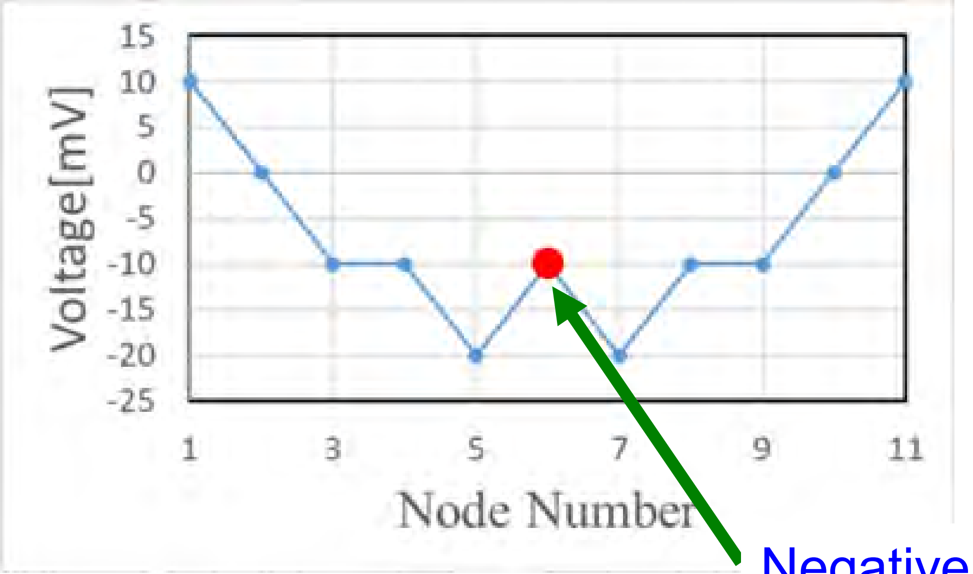
$R_\text{T} = -2\text{k}\Omega$

Spatial Impulse Response

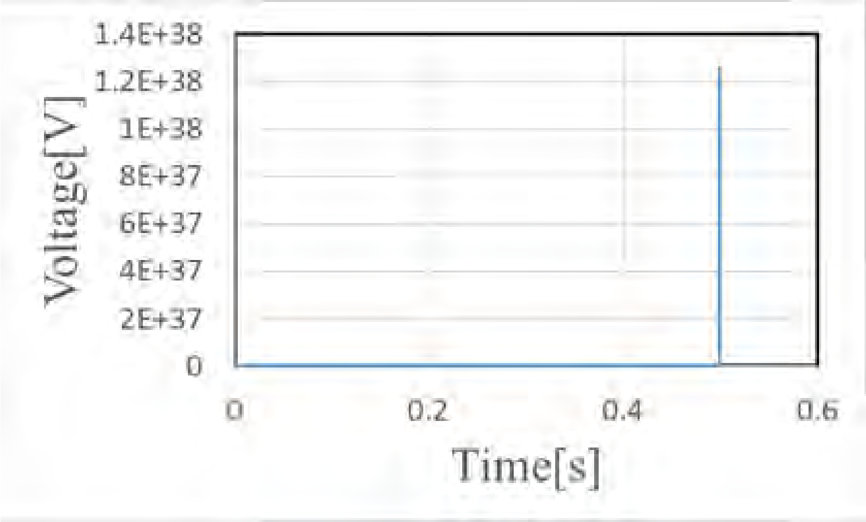
Temporally unstable

1^{st} Nearest Connection (2)



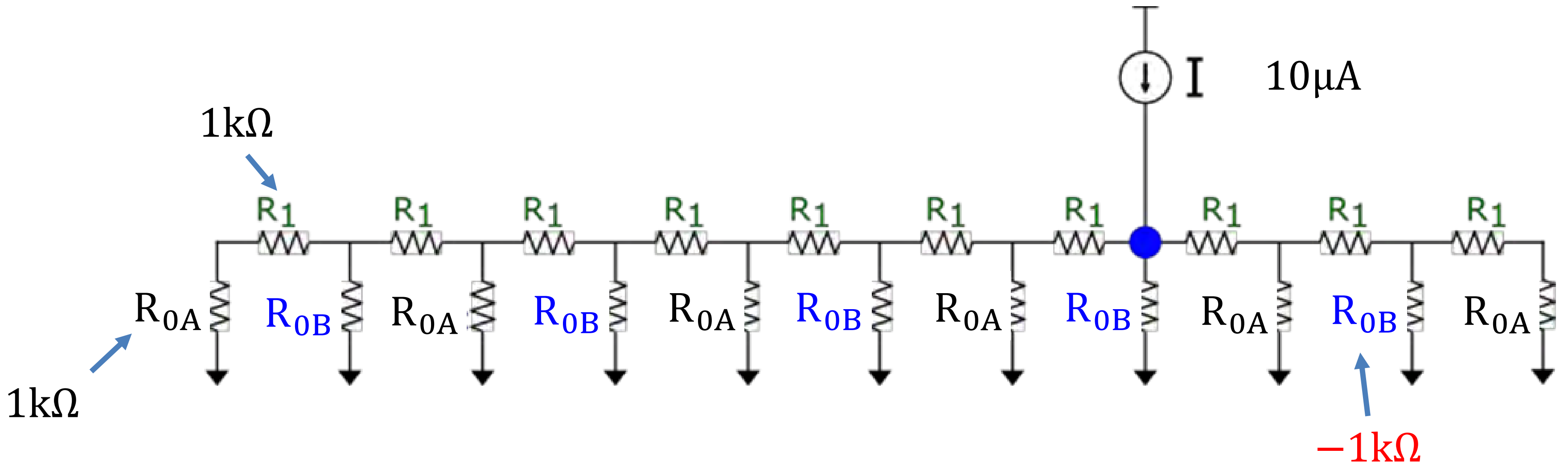


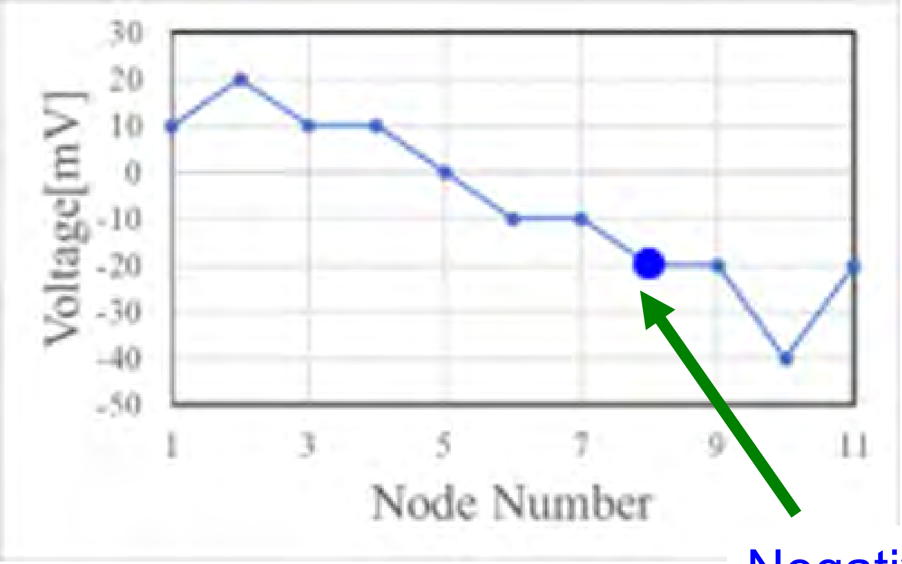
Negative



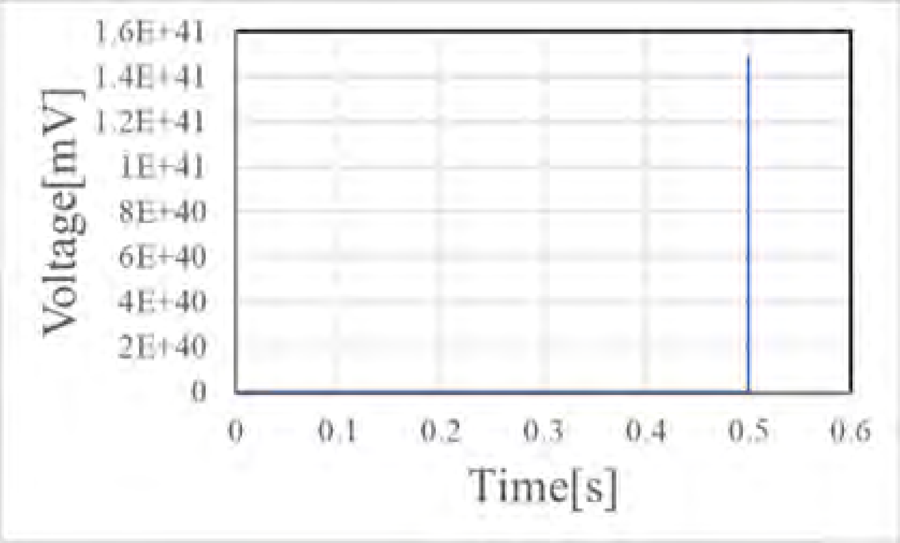
Temporally Unstable

1st Nearest Connection (3)



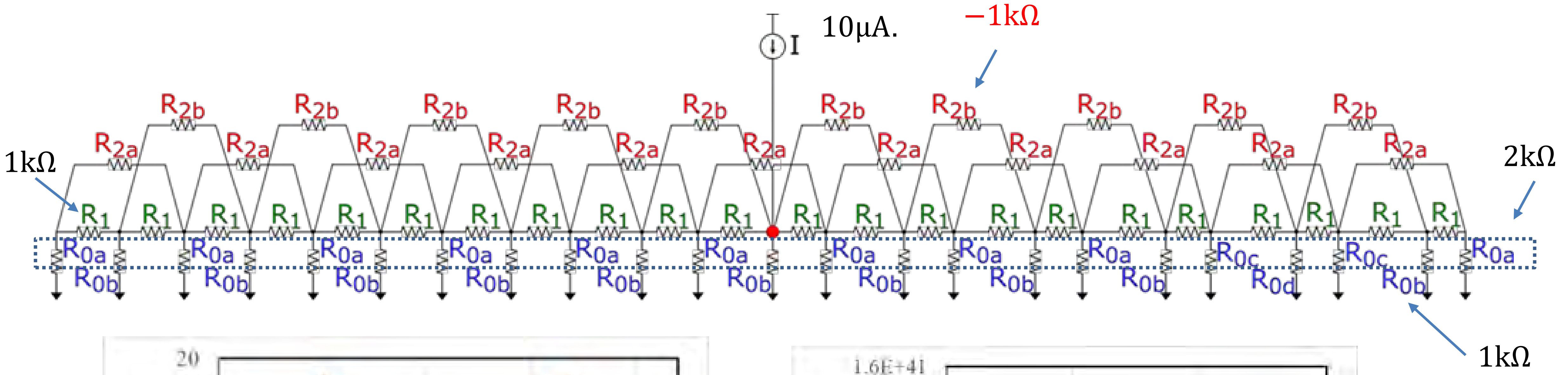


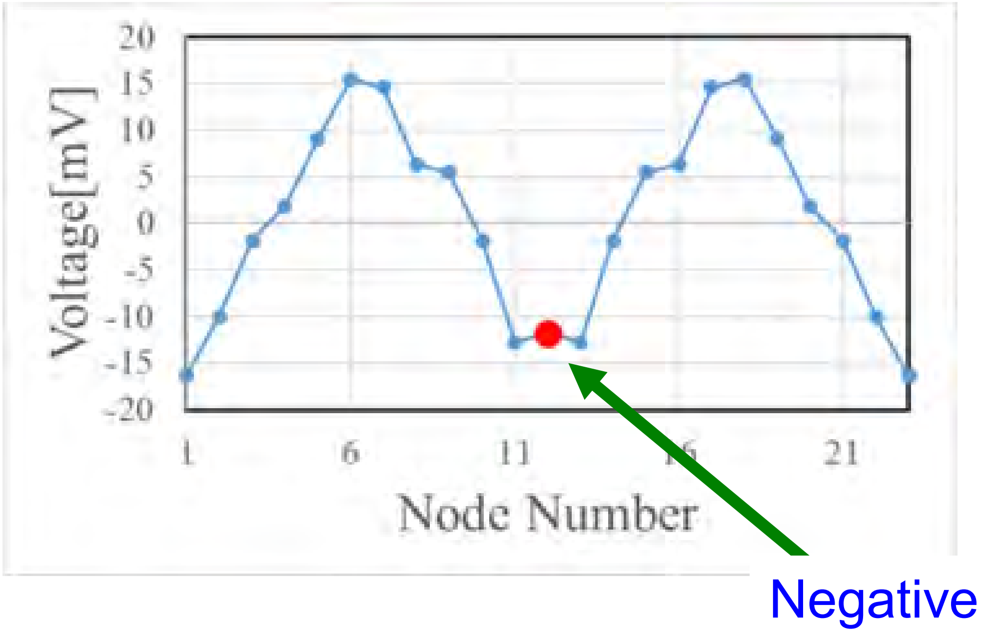
Negative

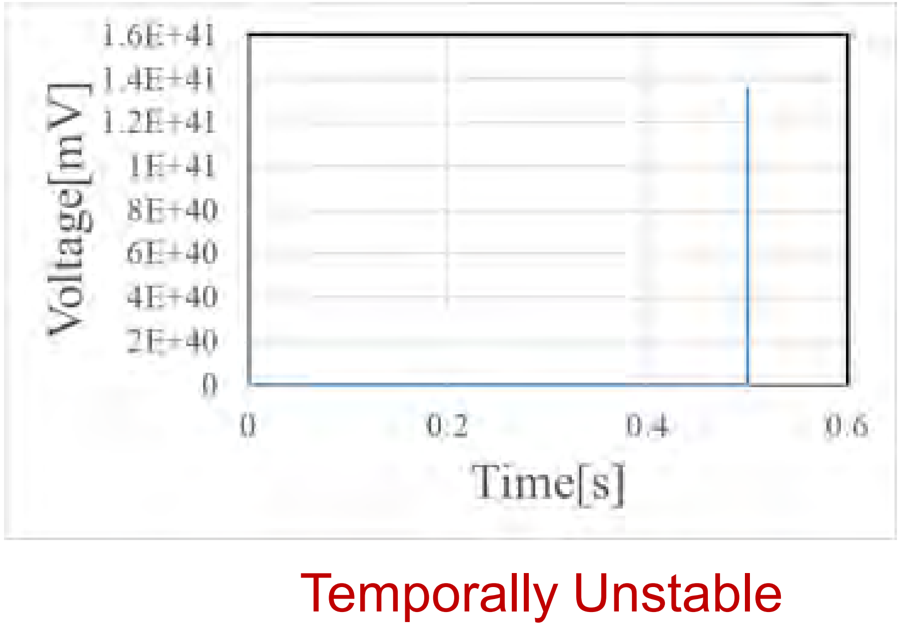


Temporally Unstable

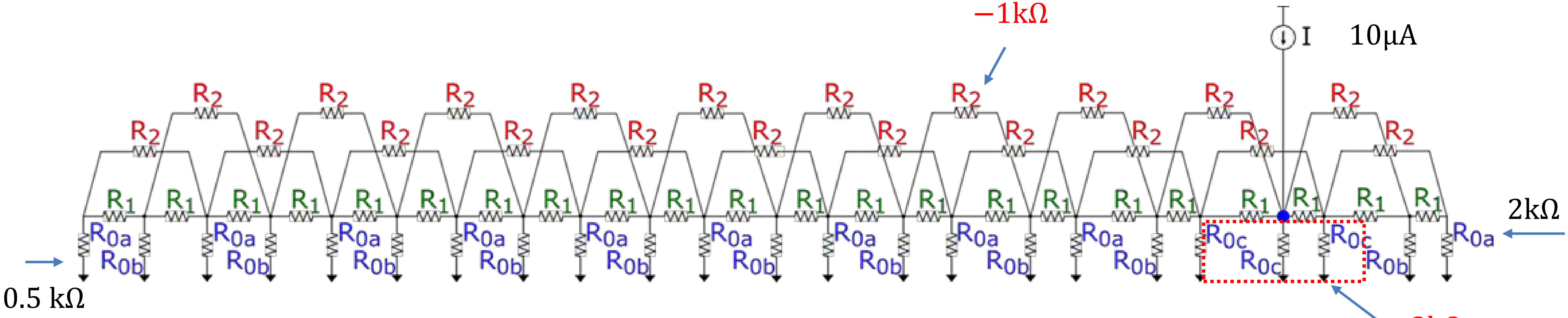
2nd Nearest Connection (1)

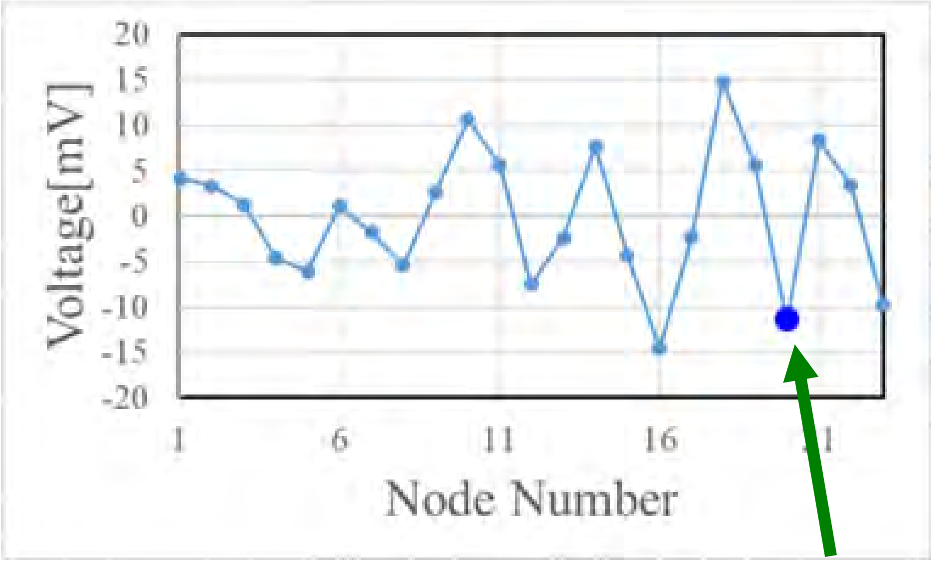




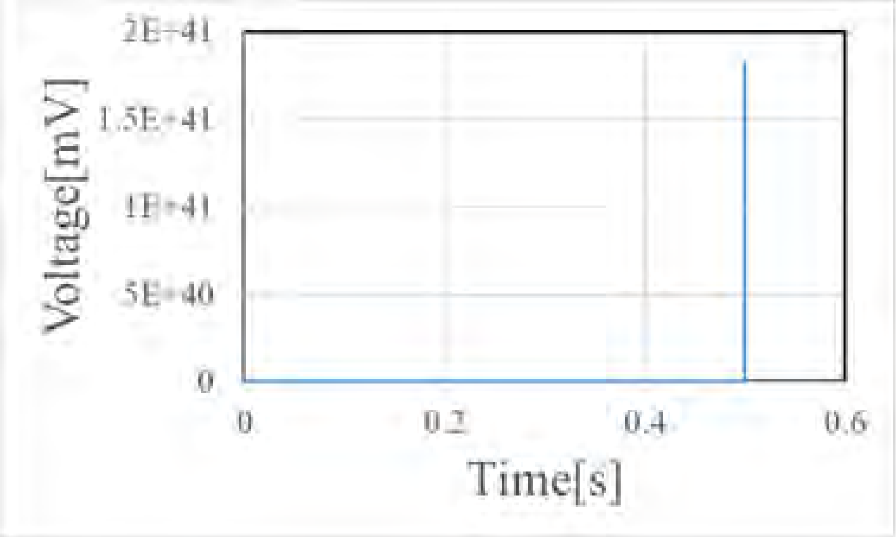


2^{nd} Nearest Connection (2)



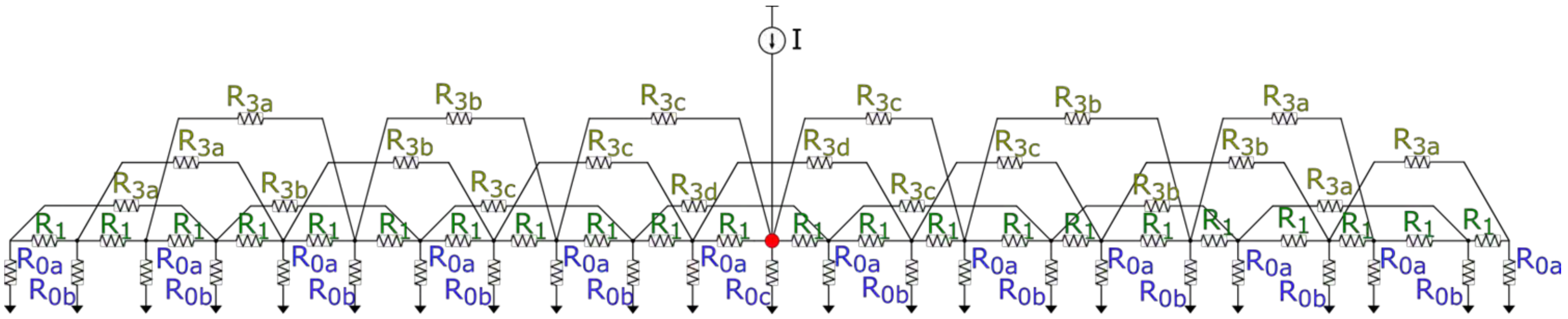


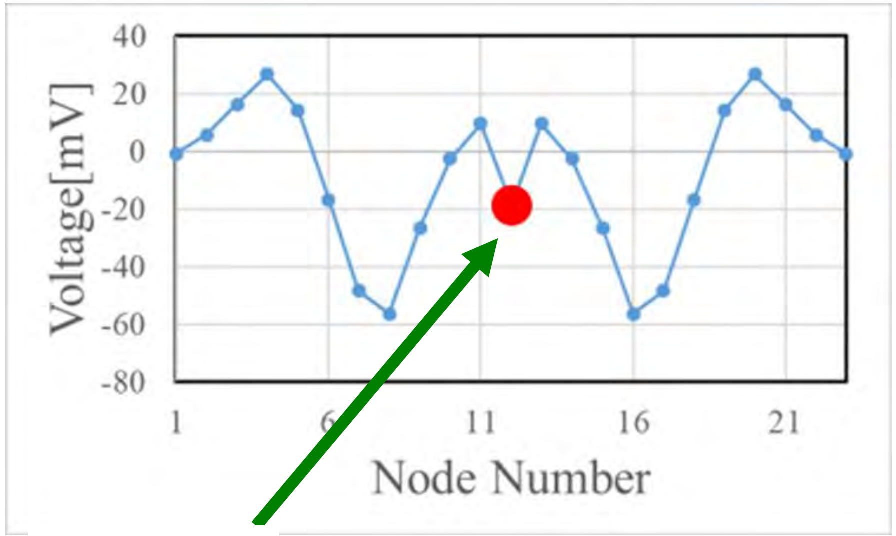
Negative



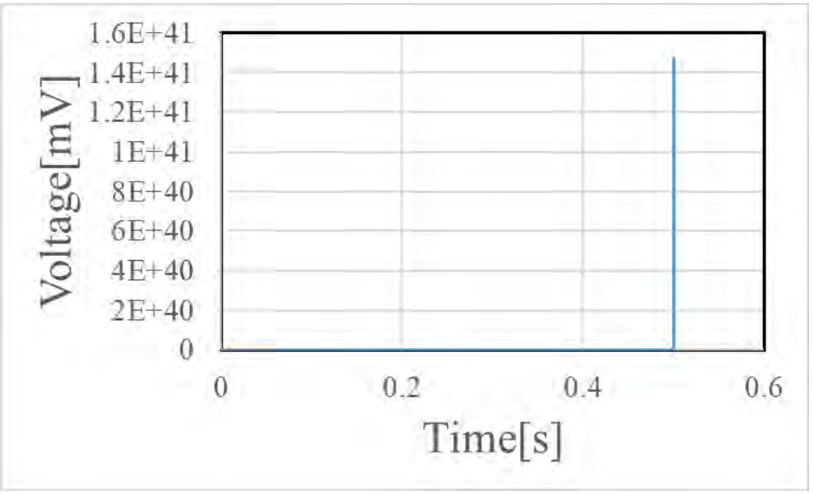
Temporally Unstable

3rd Nearest Connection





Negative



Temporally Unstable

$$R_{0a} = 2k\Omega, R_{0b} = 3k\Omega, R_{0c} = -0.25k, R_1 = 1k\Omega, R_{3a} = -4k\Omega$$
$$R_{3b} = -3k, R_{3c} = -2k, R_{3d} = -1k\Omega, I = 10\mu A$$

Finding 2

For all nodes,

“The input current is injected at each one node and

its node voltage as the spatial impulse response is positive”,

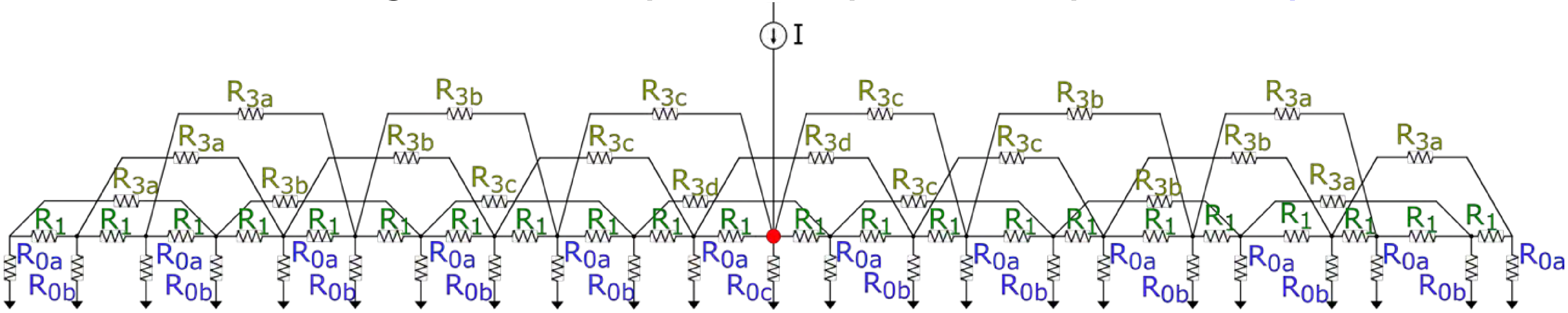
⇒ *Some networks can be temporally unstable.*

We have found such an example by simulation

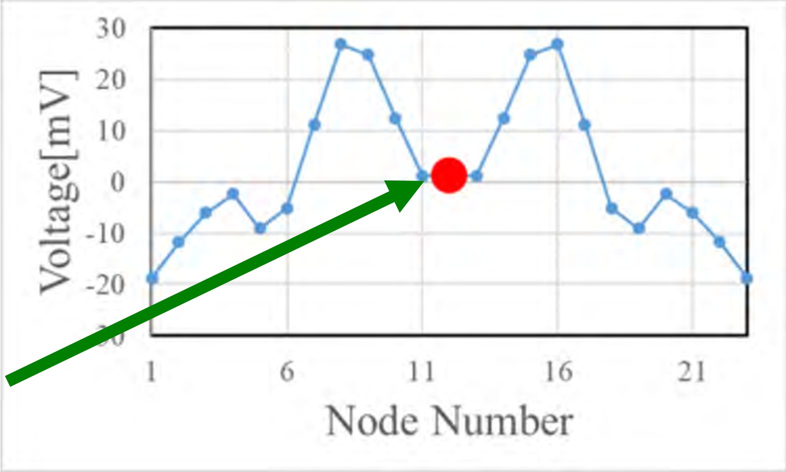
Theoretical analysis is left.

3rd Nearest Connection

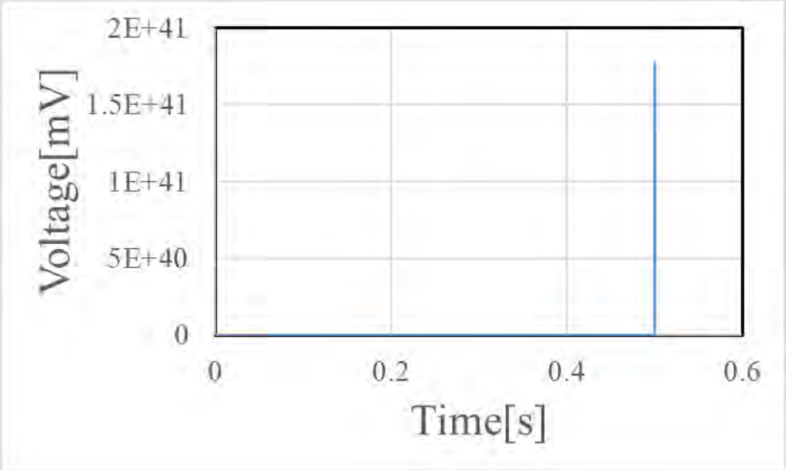
For all nodes, "the input current is injected at a node and its node voltage as the spatial impulse response is positive",



$R_{0a} = 2\text{k}\Omega$, $R_{0b} = 3\text{k}\Omega$, $R_{0c} = -0.25\text{k}$, $R_1 = 1\text{k}\Omega$, $R_{3a} = -1\text{k}$, $R_{3b} = -2\text{k}$, $R_{3c} = -3\text{k}$, $R_{3d} = -4\text{k}\Omega$, $I = 10\mu\text{A}$



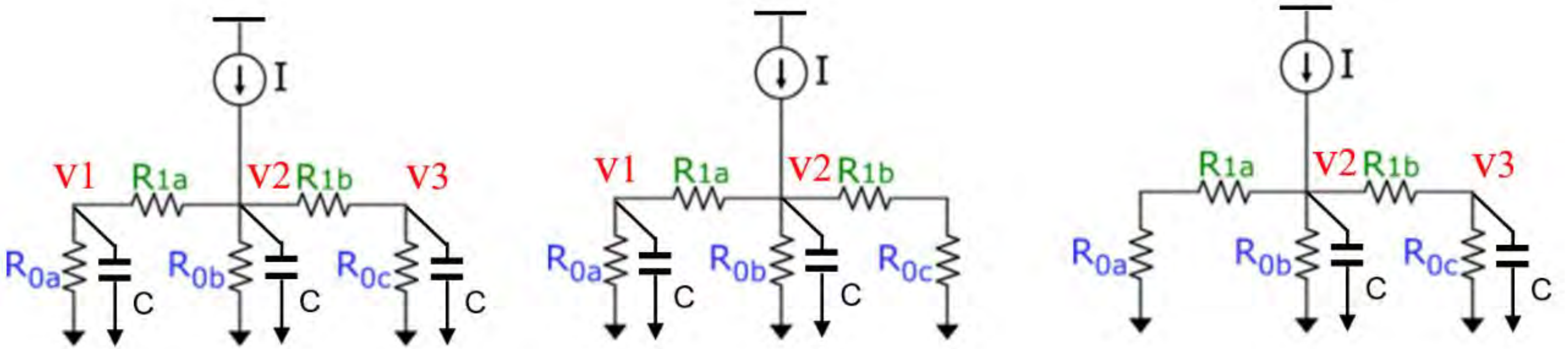
Positive



Temporally Unstable

Finding 3

Temporal stability and instability can depend on capacitors (C) from nodes to ground.



$R_{0a} = -1\ k\Omega$, $R_{0b} = 1\ k\Omega$, $R_{0c} = 0.5\ k\Omega$, $R_{1a} = -1\ k\Omega$, $R_{1b} = 0.5\ k\Omega$, $I = 10\ \mu A$,

Temporally Unstable | Unstable | Stable

→ Proved with theory

Our Three New Findings

For general non-uniform active resistor network dynamics, three new properties have been found with simulation and theoretical analysis.

Their rigorous proof has NOT been completed yet.

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ReDAC: Relaxation Digital-to-Analog Converter

Outline

From Politecnico di Torino, Italy

[5] P. S. Crovetti, et. al.,
“Relaxation Digital-to-Analogue onverter ,” Electronics Letters, 2 9.
[6] R. Rubino, et al.
“Design of Relaxation Digital-to-Analogue onverters f or IoT Applications in 4 nm MOS,”
APCCAS 2019.

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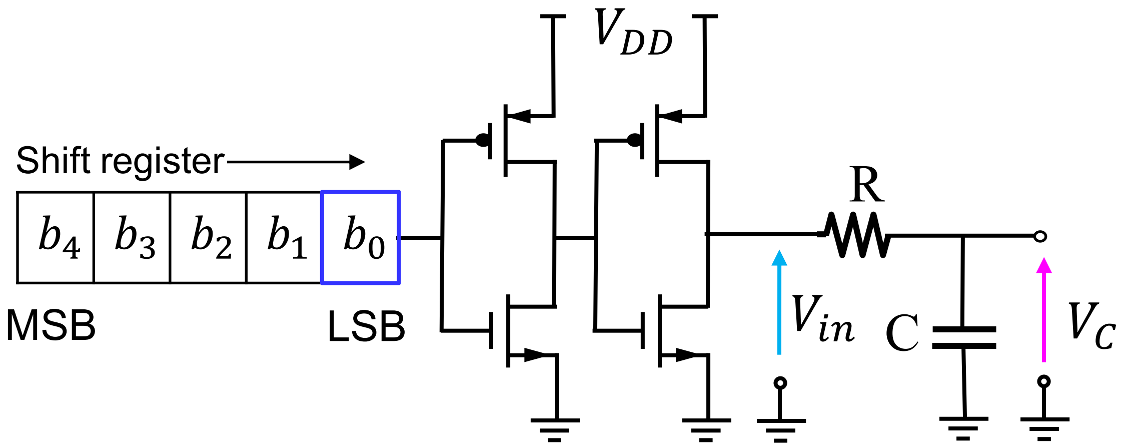
Configuration and Operation of Conventional (1)



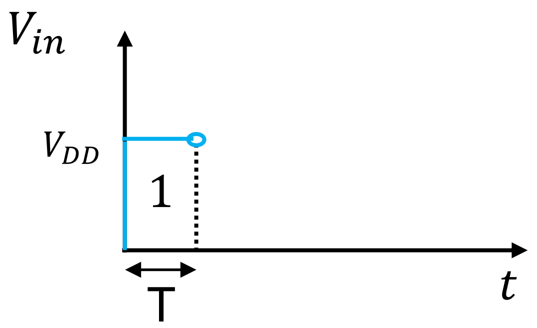
■ Digital input bit stream $b_{n-1} \dots b_0$

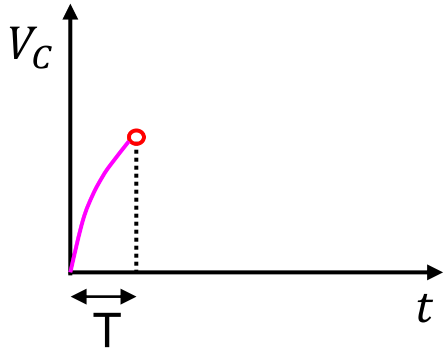
⇨ RC LPF network

LSB-first

Digital Input code

$$N = \sum_{i=0}^{n-1} b_i 2^i$$



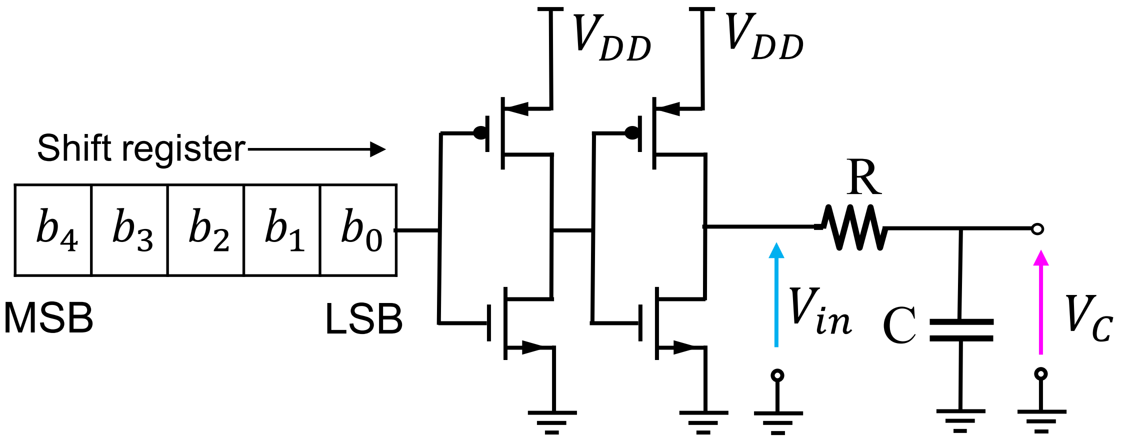


Ex: N=5 ($b_4 b_3 b_2 b_1 b_0$=00101)

$$N = 1 \cdot 2^0 + 0 \cdot 2^1 + 1 \cdot 2^2 + 0 \cdot 2^3 + 0 \cdot 2^4 = 5$$

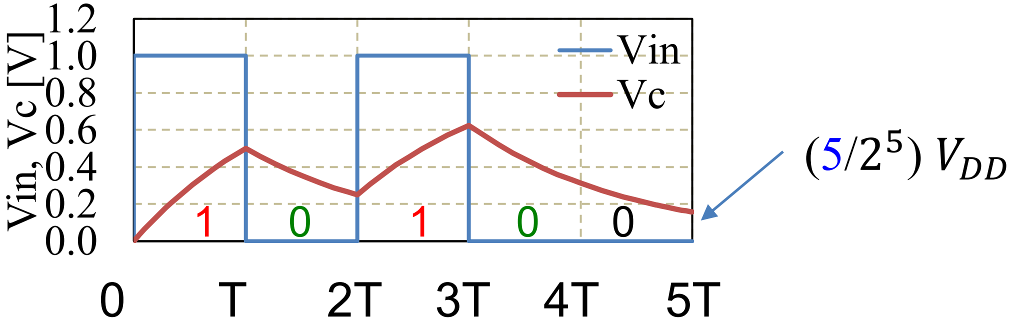
Condition $T = RC \cdot \log 2$

Configuration and Operation of Conventional (2)



RC LPF
$\tau = RC$

Ex: N=5 ($b_4b_3b_2b_1b_0$=00101)



Final capacitor voltage
→ Conversion result

$$V_C(nT) = V_{DD}\left(1 - e^{-\frac{T}{\tau}}\right) \cdot \sum_{i=0}^{n-1} b_i e^{-\frac{(n-i-1)T}{\tau}}$$

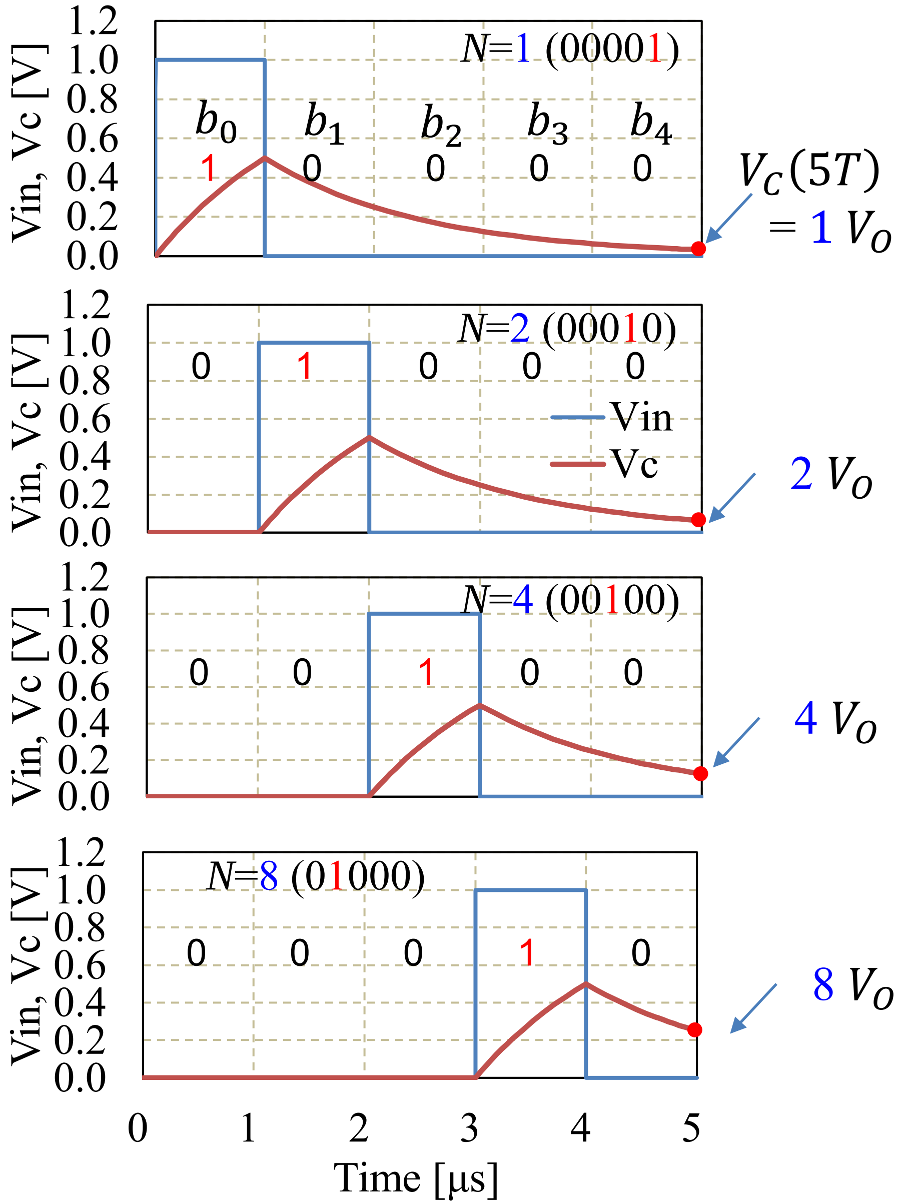
Condition

$$e^{-\frac{T}{\tau}} = \frac{1}{2} \Rightarrow T = \tau \cdot \log 2$$

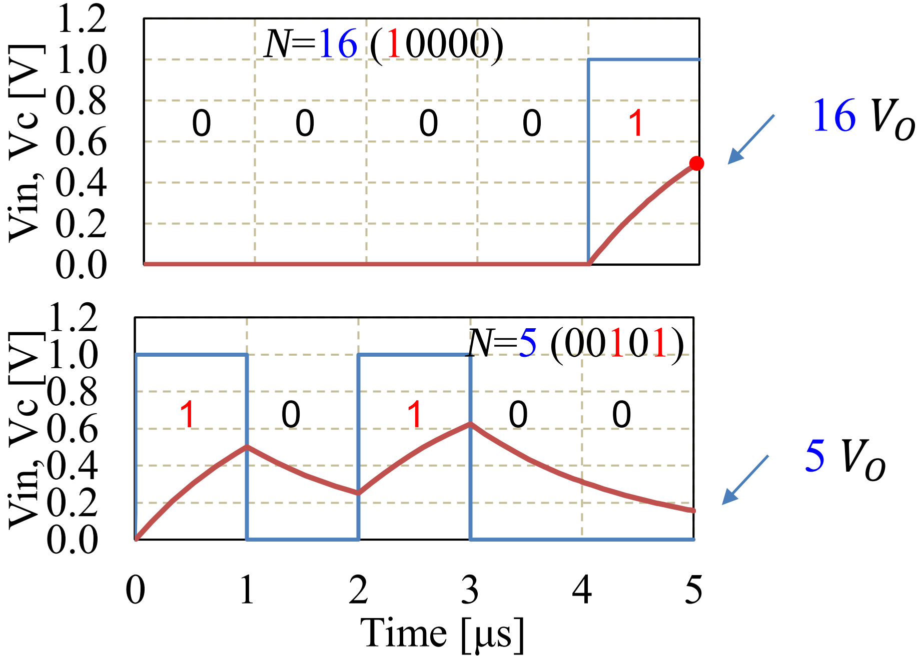
$$V_C(nT) = \frac{V_{DD}}{2^n}\sum_{i=0}^{n-1} b_i 2^i = \frac{N}{2^n} \cdot V_{DD}$$

Output voltage proportional to N

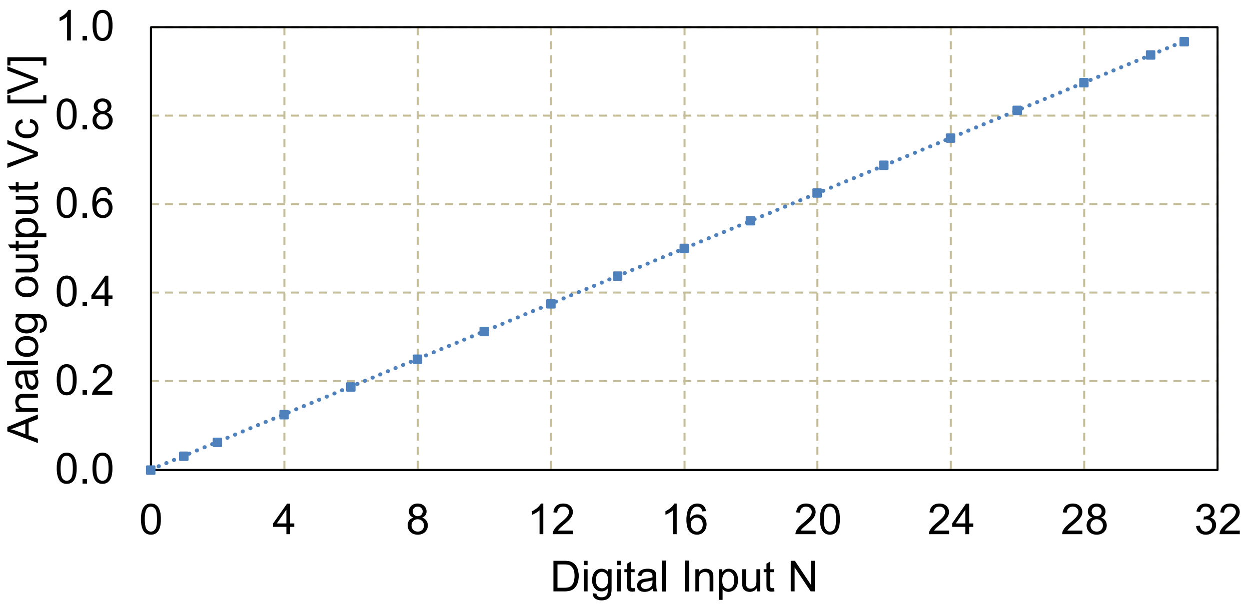
Simulation Verification of Conventional (1)



parameter	value
R	1 kΩ
C	1.443 nF
T	1 μs
V_{DD}	1 V



Simulation Verification of Conventional (2)



- Analog output is proportional to digital input data N.
- Analog output generates with only positive polarity.

➡ Negative digital input data is not available.

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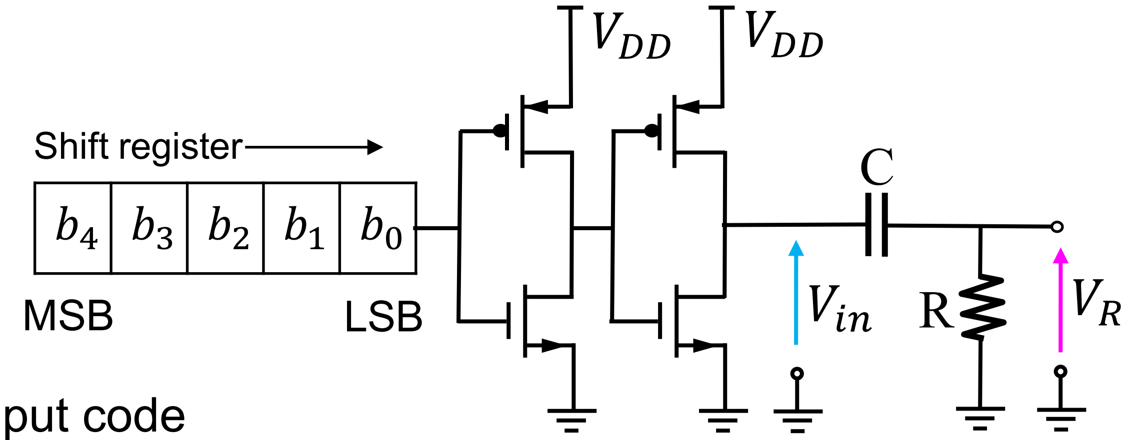
Configuration and Operation of Proposal (1)



■ Digital input bit stream $b_{n-1} \dots b_0$

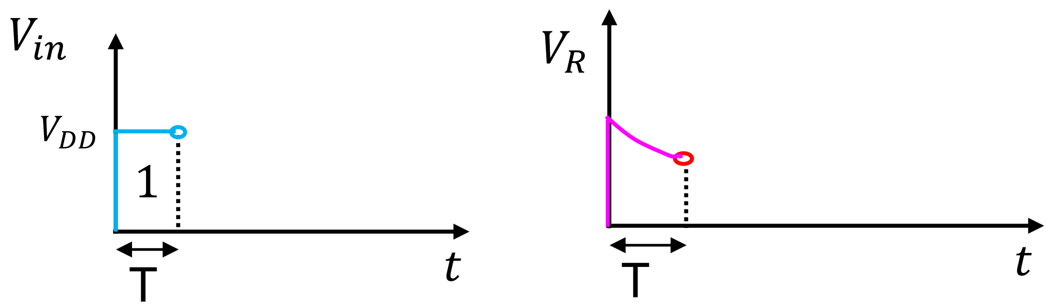
➡ RC HPF network

LSB-first

Digital input code

$$N = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i$$

Two's complement format

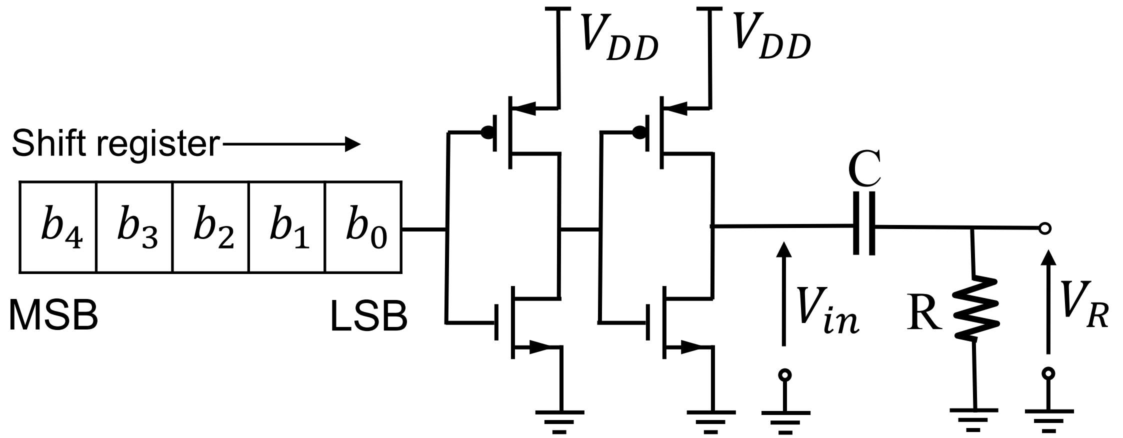


Ex: N=-11 ($b_4b_3b_2b_1b_0$=10101)

$$\mathrm{N} = 1 \cdot 2^0 + 0 \cdot 2^1 + 1 \cdot 2^2 + 0 \cdot 2^3 - 1 \cdot 2^4 = -$$

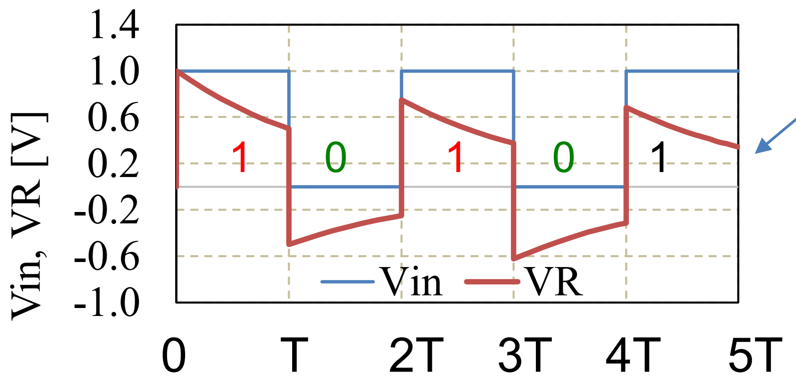
Condition $T = RC \cdot \log 2$

Configuration and Operation of Proposal (2)



RC HPF
$\tau = RC$

Ex: N=-11 ($b_4 b_3 b_2 b_1 b_0$=10101)



$-(-11/2^5)\, V_{DD}$

$= (11/2^5)\, V_{DD}$

Final resistor voltage
→ Conversion result

$$V_R(nT) = -V_{DD}\left(-b_{n-1} e^{\frac{(n-1)T}{\tau}} + \sum_{i=0}^{n-2} b_i e^{-\frac{(n-i-1)T}{\tau}}\right)$$

Condition

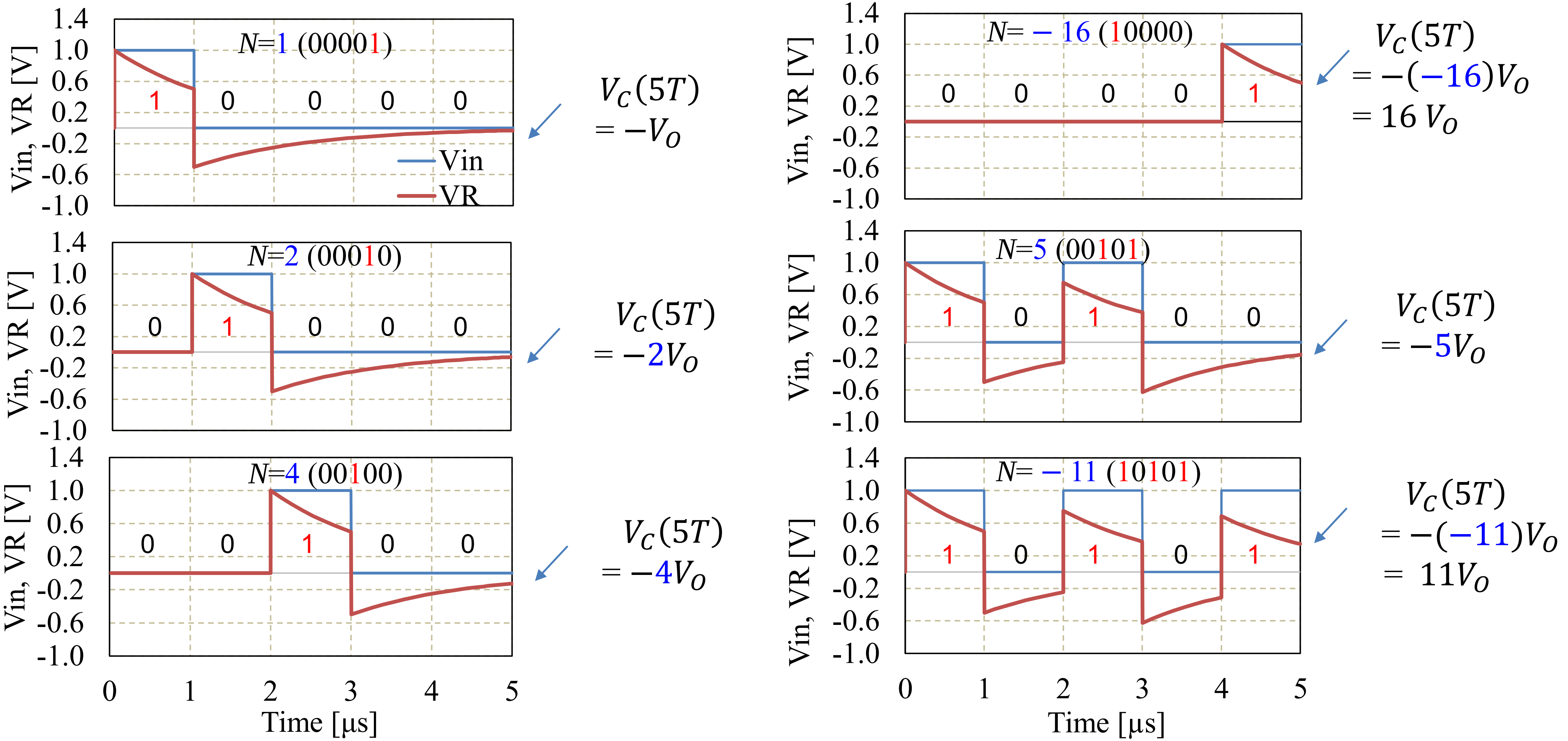
$$e^{-\frac{T}{\tau}} = \frac{1}{2} \Rightarrow T = \tau \cdot \log 2$$

$$V_R(nT) = -\frac{V_{DD}}{2^n}\left(-b_{n-1} 2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i\right)$$

$$= -\frac{N}{2^n} \cdot V_{DD}$$

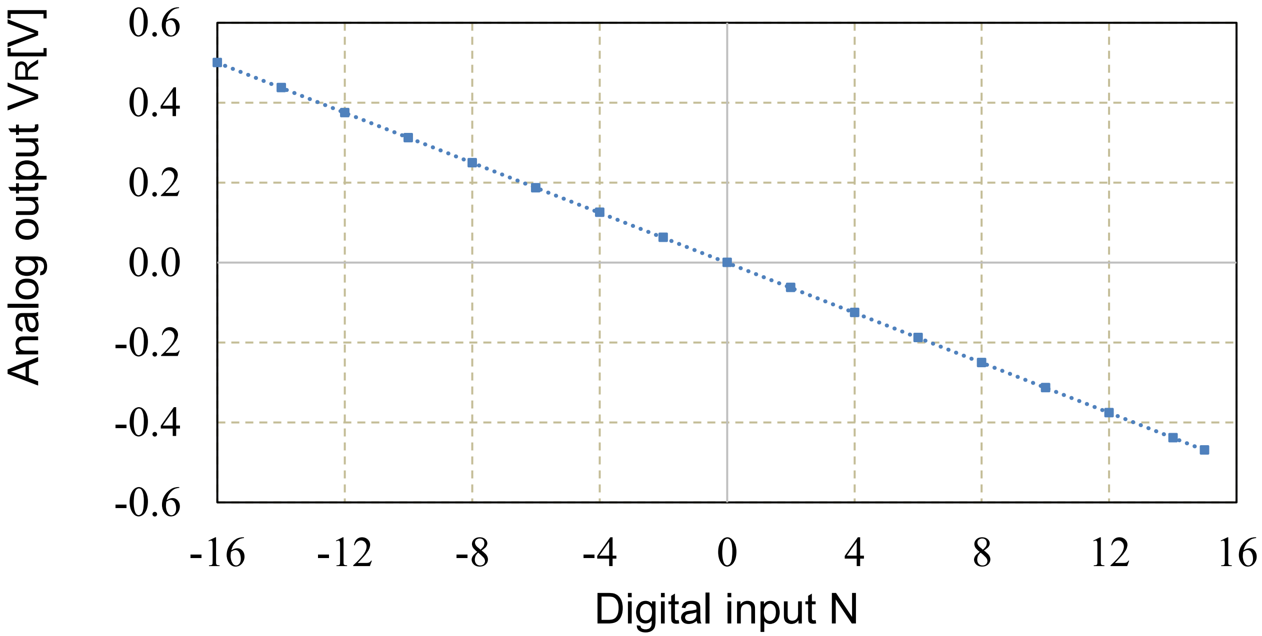
Output Voltage proportional to N

Simulation Verification of Proposal (1)



- $V_R(5T)|_{N=5} = V_R(5T)|_{N=1} + V_R(5T)|_{N=4}$
- $V_R(5T)|_{N=-11} = V_R(5T)|_{N=1} + V_R(5T)|_{N=4} + V_R(5T)|_{N=-16}$

Simulation Verification of Proposal (2)



- Analog output is proportional to the digital input data N.
- Positive and negative polarity output can be generated.
- Digital input data is in two's complement format.

Outline

- Objective of This Paper
- Active Resistor Network
  - Spatial and Temporal Dynamics
  - Three New Property Findngs
- ReDAC with RC Filter
  - Conventional ReDAC with LPF
  - Proposed ReDAC with HPF
- Conclusion

Conclusion

We have shown the following:

- Spatial and temporal dynamics of active resistor network have close relationships ➡ Theoretical analysis is left.

- Relaxation DAC with RC HPF produces positive and negative polarity output for digital input data in two’s complement format.

➡ RC linear networks still have challenges in circuit theory and application

References

Active Resistor Network Dynamics

[1] M. Chiba, H. Kobayashi, et. al., "Spatial and Temporal Dynamics of Non-Uniform Active Resistor Networks", IEEE 16th ICSICT (Oct. 2022).

[2] K. Otomo, H. Kobayashi, et. al., "Conjecture on Spatial-Temporal Response Relationship for Spatially Shift-Variant Networks with Positive and Negative Resistors", 6th ICTSS (Dec. 2022).

ReDAC with HPF

[3] L. Nengvang, H. Kobayashi, et. al., "Relaxation DAC with Positive and Negative Polarity Output using High-Pass Filter", IEICE Electronics Express (Feb. 2023).