2023 年 6 月 2 日(金)

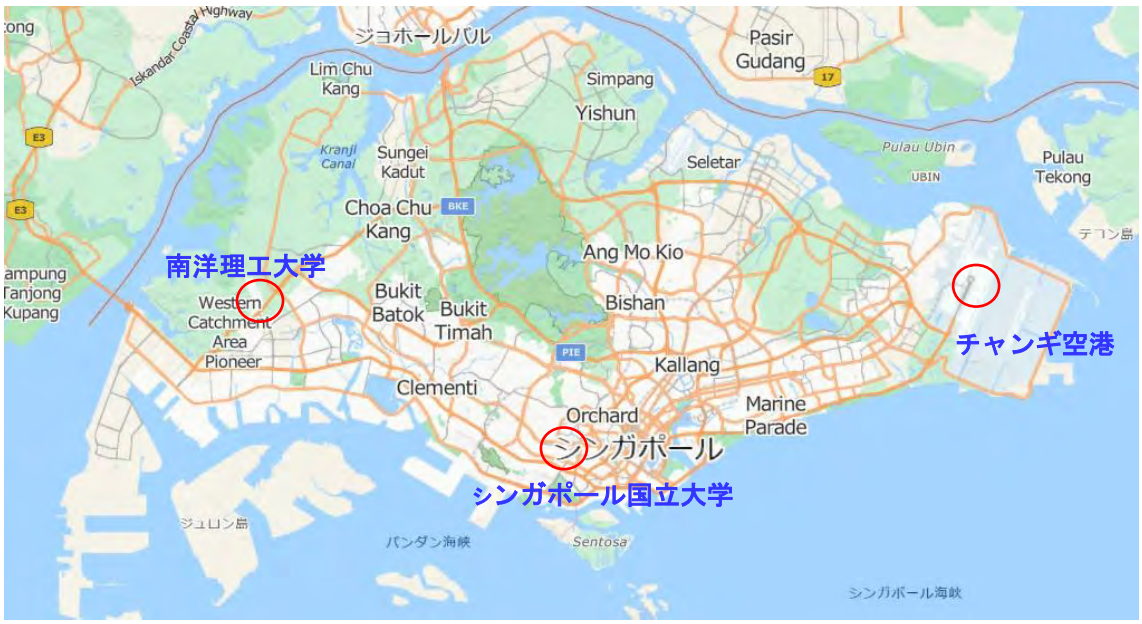
竹林を出でてシンガポールへ： 電子工学分野国際会議出席

シンガポール国立大学、南洋理工大学訪問

群馬大学 名誉教授 小林春夫

(1) はじめに

シンガポールには何かあるのではないか、ぜひ訪問したいと常々思っていた。
20 年ぶり 2 回目のシンガポール訪問である。
シンガポール - Wikipedia



(2) 電子工学分野国際会議 参加

12th International Conference on Communications, Circuits and Systems (ICCCAS)

2023 年 5 月 5 日（金）-7 日（日） 於 シンガポール 12th ICCCAS | Singapore

● Technical Program Committee Co-Chair および Track 1 Chair として招聘される

会議全体での発表論文件数は下記

キーノート 3 件

招待講演 38 件

一般論文： 12 か国から 120 件投稿、そのうち 67 採択 （採択率 約 50%）

Best Student Paper Competition 学生のコンペテション 9 件

合計 117 件の発表 （このうち 65 件のオンサイトの発表）

昨年度も招待講演者として参加

https://kobaweb.ei.st.gunma-u.ac.jp/news/pdf/2022/20220519am12.pdf

2024 年は中国（成都市または厦門市）での開催を検討するとのこと

● Track 1　をオーガナイズする。12 名を招待講演者として招聘する。
日本勢の存在感を増すことを意図する。「戦力の集中」「ランチェスターの法則」

<u>オンライン出席</u>

1. 萩原良昭先生（崇城大学、元ソニー、元群馬大学客員教授）
2. 橋本研也先生（中国 電子科技大学 教授、千葉大学 名誉教授）
3. 青木均先生（ローム、元群馬大学客員教授）
4. 傘 昊 先生（東京都市大　教授）
5. 菊池信彦先生（日立製作所）　　光野正志様からのご紹介
6. 原史朗先生（産総研）
7. 小関国夫先生（産総研、元群馬大学客員教授）
8. 伊藤直史先生（群馬大学　准教授）

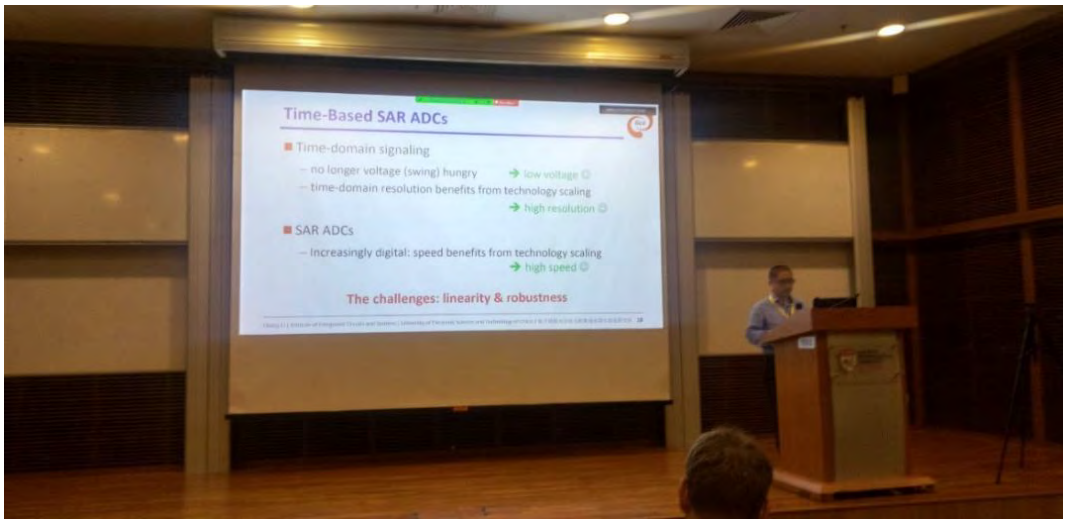
<u>オンサイト出席</u>

9. 崔通先生（東京工芸大学　准教授、元群馬大学非常勤講師）
10. 千葉明人先生（群馬大学　准教授）
11. 元澤篤史先生（ルネサスエレクトロニクス、元群馬大学非常勤講師）
12. 小林春夫（群馬大学　名誉教授）

● 学会の会場の様子

会場でのグループ写真

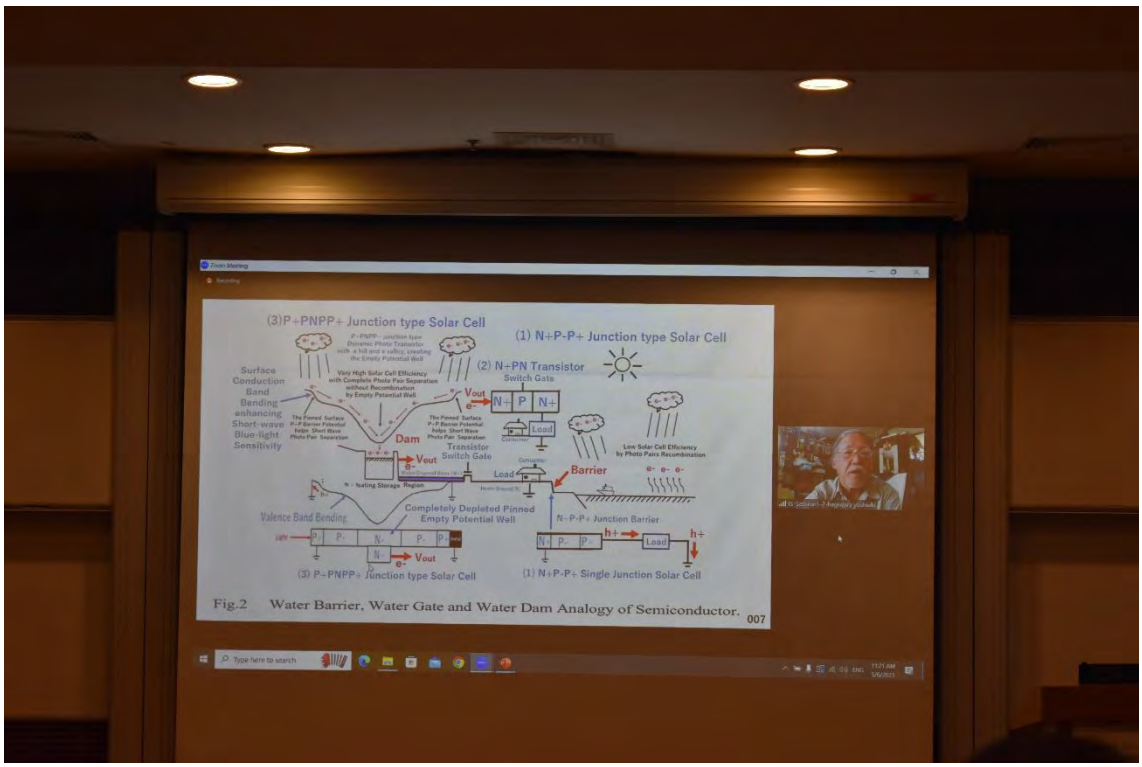
Prof. Maode Ma (Qatar University, Qatar) の司会



Prof. Qiang Li (U. of Electronic Science and Technology of China)のキーノートトーク

Prof. Massimo Alioto (National University of Singapore)のキーノートトーク

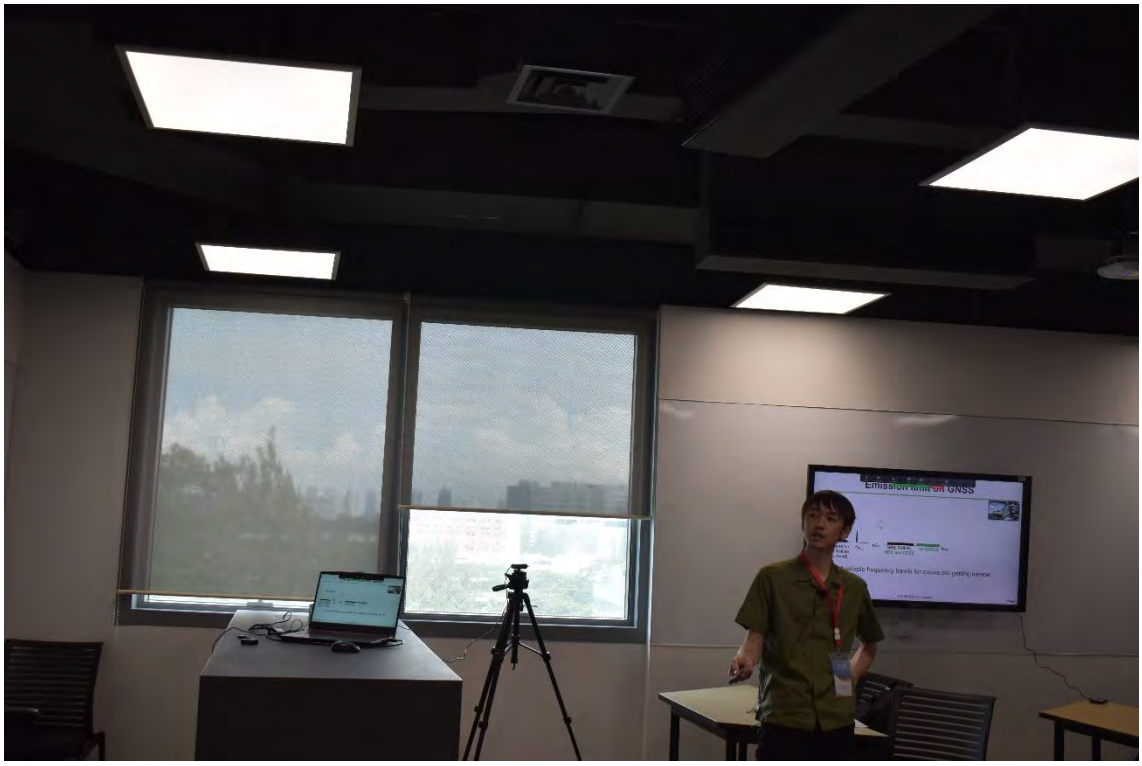
Prof. Franco Maloberti (University of Pavia, Italy)のオンライン・キーノートトーク



萩原良昭先生のオンライン招待講演

橋本研也先生のオンライン招待講演

千葉明人先生の招待講演



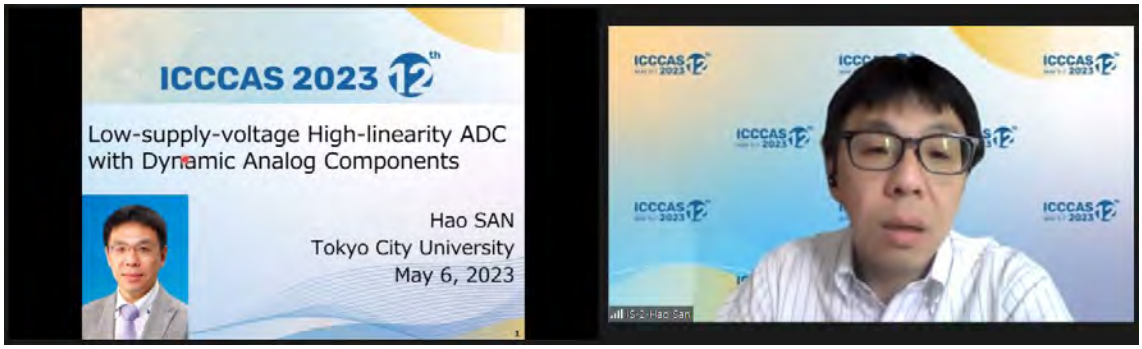
元澤篤史先生の招待講演

崔通先生の招待講演

筆者の発表

発表会場にて

学会での懇親会にて　　上　元澤先生、千葉先生；　下　崔先生　小林



傘昊先生のオンライン招待講演

青木均先生のオンライン招待講演

伊藤直史先生のオンライン招待講演

菊池信彦先生のオンライン招待講演

原史朗先生のオンライン招待講

(3) シンガポール国立大学訪問

National University of Singapore　(NUS)

シンガポール国立大学 - Wikipedia

Massio Alioto 先生の研究室を訪問。同グループは日本ではほとんど知られていないが
ISSCC2022 で Best Paper Award, ISSCC2023 でも発表等　ISSCC、JSSC の常連である。
VLSI Circuit Symposium 2023 (京都) でも論文が 6 件採択されている。

Alioto 先生 Gr は年間 20 チップのテープアウトをしているとのこと。30 名の研究者
（博士課程学生、10 名がポストドクター、大学が雇用した研究者がそれぞれ 3 分の１）
を抱えている。RF, デジタル, アナログ等それぞれ得意な研究者から構成されている。

ポストドクに慶応大学を卒業された日本人の方がおられる。
日本人は同研究室には一人、　日本からの訪問もほとんどないとのこと。

萩原良昭先生は Alioto 先生とかつて国際学会運営等で一緒に仕事をされたとのことである。

同先生グループは Green IC プロジェクト　デジタル、アナログ、システムの総合的観点
から低消費電力を実現するプロジェクトを遂行している。回路設計技術に加え AI, Security
等　多彩な技術を取り入れたバランスがとれた研究であるという印象である。

産学連携を志向している：　Soitec,　NXP のサポートプロジェクト等を行っている。
世界の主要な半導体メーカーの拠点がシンガポールにある (約 30 社)。
Foundry: TSMC, UMC, Global Foundry 等
Design Center: STM, Huawei, 等　日本からは Panasonic　等

産学連携は「大学が産業界から予算や情報を少し入れてもらう」というよりシンガポール
の国自体が「大学と産業界が強く連携することが国の発展・富を豊かにすることにつながる」
という価値観・戦略を持っていると感じる。

なお、現在の半導体分野での米国と中国とのデカプリングに対して
シンガポールは両方とも友好関係を保ち交流しているようである。

シンガポールは金融関係が発展していることが知られているが、電子産業分野に対して
でも世界各国から投資が大きいようである。

Prof. Massimo Alioto
Chair of the Distinguished Lecturer Program for the IEEE CAS Society, Fellow of IEEE

National University of Singapore, Singapore

Biography: Massimo Alioto is a Professor at the ECE Department of the National University of Singapore, where he leads the Green IC group, the Integrated Circuits and Embedded Systems area, and the FD-fAbrICS center on intelligent & connected systems. Previously, he held positions at the University of Siena, Intel Labs – CRL (2013), University of Michigan - Ann Arbor (2011-2012), University of California – Berkeley (2009-2011), EPFL - Lausanne.

He is (co)author of 350+ publications on journals and conference proceedings, and four books with Springer (with two more coming this quarter). His primary research interests include ultra-low power and self-powered systems, green computing, circuits for machine intelligence, hardware security, and emerging technologies.

He was the Editor in Chief of the IEEE Transactions on VLSI Systems and Deputy Editor in Chief of the IEEE Journal on Emerging and Selected Topics in Circuits and Systems. He is currently the Chair of the Distinguished Lecturer Program for the IEEE CAS Society, and was a Distinguished Lecturer for the SSC and CAS Society. Previously, Prof. Alioto was the Chair of the "VLSI Systems and Applications" Technical Committee of the IEEE Circuits and Systems Society (2010-2012). He served as Guest Editor of numerous journal special issues (JSSC, TCAS-I, JETCAS...), Technical Program Chair of several IEEE conferences (ISCAS, SOCC, PRIME, ICECS), and TPC member (ISSCC, ASSCC). His research group contribution has been recognized through various best paper awards (e.g., ISSCC, ICECS), and in the ten technological highlights of the TSMC 2020 annual report, among the others. Prof. Alioto is an IEEE Fellow.

Prof. Massimo Alioto (green-ic.org)

Prof. Massimo Alioto の ICCCAS2023 でのキーノートトーク

● シンガポール国立大学キャンパス

広大で学内キャンパスにサークルバスが走っている。工学部は充実している印象


SAE
29
NUS
National University
of Singapore


NUS ENGINEERING

● シンガポール国立大学の近くのシンガポール日本人小学校

(4) 南洋理工大学訪問

南洋理工大学 - Wikipedia

Prof. Chan Pak Kwong にコンタクトをとり、南洋理工大学の Centre for Integrated Circuits and Systems (CICS) を案内してもらった。

Centre for Integrated Circuits and Systems | NTU Singapore

Assoc Prof Chan Pak Kwong | Academic Profile | DR-NTU | Research | NTU Singapore

センター長の Prof. Zheng Yuanjin にもご同席いただきご説明いただいた。

Assoc Prof Zheng Yuanjin | Academic Profile | DR-NTU | Research | NTU Singapore

- 1 学年の IC 設計コースの学生は百数十名。世界の半導体メーカーがシンガポールに進出しており、即戦力の卒業生を求めている。
- 学生は中国、インド、韓国からが多い。日本人は少なし。
  教員も中国、インド、韓国からが多い。
- 中国からの学生は半分くらいは自国に戻る。
  IC 設計ではシンガポールより中国のほうが給与がよいからとのこと
  （筆者注： IC 設計ではシンガポールより中国のほうが給与が良いのかと驚いた）
- MediaTek 社の支援により TSMC のチップの相乗りが無料
- NTU では IC 設計とともに IT、ロボテクスが人気
- 高周波チップの測定設備　欧米のトップ大学より良い（世界一であろうとのこと）
- Cascade Microtech の高周波プロービングシステム
  アジレント　160Gs/s リアルタイムオシロ　等を備えている
- IC 設計教育は　ドイツのミュンヘン工科大学と連携　Technical University of Munich
  TUM Asia - Technical University of Munich Asia (tum-asia.edu.sg)
- アナログ集積回路設計テキスト： Gray Meyer, Razavi, Allen, Martin が書いた教科書
- 設計環境 Cadence のシステム
- 学食　中華、韓国、タイ、インド、ハラル　等　国際色豊かな学生向けレストラン
  街中はバス、トラムの公共交通が便利で運賃が非常に安い
  エコ社会の実現

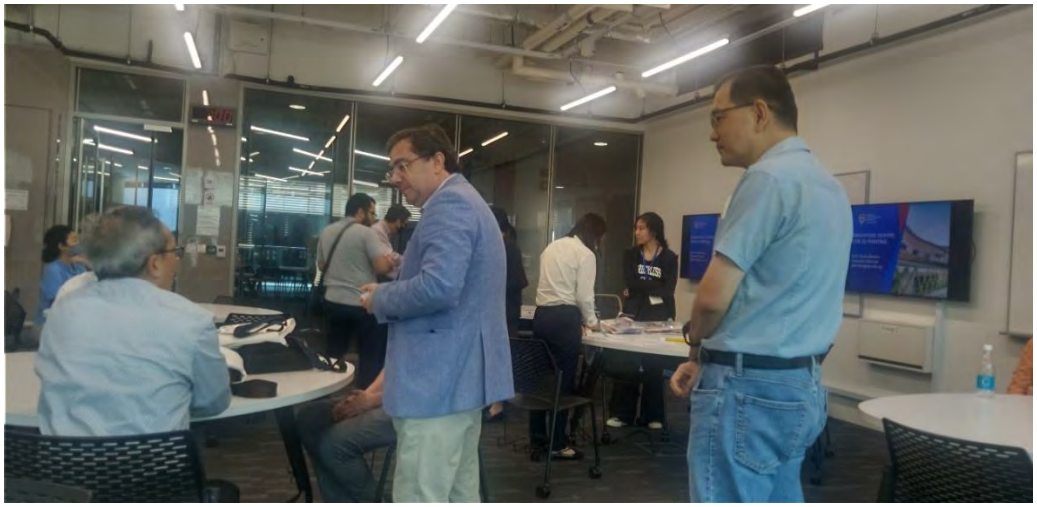
左より　Prof. Chan，小林、崔先生、Prof. Zheng

センターは　「Center」（米語表記）ではなく「Centre」(英語表記)であることに気が付く

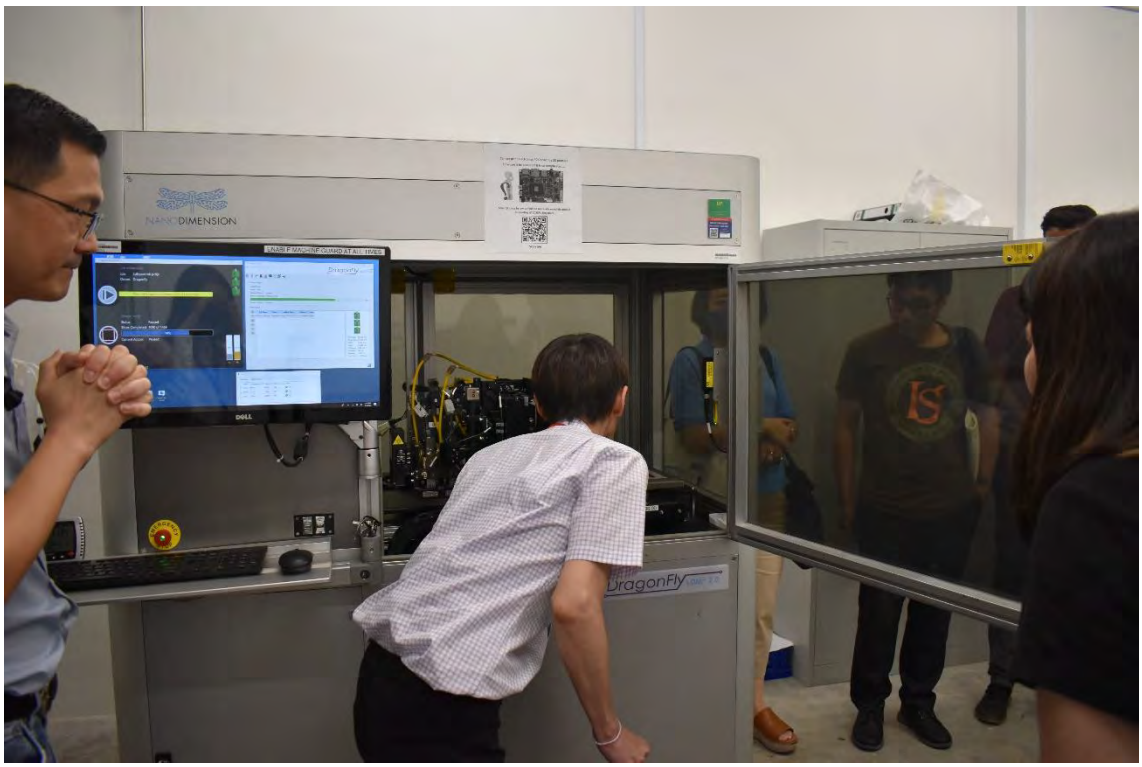
● 南洋理工大学と市内を結ぶバス

● 学会主催の南洋理工大学の 3D Printer プロジェクトの紹介・見学会

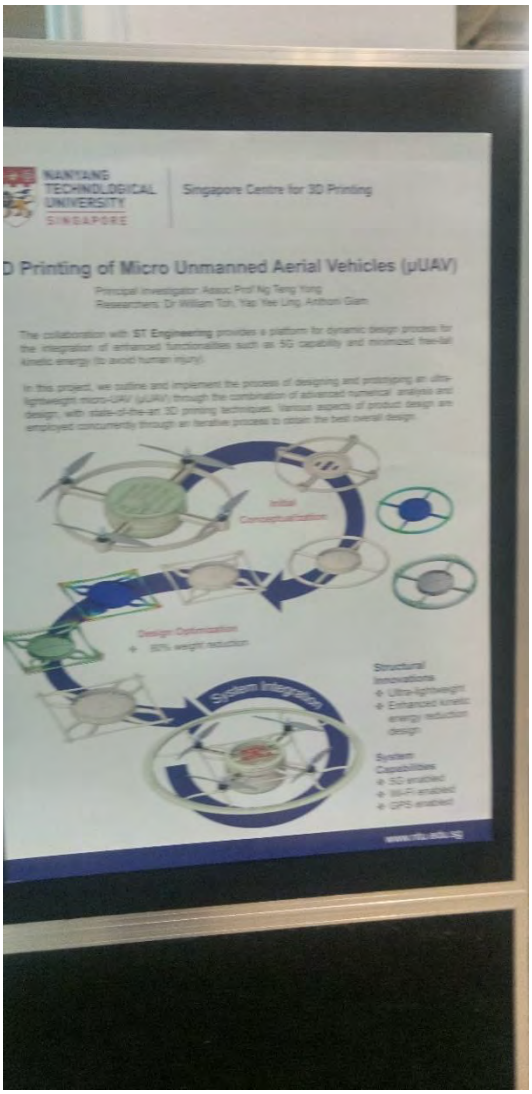
Singapore Centre for 3D Printing (SC3DP) | NTU Singapore

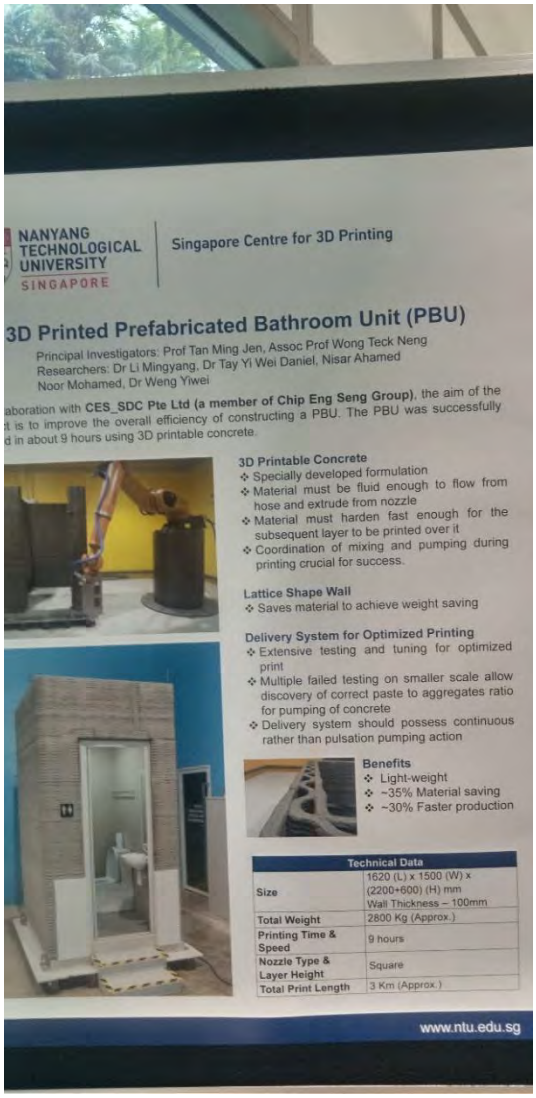


3D Printing Programme Director at NTU, Prof. Paulo Bartolo　による説明


NANODIMENSION
DragonFly


SINGAPORE CENTRE FOR 3D PRINTING


NANYANG TECHNOLOGICAL UNIVERSITY SINGAPORE
Singapore Centre for 3D Printing
D Printing of Micro Unmanned Aerial Vehicles (μUAV)


NANYANG TECHNOLOGICAL UNIVERSITY SINGAPORE
Singapore Centre for 3D Printing
3D Printed Prefabricated Bathroom Unit (PBU)
Principal Investigators: Prof Tan Ming Jen, Assoc Prof Wong Teck Neng
Researchers: Dr Li Mingyang, Dr Tay Yi Wei Daniel, Nisar Ahamed
Noor Mohamed, Dr Weng Yiwei
3D Printable Concrete
Specially developed formulation
Material must be fluid enough to flow from hose and extrude from nozzle
Material must harden fast enough for the subsequent layer to be printed over it
Coordination of mixing and pumping during printing crucial for success.
Lattice Shape Wall
Saves material to achieve weight saving
Delivery System for Optimized Printing
Extensive testing and tuning for optimized print
Multiple failed testing on smaller scale allow discovery of correct paste to aggregates ratio for pumping of concrete
Delivery system should possess continuous rather than pulsation pumping action
Benefits
Light-weight
~35% Material saving
~30% Faster production
Technical Data
Size
1620 (L) x 1500 (W) x (2200+600) (H) mm
Wall Thickness – 100mm
Total Weight
2800 Kg (Approx.)
Printing Time & Speed
9 hours
Nozzle Type & Layer Height
Square
Total Print Length
3 Km (Approx.)
www.ntu.edu.sg

国、産業界からの支援

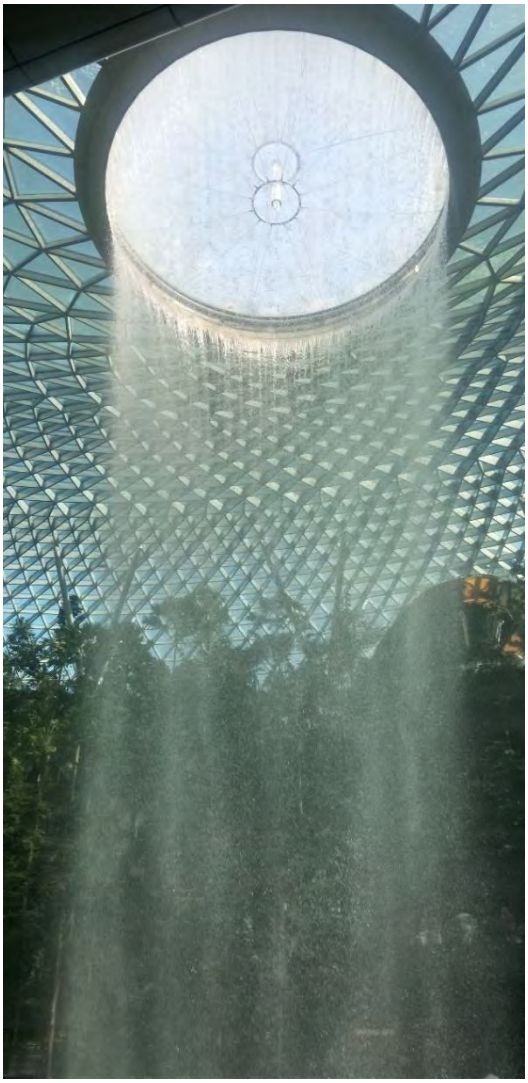
● 南洋理工大学の図書館

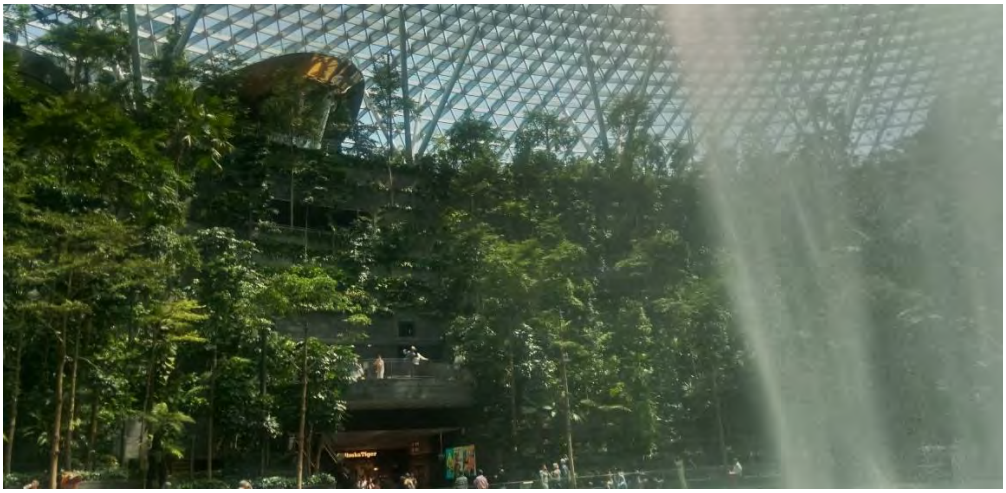
● 産学連携

Alibaba, Delta, Shaeffler 社との連携がうかがい知れた

(5) シンガポール市内観光

● Changi Internaionational Airport （チャンギ国際空港） アジアのハブ空港





● シンガポール市内の印度人街　(Little India)

- 南インドではバナナの葉の上に食事を置く。
  味（香りも？）が滲みだして美味しくなるとのこと（崔先生より）
- 復路の機内で大作のインド映画「RRR」を観る。

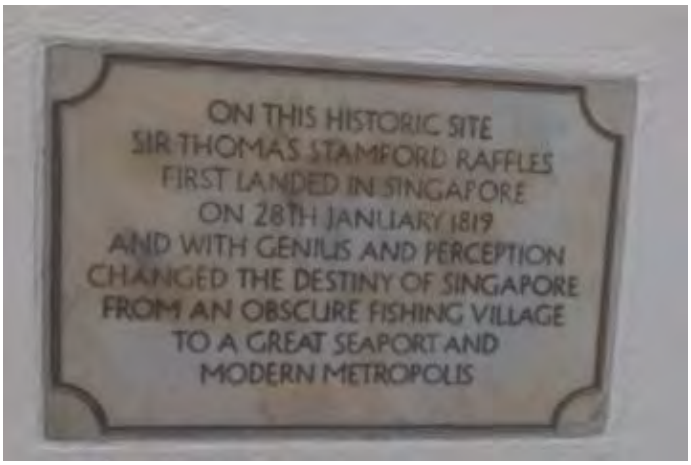
● マーライオン 他


THE MERLION DARUMA
$90
SUPERMAMA


Esplanade Dr
Nicoll Highway

● イギリス人で最初にシンガポールに上陸したトーマス・ラッフルズの像

Stamford Raffles - Wikipedia




SEMANGAT
YANG BARU


THE ARTS HOUSE AT THE OLD PARLIAMENT
THE ANATOMY
OF PERFORMANCE
EXPLORE THE SPECTRUM
OF HUMAN EXPERIENCE
AT SINGAPORE'S
PINNACLE ARTS FESTIVAL
TICKETS FROM $25
19 MAY
–
4 JUNE
Angel Island
Realm of Silk
Humans 2.0
Pompeii
Abyss
BLKDOG
FOR FULL FESTIVAL LINE-UP & TO BOOK TICKETS, VISIT SIFA.SG
#SIFA2023


ASIAN CIVILISATIONS MUSEUM


LOUIS VUITTON

崔先生の「シンガポールは常に新しい建物を作っている」との言葉が印象的である。

● シンガポールマネージメント大学の建物

Home | Singapore Management University (SMU)

(6) 最後に

世界大学ランキングでは　シンガポール国立大学、南洋理工大学ともアジアでトップを競っているが、ランキングをあげることでブランドを確立しようとする強い方針・戦略を感じる。産学連携を行いながらも、「世界のトップジャーナルへの論文発表」ということを強く意識している。短期間に世界上位になっており、そのやり方を学ぶ必要があろう。

QS世界大学ランキング2022年版：アジアの上位10校

2022	2021	大学名	国
11位	11位	シンガポール国立大学	シンガポール
12位	13位	南洋理工大学	シンガポール
17位	15位	清華大学	中国
18位	23位	北京大学	中国
22位	22位	香港大学	香港
23位	24位	東京大学	日本
31位	34位	復旦大学	中国
33位	38位	京都大学	日本
34位	27位	香港科技大学	香港
36位	37位	ソウル大学校	韓国

https://www.topuniversities.com/

今回の出張の前に「中国が半導体のオリンピック ISSCC2023 での発表件数が世界一になった理由」のご意見を ISSCC2008 TPC Chair を務められた萩原良昭先生にうかがった。
CenterNews07-1.QX (gunma-u.ac.jp)

「中国はこの分野の技術者の待遇が良いので優秀な人が集まってくるのではないか」とのことであった。以前に国立台湾大学を訪問したときに、同大学では「電気電子工学分野が圧倒的に人気がある、この分野の技術者の収入がよいからである」とその教授が話していた。今回の国際会議に参加し、またシンガポール国立大学、南洋理工大学を訪問して聞いた話からも同様なことを推測できる。

シンガポール、中国、韓国、台湾等では（優秀な）電子技術者・マネージャは他の業種に比べて場合によっては数倍の収入があるのかもしれない。この分野は職業的・経済的に非常に魅力がある、優秀な人が集まってくる、ますますその業界・企業が発展する、大学のその分野が強化される、国も支援するというポジテブフィードバックがかかっている、社会で正のスパイラルに入っていることがうかがい知れる。

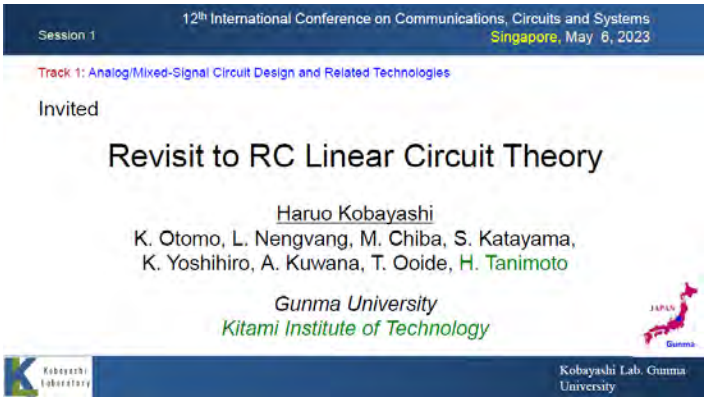
「激水の疾くして石を漂わすに至るは 勢なり」　孫子

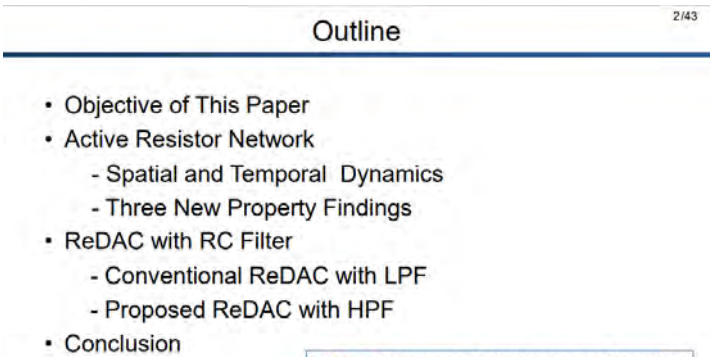
日本社会はこのことを認識すべであると思う。

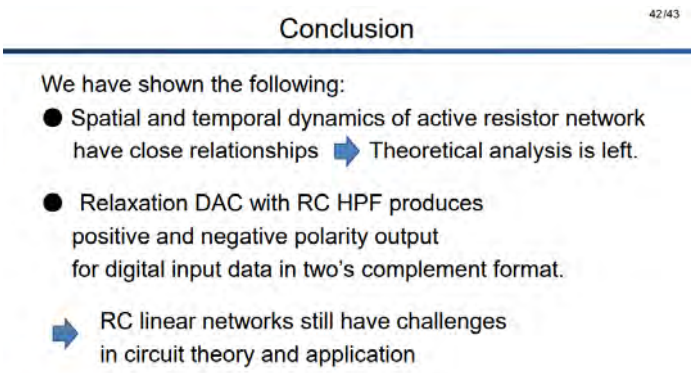
「彼を知り己を知れば　百戦殆あやうからず。彼を知らずして己を知れば
一勝一負す。彼を知らず己を知らざれば 戦うごとに必ず殆し。」　孫子

(7) 付録

1. 筆者の発表スライドの表紙、目次、結論







2. 出席国際学会の関係プログラムで筆者に関係した部分等を抽出したものを次頁以降に添付する。

ICCCAS 2023

2023 The 12th International Conference on

Communications, Circuits, and Systems

Singapore | May 5-7, 2023 | GMT+8

Conference Committees

Conference Committee Chairs

Franco Maloberti, FIEE, University of Pavia, Italy
Massimo Alioto, FIEEE, National University of Singapore, Singapore

Conference Committee Co-Chair

Maode Ma, FIET, Qatar University, Qatar

Program Committee Chairs

Lin Wang, SMIEEE, Xiamen University, China
Haruo Kobayashi, SMIEEE, Gunma University, Japan

Program Committee Co-Chairs

Yang Yue, SMIEEE, Xi'an Jiaotong University, China
Jeff Kilby, Auckland University of Technology, New Zealand
Kanglian Zhao, Nanjing University, China

Award Chairs

Char-Dir Chung, FIEEE, National Taiwan University, Taiwan
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Session 1
Analog/Mixed-Signal Circuit Design and Related Technologies

Session Chair: Prof. Haruo Kobayashi, Gunma University, Japan

Time: 10:40-12:00, May 6, 2023	**Onsite Room: AUD302**
Meeting ID: 839 7342 5289	**Link: https://us02web.zoom.us/j/83973425289**
10:40-11:00	**Invited Speech (Online)**
	Radio Frequency Acoustic Wave Devices in RF Front-End in Mobile Communications --- Why Unavoidable? **Prof. Ken-ya Hashimoto** University of Electronic Science and Technology of China
11:00-11:20	**Invited Speech (Online)**
	Artificial Intelligent Partner System (AIPS) with Pinned Photodiode Used for Robot Vision and Solar Panel **Prof. Yoshiaki Daimon Hagiwara** Sojo University, Japan
11:20-11:40	**Invited Speech (Onsite)**
	Revisit to RC Linear Circuit Theory **Prof. Haruo Kobayashi** Gunma University, Japan
11:40-12:00	**Invited Speech (Onsite)**
	Power Conversion Circuits for Distributed PV Systems **Assoc. Prof. Toru Sai** Tokyo Polytechnic University, Japan

Session 2
Analog/Mixed-Signal Circuit Design and Related Technologies

Session Chair: Prof. Haruo Kobayashi, Gunma University, Japan

Time: 14:00-15:40, May 6, 2023 **Onsite Room: SR903**

Meeting ID: 839 7342 5289 **Link: https://us02web.zoom.us/j/83973425289**

14:00-14:20	**Invited Speech (Onsite)**
	RF Parameter Estimation Using Lightwave Modulation **Assoc. Prof. Akito Chiba** Gunma University, Japan
14:20-14:40	**Invited Speech (Onsite)**
	An Attachable Fractional Divider Transforming an Integer-N PLL Into a Fractional-N PLL with SSC Capability **Mr. Atsushi Motozawa** Renesas Electronics Corp., Japan
14:40-15:00	**Invited Speech (Online)**
	Low-supply-voltage High-linearity ADC with Dynamic Analog Components **Prof. Hao San** Tokyo City University, Japan
15:00-15:20	**Invited Speech (Online)**
	A Unified Model of MIS and Ridge HEMTs for Fast and High-Power Switching Applications **Dr. Hitoshi Aoki** Rohm Semiconductor, Japan
15:20-15:40	**Invited Speech (Online)**
	Recent Progress in High-Voltage SiC Devices and its Application Development **Dr. Kunio Koseki** National Institute of Advanced Industrial Science and Technology, Japan

Session 7
Analog/Mixed-Signal Circuit Design and Related Technologies

Session Chair: Prof. Haruo Kobayashi, Gunma University, Japan

Time: 10:00-11:15, May 7, 2023	**Onsite Room: SR902**
Meeting ID: 832 5613 7923	**Link: https://us02web.zoom.us/j/83256137923**

10:00-10:15	**CS23-210**
	A 0.4V 21.6nW Duty Cycle Generator Based on Compact Pulsed Modulator for MEMs Sensing Interface **Presenter: Xi Sung Loo** Xi Sung Loo, Wang Ling Goh and Yuan Gao Nanyang Technological University, Singapore
10:15-10:30	**CS23-232**
	Single OTRA Based Universal Third Order Butterworth Filter and Its Performance Study **Presenter: Mourina Ghosh** Subhasish Banerjee, Mourina Ghosh and Pulak Mondal Indian Institute of Information Technology, India
10:30-10:45	**CS23-255**
	Design of High Quality Factor Fully Differential CMOS Active Inductor With Cascode Current Mirror for 2-5 GHz Frequency Ranges **Presenter: Sohiful Anuar Zainol Murad** Hussein Anes Abdulqader Aishaikh Ali, Sohiful Anuar Zainol Murad, Faizah Abu Bakar, Ahmad Fariz Hasan and Jamilah Karim Universiti Malaysia Perlis, Malaysia
10:45-11:00	**CS23-1347**
	Low Power-Delay-Product Ternary Adder with Optimized Ternary Cycling Gates **Presenter: Zhiwei Zeng** Zhiwei Zeng, Guangchao Zhao, Xingli Wang, Beng Kang Tay and Mingqiang Huang Chinese Academy of Sciences, China
11:00-11:15	**CS23-1386**
	Design Step for Op Amp based CMOS Feedback Amplifiers **Presenter: Suriya Adirek** Suriya Adirek, Chaiyan Chanapromma and Jirayuth Mahattanakul Nakhon Sawan Rajabhat University, Thailand

Session 9
Analog/Mixed-Signal Circuit Design and Related Technologies

Session Chair: Prof. Haruo Kobayashi, Gunma University, Japan

Time: 13:00-14:00, May 7, 2023	**Onsite Room: SR902**
Meeting ID: 832 5613 7923	**Link: https://us02web.zoom.us/j/83256137923**
13:00-13:20	**Invited Speech (Online)**
	Principle and Application of Electrical Impedance Tomography **Assoc. Prof. Tadashi Itoh** Gunma University, Japan
13:20-13:40	**Invited Speech (Online)**
	Ultra-low Power Multi-Point Remote Sensing Technology Using Opticlal Fiber Power Supply for Sewage Systems **Dr. Nobuhiko Kikuchi** R&D Group, Hitachi Ltd., Japan
13:40-14:00	**Invited Speech (Online)**
	Minimal Fab Using Half-inch Wafers for Low-volume Device Markets **Dr. Shiro Hara** National Institute of Advanced Industrial Science and Technology, Japan

Conference Chair

Prof. Maode Ma

Qatar University, Qatar

Time:	9:05-9:10, May 6, 2023	**Onsite Room:**	AUD302
Zoom ID:	839 7342 5289	**Zoom Link:**	https://us02web.zoom.us/j/83973425289

Bio: Prof. Maode Ma, a Fellow of *IET*, received his Ph.D. degree from Department of Computer Science in Hong Kong University of Science and Technology in 1999. Now, Dr. Ma is a Research Professor in the College of Engineering at Qatar University in Qatar. Before join Qatar University, he has been a faculty member at Nanyang Technological University in Singapore for over 20 years. He has extensive research interests including network security and wireless networking. He has led 25 research projects funded by government, industry, military and universities in various countries. He has supervised over 20 research students to get their Ph. D degree. He has been a conference chair, technical symposium chair, tutorial chair, publication chair, publicity chair and session chair for over 100 international conferences. He has been a member of the technical program committees for more than 200 international conferences. Dr. Ma has about 450 international academic publications including more than 220 journal papers and over 230 conference papers. He has edited a few technical books and produced over 25 book chapters. His publication has received over 6700 citations in Google Scholar. He has delivered over 80 keynote speeches and 10 tutorials at various international conferences. He currently serves as the Editor-in-Chief of *International Journal of Computer and Communication Engineering* and *Journal of Communications.* He also serves as a Senior Editor for *IEEE Communications Surveys and Tutorials*, and an Associate Editor for International Journal of *Wireless Communications and Mobile Computing* and *International Journal of Communication Systems.* Dr. Ma is a senior member of *IEEE Communication Society* and a member of *ACM.* He is now the Education Chair of the *IEEE* Singapore Section and the Chair of the *ACM*, Singapore Chapter.

Award Chair

Prof. Char-Dir Chung

National Taiwan University, Taiwan

Time:	18:30, May 6, 2023	**Onsite Room:**	CALI Park Avenue Rochester
Zoom ID:	N/A	**Zoom Link:**	N/A

Bio: Char-Dir Chung received the B.S. degree in electrical engineering from the National Taiwan University (NTU), Taipei, in 1983, and the M.S. and Ph.D. degrees in electrical engineering from the University of Southern California, Los Angeles, in 1986 and 1989, respectively.

From 1989 to 1992, Dr. Chung was with the LinCom Corporation, Los Angeles, where he worked on analytical and simulation modeling of scientific and military satellite communication systems. From 1992 to 2005, he joined the faculty of the National Central University (NCU) in Taiwan. At NCU, he founded the Advanced Communication Laboratory in 1998, the Graduate Institute of Communication Engineering in 2000 and the Communication Engineering Department in 2003, and was the founding heads of these organizations. Since 2005, he has been on the faculty of the National Taiwan University, where he is now a Distinguished Professor of the Electrical Engineering Department and the Graduate Institute of Communication Engineering. Prof. Chung was endowed with the SiS Technology Chair for the 2009 academic year at NTU. His current research interests include digital modulation theory, wireless communications, spread spectrum communications and statistical signal processing. He has published more than 80 journal and conference papers and holds 6 patent rights in these areas.

Dr. Chung received the Group Achievement Award from the National Aeronautics and Space Administration, USA, in 1991; the Young Scientists Award from the International Union of Radio Science in 1993; the annual Research Award from the National Science Council, ROC, in 1992 and from 1994 to 2001, the Kentucky Colonel grade from the Commonwealth of Kentucky, USA, in 2003, and the FORMOSAT-2 Satellite Project Award from the National Space Center, ROC, in 2005. In 2005, Dr. Chung was ranked as the first-grade project investigator by the National Science Council, ROC. He served as the Chairman of IEEE Information Theory Society, Taipei Chapter, from 1997 to 1999, and the Secretary of Taipei Section from 2007 to 2008. He was an editor for the Journal of the Chinese Institute of Electrical Engineering from 2000 to 2004 and an editor for the Magazine of the same organization from 2003 to 2008. He was a guest co-editor for the IEEE Transactions on Vehicular Technology (Special Issue on Intelligent Transportation Systems and Telematics Applications) in 2008. Dr. Chung is a Fellow of the IEEE.

Dr. Chung has been very active in industrial development and government services in Taiwan. From 2004 to 2008, he served as the Chairman of the Wireless System Group of the National Science and Technology Program for Telecommunications, and the founding Chairman of the Taiwan Broadband Wireless Communications Industry Alliance. Since 2001, Dr. Chung joined several Technology Review Boards of the Ministry of Economic Affairs, and acted as the Chairman of the Board of Computer, Consumer Electronics, Communications, Optoelectronics, and Semiconductor Electronics from 2005 to 2008 and the Board of the Technologies and Applications from 2012 to 2013. Dr. Chung acted as Deputy Executive Secretary of the Science and Technology Advisory Group and of the National Information and Communication Security Taskforce during 2008-2011, Executive Secretary of the Digital Convergence Taskforce during 2011-2012 and of the National Information and Communication Initiative Committee during 2014-2016, Member and Executive Secretary of the Board of Science and Technology during 2014-2016, and Minister without Portfolio

in 2016, all under the Executive Yuan (the Cabinet), and was involved in cross-ministry national policy making and coordination in a variety of science and technology areas including information and communications, digital content, digital convergence, electronics, technological innovation, biotechnology, agrobiology, talent cultivation, etc. Dr. Chung was awarded Merit Medal by Executive Yuan in 2016 to honor his contribution in reviewing national programs and making national policies in science and technology.

Speaker Introduction

Prof. Massimo Alioto

National University of Singapore, Singapore

Time:	9:10-9:40, May 6, 2023	**Onsite Room:**	AUD302
Zoom ID:	839 7342 5289	**Zoom Link:**	https://us02web.zoom.us/j/83973425289

Aggressive Design Reuse for Ubiquitous and Hardware-Patchable Secure Chips – From Physical Design to On-Chip Machine Learning

Abstract: Divide-and-conquer design methodologies facilitate building block design, but conflict with basic security requirements, while also precluding opportunities for efficient system integration and inexpensive embedment of security features. At the same time, the insertion of security primitives as standalone blocks is inherently additive in terms of area, power, design effort and integration effort, limiting their embeddability in low-cost devices (i.e., the vast majority of the upcoming trillion chips for the Internet of Things). As further limitation of conventional approaches to security enforcement in silicon chips (e.g., against side-channel attacks), the discovery of hardware vulnerabilities cannot be followed by later hardware fixes as we are used to do with software systems.

In this keynote, the road towards ubiquitous hardware security is pursued from a primitive design perspective, designing PUFs and TRNGs that are inherently immersed in existing memory arrays and logic fabrics, and breaking the boundaries of traditional system partitioning. The new concept of hardware patching is also discussed, where circuit flexibility is introduced to make silicon chips able to evolve over time and counteract newly discovered vulnerabilities through learning-based physical protection mechanisms.

Bio: Massimo Alioto is a Professor at the ECE Department of the National University of Singapore, where he leads the Green IC group, the Integrated Circuits and Embedded Systems area, and the FD-fAbrICS center on intelligent&connected systems. Previously, he held positions at the University of Siena, Intel Labs – CRL (2013), University of Michigan - Ann Arbor (2011-2012), University of California – Berkeley (2009-2011), EPFL - Lausanne.

He is (co)author of 300+ publications on journals and conference proceedings, and four books with Springer. His primary research interests include ultra-low power and self-powered systems, green computing, circuits for machine intelligence, hardware security, and emerging technologies.

He is the Editor in Chief of the IEEE Transactions on VLSI Systems, Distinguished Lecturer for the IEEE Solid-State Circuits Society, and was Deputy Editor in Chief of the IEEE Journal on Emerging and Selected Topics in Circuits and Systems. Previously, Prof. Alioto was the Chair of the “VLSI Systems and Applications” Technical Committee of the IEEE Circuits and Systems Society (2010-2012), Distinguished Lecturer (2009-2010) and member of the Board of Governors (2015-2020). He served as Guest Editor of numerous journal special issues, Technical Program Chair of several IEEE conferences (ISCAS 2023, SOCC, PRIME, ICECS), and TPC member (ISSCC, ASSCC). Prof. Alioto is an IEEE Fellow.

Prof. Qiang Li

University of Electronic Science and Technology of China, China

Time:	9:40-10:10, May 6, 2023	**Onsite Room:**	AUD302
Zoom ID:	839 7342 5289	**Zoom Link:**	https://us02web.zoom.us/j/83973425289

TBA

Abstract:

Bio: Qiang Li received the B.Eng. in Electrical Engineering from the Huazhong University of Science and Technology (HUST), Wuhan, China and the Ph.D. in Electronic Engineering from the Nanyang Technological University (NTU), Singapore, in 2001 and 2007, respectively. He has been working on analog/RF and mixed-signal circuits in both academia and industry, holding positions of Engineer, Project Leader & Technical Consultant in Singapore. He has been an Associate Professor at the Aarhus University, Denmark during 2011-2014, and the Vice Dean of the School of Microelectronics and Solid-State Electronics, UESTC during 2014-2018. He is currently a full Professor at the University of Electronic Science and Technology of China (UESTC), heading the analog group. His research interests include low-voltage and low-power analog/RF circuits, data converters, and mixed-mode circuits for biomedical and sensor interfaces.

He has founded and is currently heading the UESTC Institute of Integrated Circuits and Systems. In January 2018, The Institute is accredited as an international collaboration platform (111 Project) co-supported by the Chinese Ministry of Education and SAFEA.

Prof. Li serves as the Distinguished Lecturer of the IEEE Solid-State Circuits Society (SSCS), a member of the Technical Program Committee of IEEE Custom Integrated Circuits Conference (CICC), a member of the Technical Program Committee of European Solid-State Circuits Conference (ESSCIRC), and a member of the Technical Program Committee of IEEE Asian Solid-State Circuits Conference (ASSCC). He was a member of the Student Research Preview (SRP) committee of the International Solid-State Circuits Conference (ISSCC) and the TPC Chair of 2018 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS). He served/serves as a Guest Editor of IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I) and an Associate Editor of IEEE Open Journal of Circuits and Systems (OJCAS). He is the Founding Chair of IEEE Chengdu SSCS/CASS Joint Chapter.

Prof. Ken-ya Hashimoto

University of Electronic Science and Technology of China, China

Time:	10:40-11:00, May 6, 2023	**Onsite Room:**	AUD302
Zoom ID:	839 7342 5289	**Zoom Link:**	https://us02web.zoom.us/j/83973425289

Radio Frequency Acoustic Wave Devices in RF Front-End in Mobile Communications --- Why Unavoidable?

Abstract: Several tens of radio frequency devices based on surface and bulk acoustic wave technologies are installed in each smartphone as filters, duplexers, and multiplexers. The number is still growing and expected to be more than one hundred near future. IC industires attemped to realize most of all functionalities on Si. It is also true for high speed communications. Nevertheless, why are acoustic wave devices still used? The biggest obstacle is non-linearity. RF filters must be quite linear to avoid unnecessary signal generation equivalent to noise. Although acoustic wave devices are quite linear, further linearity improvement is strongly requested. This is due to introduction of the inter-band carrier aggregation and recent trend of inreasing the transmit power. Self-mixing of transmit signals may be cancelled in some extent by circuit design and/or digital signal processing. However, they are not usable for mixture including out-coming jummer signals. To replace acoustic wave devices with those based on another technology, they must fullfil varius tough specifications given to current acoustic wave devices in addition to the linearity: low insertion loss in the passband, good out-of-band rejection, narrow transition bandwidth, small passband ripples, temperature stability, power durability, small size, and low price. This paper reviews current status of RF SAW/BAW devices used in high-speed mobile communications. Typical device performances are presented, and discussions are given on why such tough specifications are enforced. Nonlinearity in RF frontend and its impact to high-speed communications are detailed.

Bio: Ken-ya Hashimoto was born in Fukushima, Japan, in March 2, 1956.He received the B.S. and M.S. degrees in electrical engineering from ChibaUniversity, Chiba, Japan, in 1978 and 1980, respectively, and the D.Eng. degreefrom the Tokyo Institute of Technology, Tokyo, Japan, in 1989.He joinedChiba University as a Research Associate in 1980 and retired there as aProfessor Emeritus in 2021. From 2013 to 2015, he was the Director of theCenter for the Frontier Science with Chiba University. Right after retirement,he moved to the University of Electronic Science and Technology of China(UESTC), Chengdu, China, as a Professor. He had Visiting Professor/Researcherpositions in various institutions, such as the Helsinki University ofTechnology, Espoo, Finland, in 1998, the Laboratoire de Physique et Metrologiedes Oscillateurs, CNRS, Besancon, France, in 1998/1999, Johannes KeplerUniversity, Linz, Austria, in 1999 and 2001, the Institute of Acoustics,Chinese Academy of Science, Beijing, China, from 2005 to 2006, UESTC from 2009to 2012, and the Shanghai Jiao Tong University, Shanghai, China, in 2015.He servedas a Guest Coeditor of the IEEE Transactions on Microwave Theory and TechniquesSpecial Issue on Microwave Acoustic Wave Devices for Wireless Communications in2001, and a Publicity Cochair of the 2002, 2015 and 2021 IEEE InternationalUltrasonics Symposia, an International Distinguished Lecturer of the IEEEUltrasonics, Ferroelectrics, and Frequency Control (UFFC) Society from 2005 to2006, an Administrative Committee Member of the IEEE UFFC Society from 2007 to2009 and from 2014 to 2016, a Distinguished Lecturer of the IEEE ElectronDevices Society from 2007 to 2009, and a General Cochair of the 2011 and 2018IEEE International Ultrasonics Symposia.Hereceived IEEE Fellow in 2005 (now IEEE Life Fellow), the Ichimura IndustrialAward from the New Technology Development Foundation for Development of OptimalSubstrate 42-LT for Radio Frequency Surface Acoustic Wave Devices in 2015, TheCommendation for Science and Technology by the Minister of Education, Culture,Sports, Science

and Technology for Research on High Performance Radio FrequencySurface Acoustic Wave Devices in 2018, and the Distinguished Service Award fromthe IEEE UFFC Society in 2019.His current researchinterests include simulation and design of various high-performance surface andbulk acoustic wave devices, acoustic wave sensors and actuators, piezoelectricmaterials, and RF circuit design.

Prof. Yoshiaki Daimon Hagiwara

Sojo University, Japan

Time:	11:00-11:20, May 6, 2023	**Onsite Room:**	AUD302
Zoom ID:	839 7342 5289	**Zoom Link:**	https://us02web.zoom.us/j/83973425289

Artificial Intelligent Partner System (AIPS) with Pinned Photodiode used for Robot Vision and Solar Panel

Abstract: The future of real-time computing will include massive assemblies of parallel processors over mesh-connected wireless networks to execute the vast amounts of computation with vast number of sensors of all types in order to change the way humans and computers interact in order to meet our human needs. This paper explains the details of the artificial intelligent partner system (AIPS) which was originally introduced in 2008 by Sony, using Play Station III Cell Processor and the intelligent image sensor real-time system, using the Sony Original Pinned Photodiode used for future robot vision and solar panels with the excellent short-wave blue light sensitivity and the electronic and global shutter function capabilities for fast action pictures.

Bio: Yoshiaki Daimon Hagiwara graduated California Institute of Technology (Caltech) in Pasadena California USA with BS71 with honor, MS1972 and PhD1975. While working at Sony in Japan during 1975 till 2008, he was engaged in the early developments of image sensor and the digital camera chip set including the ADC, DRAM and high-speed Cache SRAM buffer memory chips and digital processor chips used for the AIBO, PS2 and PS3 cells. He was invited to talk at IEEE sponsored CCD'79, ECS1980, ESSCIRC2001, ESSCIRC2008 and ISSCC2013 conferences for his works at Sony.

In 1992, he also served as a member of JEDEC memory standardization committee and also as the IEC TC47 technical committee chair of the international standard committee (IEC). He also served as the international program chair and an operational committee member in IEEE EDS sponsored ICMTS conferences since 1991 till 2008, IEEE ISSCC conferences for which he served as the ISSCC Asian Committee chair and also as the ISSCC international technical program (ITC) chair in series. He was also a member of the PC and OC since 1991 and now an advisory committee member of IEEE Cool Chips conferences.

In 2008 he founded and worked as the president in the artificial intelligent partner system laboratory (AIPLAB consortium), a nonprofit research organization (NPO) registered by Kanagawa prefecture government in Japan.

Since 1998 till 1999, he served as a visiting professor at Prof. C. A. Mead Lab of the electrical department at Caltech and also at Prof. T.C. McGill Lab of the applied physics department at Caltech. Since 2003 till 2006, he served also as a visiting professor at Prof. H. Kobayashi Lab in the electronic engineering department at Gunma University in Japan.

Since 2009 till 2017, he taught graduate and undergraduate students as a full professor of the information science department at Sojo University in Kumamoto city Japan. Currently he is serving as a specially appointed professor at the president office in Sojo University and also as a member of the educational committee in Society of Semiconductor Industry Specialists (SSIS) in Japan. He is a Caltech Distinguished Alumni and an IEEE Life Fellow.

Prof. Haruo Kobayashi

Gunma University, Japan

Time:	11:20-11:40, May 6, 2023	**Onsite Room:**	AUD302
Zoom ID:	839 7342 5289	**Zoom Link:**	https://us02web.zoom.us/j/83973425289

Revisit to RC Linear Circuit Theory

Abstract: This paper discusses two RC linear circuits. (i) The first one is the spatial and temporal response of spatially shift-variant (non-uniform) networks with positive and negative resistors. Response of general spatially shift-variant networks whose resistor components are different from each other is investigated. This study is motivated by the vision chip in [1] whose network consists of positive and negative resistors with parasitic capacitors; we previously found there that when the negative resistance effect becomes large, the resistor network becomes unstable [2]. We also showed that both spatial and temporal network behaviors have some relationships even for the shift-variant network [3]. In this paper, we have further investigated their relationships and obtained the following conjecture from extensive simulations: "The network is temporally unstable if there is a node where the input current is injected and its node voltage as the spatial impulse response is negative. However even if there is NOT such a node, there are some networks which are temporally unstable". (ii) The second one is a relaxation digital-to-analog converter (ReDAC) configuration with positive and negative polarity output with a simple RC high pass filter (HPF) [4]. Its digital input is provided in two's complement format, to which the proposed ReDAC configuration directly matches. The proposed ReDAC with HPF is an extension of the conventional ReDAC using a simple RC low-pass filter (LPF) which generates an analog output with only positive polarity. We remark that the RC linear circuit theory is considered as a mature research area, but still there are challenging problems.

Bio: Haruo Kobayashi received the B.S. and M.S. degrees in information physics from University of Tokyo in 1980 and 1982 respectively, the M.S. degree in electrical engineering from University of California, Los Angeles (UCLA) in 1989, and the Ph. D. degree in electrical engineering from Waseda University in 1995. He joined Yokogawa Electric Corp. Tokyo, Japan in 1982, and was engaged in research and development related to measuring instruments and mini-supercomputer. In 1997, he joined Gunma University and presently is a Professor in Division of Electronics and Informatics there. His research interests include mixed-signal integrated circuit design & testing, and signal processing algorithms. He has published more than 120 journal papers and 450 international conference papers. Also he has supervised 16 Ph. D. students and 150 M. S. Students. He received the Yokoyama Award in Science and Technology in 2003. He is a Senior Member of IEEE.

Assoc. Prof. Toru Sai

Tokyo Polytechnic University, Japan

Time:	11:40-12:00, May 6, 2023	**Onsite Room:**	AUD302
Zoom ID:	839 7342 5289	**Zoom Link:**	https://us02web.zoom.us/j/83973425289

Power Conversion Circuits for Distributed PV Systems

Abstract: There are two types of distributed Photovoltaic (PV) systems, AC module type and DC module type. In AC module type, the key component is the Step-up DC-DC converter which boosts the output voltage of a PV panel to Grid. In this presentation new High Step-up DC-DC converter is introduced which is based on Quasi-Z-source network. The proposed converter futures low voltage ripple at output voltage, low voltage stress and free from the high side driver. On the other hand, in DC module type the obstacle of it is the partial shadow problem because of the series connection of PV panels. We introduced the new configuration for DC module type based on Buck-only converter with Current Source Inverter (CSI). The proposed configuration provides simple Module Integrated Converter (MIC) and high reliability. To confirm the validity of the proposals the measurement results of both are shown.

Bio: Toru Sai (Member, IEEE) received the B.S., M.E., and the Dr. Eng. degree in electrical engineering from Chuo University, Tokyo, Japan, in 1986, 1988, and 2012, respectively. In 1988, he joined the research and development center of Yokogawa Electric Company, Tokyo, Japan. From 2016 to 2020, he was a Project Research Associate with The University of Tokyo, Tokyo, Japan. Currently, he is an Associate Professor at Tokyo Polytechnic University and a Research Fellow at the Institute of Industrial Science, the University of Tokyo. His current research interests include DC-DC converters, Gate drivers, and A/D converters. He received the Best Paper Award in 2019 IEEE International Future Energy Electronics Conference.

Prof. Franco Maloberti

Univeristy of Pavia, Italy

Time:	13:30-14:00, May 6, 2023	**Onsite Room:**	SR903
Zoom ID:	839 7342 5289	**Zoom Link:**	https://us02web.zoom.us/j/83973425289

The Role of Communications Circuits and Systems in Human Development

Abstract: Scientific knowledge is essential for human development, especially in communication, circuits, and systems. Until a century ago, mechanics was the leading actor as machines relieved physical fatigue. In the recent past electrical disciplines have replaced mechanics as the prevailing factor. Until now, the unrestricted use of energy has supported development, but the economic and social growth of an increasing number of people leads to new energy challenges. They are not only social and political but also engineering.

A second essential aspect concerns "brain fatigue." It must not be alleviated but supported if we do not want to become slaves of the now increasingly "intelligent" machines. Also, the role of communication, circuits, and systems is and will be vital for this aspect.

Bio: Franco Maloberti received the Laurea degree in physics (summa cum laude) from the University of Parma, Parma, Italy, in 1968, and the Dr. Honoris Causa Ph.D. in electronics from the Instituto Nacional de Astrofisica, Optica y Electronica (Inaoe), Puebla, Mexico, in 1996.

He is Emeritus Professor, University of Pavia, Italy and Visiting Chair Professor, University of Macau, China SAR. In 1993, he was a Visiting Professor at The Swiss Federal Institute of Technology (ETH-PEL), Zurich, Switzerland and in 2004 Visiting Professor at EPFL, Lausanne, Switzerland. From 2000 to 2002 he was the TI/J.Kilby Analog Engineering Chair Professor at the Texas A&M University and from 2002 to 2004 the Distinguished Microelectronic Chair Professor at the University of Texas at Dallas.

His professional expertise is in the design, analysis, and characterization of integrated circuits and analog digital applications, mainly in the areas of switched-capacitor circuits, data converters, interfaces for telecommunication, sensor systems, portable power management, and CAD for analog and mixed A/D design. He has written about 600 published papers, seven books and holds 36 patents.

He is Director of the Division I of IEEE. He was President of the IEEE CAS Society, VP Region 8 of IEEE CAS (1995-1997), Associate Editor of IEEE-TCAS-II, President of the IEEE Sensor Council (2002-2003), IEEE CAS BoG member (2003-2005), VP Publications IEEE CAS (2007-2008). He was DL IEEE SSC Society (2009-2010) and DL IEEE CAS Society (2006-2007; 2012-2013). He received the 1999 IEEE CAS Society Meritorious Service Award, the 2000 CAS Society Golden Jubilee Medal, and the IEEE Millenium Medal. He received the 1996 IEE Fleming Premium, the ESSCIRC 2007 Best Paper Award and the IEEJ Workshop 2007 and 2010 Best Paper Award. He received the IEEE CAS Society 2013 Mac Van Valkenburg Award.

Assoc. Prof. Akito Chiba

Gunma University, Japan

Time:	14:00-14:20, May 6, 2023	**Onsite Room:**	SR903
Zoom ID:	839 7342 5289	**Zoom Link:**	https://us02web.zoom.us/j/83973425289

RF Parameter Estimation Using Lightwave Modulation

Abstract: RF signal processing via lightwave and its technique is known as "microwave- and millimeter-wave photonics (MWP)". This approach possesses some advantages such as avoidance from electromagnetic noises, and wide-bandwidth operation originating from the frequency range of lightwave higher than that of an RF signal with the degree of 4-5 orders. Now various functions have been demonstrated by adopting MWP: RF signal generation in high-frequency region, frequency upconversion and ultra-narrowband RF notch filters.

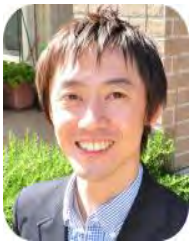
In this invited talk, we introduce an RF signal measurement based on MWP [1]. This scheme utilizes a beat signal between two lightwaves whose phases are independently modulated by a reference RF signal and the RF signal under the test. Into the beat signal, parameters of the RF signal under the test are reflected so that these parameters such as its amplitude and phase can be estimated. Since the frequency of the beat signal becomes into kHz-order one, broadband frequency response is not required in the electronic circuit for the RF parameter estimation.

First, we investigated the case where the frequency of the reference RF signal is the same as that of the RF signal under the test, and found that the beat signal has been expressed using these parameters. Based on the expression derived from model analysis, RF parameter estimation was conducted from the experimentally-obtained beat signal. The phases of the 10-GHz RF signal has been successfully obtained from the beat signal acquired by the experiment via offline processing. For the parameter estimation a prototype has been also designed and implemented as an electronic circuit.

We also extended this scheme by adopting higher-order optical sidebands due to modulation by a reference RF signal, in order to decrease reference RF signal frequency required for RF parameter estimation [2]. This extended approach will be presented from the view of both model analysis and experimental verification.

Bio: Akito Chiba received his B.E. degree in electric and precision engineering, and his M.E. and Ph.D. degrees in the field of electronics and information engineering from Hokkaido University, Sapporo, Japan, in 2000, 2002, and 2005, respectively. From 2005-2010, he worked with the Lightwave Devices Project of the New-Generation Network Research Center, National Institute of Information and Communications Technology (NICT), Koganei, Tokyo, Japan, where he engaged with Lithium Niobate electrooptic devices and their applications to optical communication. From 2010-2011, he joined the Faculty of Engineering, Shizuoka University, Hamamatsu, Shizuoka, Japan, where he served as a Postdoctoral Fellow for CREST Project of Japan Science and Technology Agency, and he was involved in the development of a cathodoluminescent thin film for electron-beam-assisted high-resolution optical imaging. From 2011 he has been with Gunma University, Kiryu, Gunma, Japan, and now he serves as an associate professor in the Division of Electronics and Informatics, Faculty of Science and Technology of the University. In 2018 he was also a visiting scholar at the Department of Electrical and Computer Engineering, Henry Samueli School of Engineering and Applied Science, University of California, Los Angeles. His current research interests include the field of applied optics, fiber optics, and RF photonics, utilizing modulation and demodulations for optical communication, measurement, and RF signal processing. Dr. Chiba is a member of Optica (formerly the Optical Society (OSA)),

IEEE Photonics Society (IEEE-PS), the Japan Society of Applied Physics (JSAP), the optical society of Japan (OSJ), and the Institute of Electronics, Information, and Communication Engineering of Japan (IEICE).



Mr. Atsushi Motozawa

Renesas Electronics Corp., Japan

Time:	14:20-14:40, May 6, 2023	**Onsite Room:**	SR903
Zoom ID:	839 7342 5289	**Zoom Link:**	https://us02web.zoom.us/j/83973425289

An Attachable Fractional Divider Transforming an Integer-N PLL Into a Fractional-N PLL with SSC Capability

Abstract: PLLs are utilized in SoCs for automotive industry. In the industry, the system handles with satellite signals which are weak radio waves coming from space. Therefore, the output frequency of PLLs is carefully designed to avoid EMI. Recently, Global Navigation Satellite System (GNSS) is becoming more common and available frequency bands for clocks are getting narrow. That leads, in many products, replacement integer-N PLLs with fractional-N PLLs is needed to obtain smaller output frequency steps than reference frequency. The attachable fractional divider introduced in this talk transforms an integer-N PLL into a fractional-N PLL with only 0.35 psrms of integrated RMS jitter degradation.

Bio: Atsushi Motozawa received B.S. and M.S. degrees in electrical engineering from Gunma University, Gunma, Japan, in 2006 and 2008, respectively. He joined Renesas Technology Corp., Takasaki, Japan, in 2008, where he was engaged in development of an RX analog front end for NFC LSIs. From 2010 to 2014, he was with Renesas Electronics Corp., Kawasaki, Japan, where he was engaged in designing sensors and a low power BGR for industrial ICs, and PLLs for automotive ICs. From 2014, he was with Renesas System Design, Co., Ltd. Since 2017, he has been with Renesas Electronics Corp., Kodaira, Japan. He is engaged in designing PLLs for SoCs.

Prof. Hao San

Tokyo City University, Japan

Time:	14:40-15:00, May 6, 2023	**Onsite Room:**	SR903
Zoom ID:	839 7342 5289	**Zoom Link:**	https://us02web.zoom.us/j/83973425289

Low-supply-voltage High-linearity ADC with Dynamic Analog Components

Abstract: This paper presents high-linearity analog-to-digital converter (ADC) techniques with dynamic analog components at supply voltages below 1V. To reduce the complexity of the circuit configuration and minimize the active area of multi-bit ADC for high-resolution, the cyclic ADC consist of a simple analog conversion stage and backend logic circuits is applied. The 1bit/step conversion method is utilized, where each conversion step employs the same conversion stage circuit for analog signal processing, resulting in minimal parameter variation between steps. A non-binary method is also proposed for cyclic ADC, which utilizes the redundancy of non-binary AD conversion to tolerate the analog errors caused by circuit element mismatch and non-ideal characteristics of the amplifier and/or comparator in the analog conversion stage, and thus guarantee the linearity of ADC. The body-voltage-control technique is utilized to decrease the threshold voltage of SOTB CMOS, thereby facilitating the low-voltage operation of the ADC circuit. Dynamic analog components such as amplifiers and comparators are utilized for low-voltage operation, while circuit techniques are developed to improve the DC gain and bandwidth of the amplifier. These improvements further enhance the linearity and speed of the ADC at low-supply-voltage. The experimental results of the proposed non-binary cyclic ADCs show that 14-bit linearity can be achieved at Vdd = 0.9V, demonstrating the feasibility and effectiveness of the proposed circuit techniques for high-linearity ADCs at supply voltages below 1V.

Bio: Hao San received M.S. and Dr. Eng. degrees in electronic engineering from Gunma University, Japan, in 2000 and 2004, respectively. From 2000 to 2001, he worked with Kawasaki Microelectronics, Inc. He joined Gunma University as an assistant professor in the Department of Electronic Engineering in 2004. In 2009, he joined Tokyo City University, and is presently a professor in Department of Electrical, Electronics and Communication Engineering there. His research interests include analog and mixed-signal integrated circuits. Dr. San has been an Associate Editor of IEICE Transactions on Electronics from 2010 to 2016. He was the treasurer of the IEEE Circuits and Systems Society Japan Chapter from 2011 to 2012. He is a member of the IEEE, IEICE and IEEJ.

Dr. Hitoshi Aoki

Rohm Semiconductor, Japan

Time:	15:00-15:20, May 6, 2023	**Onsite Room:**	SR903
Zoom ID:	839 7342 5289	**Zoom Link:**	https://us02web.zoom.us/j/83973425289

A Unified Model of MIS and Ridge HEMTs for Fast and High-Power Switching Applications

Abstract: A verilog-A based compact model of AlN/GaN based MIS (Metal Insulator Semiconductor) -HEMT (High Electron Mobility Transistor)s and ridge (Gate Injection Transistor) HEMTs has been developed for embedded-source-field-plate (ESFP) structures. Characteristic differences in these two structures are theoretically and experimentally analyzed with measurements of fabricated devices. For ridge HEMTs, hole injection current and leakage current are focused on, whereas the MIS-HEMTs use a MOSFET gate modeling approach. Also, the parasitic transistor model caused by the ESFP is developed. For high frequency operations, S-parameter characterizations with G-S-G pads structures for both types of HEMTs are fabricated. Because the simulation results show good agreements with the measurements, one model can be applied to both MIS and ridge HEMTs to design switching power supply circuits.

Bio: Dr. Hitoshi Aoki is a technical adviser at Rohm Co. ltd. He had been a professor at Teikyo Heisei University and Gunma University in Japan. He has over 35 years of device modeling experience in electronic industries. Prior to his carrier with Universities, Dr. Aoki founded a modeling company, MoDeCH Inc. in 2002, where he is now an Executive Advisor Consultant. Previously, he had been working at some leading companies of electronics in both the U.S.A. and Japan including the ULSI Research Laboratory of Hewlett-Packard Laboratories U.S.A, Agilent Technology, and Hewlett-Packard Japan. He authored and coauthored two books related to compact modeling and more than 130 technical papers. Dr. Aoki is a senior member of IEEE.

Dr. Kunio Koseki

National Institute of Advanced Industrial Science and Technology, Japan

Time:	15:20-15:40, May 6, 2023	**Onsite Room:**	SR903
Zoom ID:	839 7342 5289	**Zoom Link:**	https://us02web.zoom.us/j/83973425289

Recent Progress in High-Voltage SiC Devices and its Application Development

Abstract: The development of high-voltage power devices using silicon carbide, a next-generation semiconductor material, is progressing. Devices with a rated voltage of up to 3.3 kV have been put into practical use. In recent years, the development of devices with higher withstand voltages up to 13 kV have been developed at the laboratory. In addition, evaluation of the conduction and the switching characteristics have been carried out. Applications development such as inverter circuits have also been studied. In the presentation, we report on the development status of these high-voltage SiC devices and its application.

Bio: Kunio Koseki received the B.S. and M.S. degrees in physics from the University of Tsukuba, Tsukuba, Japan, in 1998 and 2000, respectively, and the Ph.D. degree in engineering from the Graduate University for Advanced Studies, Hayama, Japan, in 2005.

He was working for the research and development of various power supplies with the High Energy Accelerator Research Organization for accelerators and particle physics experiments from 2005 to 2015.

In 2015, he joined the Advanced Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan, as a Senior Research Scientist. His current research interests include various power systems with high-voltage SiC power devices.

Assoc. Prof. Tadashi Itoh

Gunma University, Japan

Time:	13:00-13:20, May 7, 2023	**Onsite Room:**	SR902
Zoom ID:	832 5613 7923	**Zoom Link:**	https://us02web.zoom.us/j/83256137923

Principle and Application of Electrical Impedance Tomography

Abstract: It is well known that the electrical resistance R between cross sections of a columnar conductor of length d and cross-sectional area S can be expressed as R=ρd/S where the proportional constant ρ is the resistivity. Its reciprocal, σ=1/ρ, is called conductivity and expresses how readily electricity flows. Conductivity is a material constant that is independent of the shape and size of the conductor and varies with the type and state of the material (temperature, pressure, water content, etc.). Therefore, by measuring the conductivity, information about the type and state of the substance can be obtained.

Electrical Impedance Tomography (EIT) is a measurement technology in which a large number of electrodes are placed in contact with the surface of the object under measurement, weak currents are applied from the electrodes, and the distribution of electrical conductivity inside the object is estimated and imaged from the measured electrode potential data.

In this talk, the history and current status of EIT will be summarized with a focus on its application to medical imaging, followed by an explanation of its principle in the following order: formulation of the forward problem, finite element method for discretizing and treating continuously distributed potentials and currents in the object, electrode model as an interface to measurement, and algorithm for reconstructing conductivity distribution.

An application to the measurement of body fat distribution, which we are currently developing, will also be introduced.

Bio: Tadashi Ito was born in Tokyo, Japan in 1961. He received the degrees of B.Sc. and M.Sc. in Mathematical Engineering and Information Physics from the University of Tokyo, Tokyo, Japan in 1984 and 1986, respectively. From 1986 to 1990, he was employed at Yokogawa Electric Corp., Tokyo, Japan. From 1990 to 1995, he was a research associate at the University of Tokyo. He received the D. Eng. degree from the University of Tokyo in 1995. In 1995, he joined Gunma University as a lecturer in the Department of Electronic Engineering, and has been an associate professor from 2010. He has been engaged in research and development of various measurement systems such as electrical impedance tomography, application of image analysis, automation of visual inspection and self-localization for autonomous vehicle.

Dr. Nobuhiko Kikuchi
R&D Group, Hitachi Ltd., Japan

Time:	13:20-13:40, May 7, 2023	**Onsite Room:**	SR902
Zoom ID:	832 5613 7923	**Zoom Link:**	https://us02web.zoom.us/j/83256137923

Ultra-low Power Multi-Point Remote Sensing Technology Using Opticlal Fiber Power Supply for Sewage Systems

Abstract: Recent change of climate and growth of environmental awareness encourages the need for close control of sewage systems in metropolitan area, and its sensing and visualization becomes ever important to reduce the risk of its flooding, pollution, odor issues and so on. However, remote sensing of actual underground sewage systems faces many difficulties such as the lack of reliable communication and power feeding media, the risk of submergence, the generation of corrosive and explosive gasses, and so on. To over come it, we have developed an ultra low-power multi-point sensing system utilizing a single strand of optical fiber as power supply and communication media. It enables reliable and fast real-time monitoring and surveillance of various quantities in under-ground sewage systems utilizing diverse sensors and cameras, such as water-height, water quality, gas concentration, surface status of sewage water and its overflow. One of the key challenges of its realization is significant reduction of power consumption, since available power from the optical power supply is tightly limited to less than several milli-watts due to fiber loss, branch loss and power conversion efficiency. This paper will report its concept, circuit design for optical power supply and multi-point bidirectional communication, implementation of low-power sensors and camera, and their performances.

Bio: Nobuhiko Kikuchi received the B.E. and M.E. degrees in precision machinery engineering from Tokyo University, Japan, in 1988, 1990, and the D.E. degree in electrical engineering from Tokyo University, Japan, in 2010. In 1990, he joined Central Research Laboratory, Hitachi Ltd. where he has been working on the research and development of high-speed optical fiber communication covering multilevel coding and non-linear impairments, and low-power environmental sensing systems. His interests span from analogue and digital circuit design, digital signal processing, embedded MPU systems, and system integrations. He has published more than 100 patents and 50 international conference papers as the main author. Dr. Kikuchi is a member of the Institute of Electrical and Electronics Engineers, Inc. (IEEE), and Institute of Electronics, Information, and Communication Engineers (IEICE) of Japan.

Dr. Shiro Hara

National Institute of Advanced Industrial Science and Technology, Japan

Time:	13:40-14:00, May 7, 2023	**Onsite Room:**	SR902
Zoom ID:	832 5613 7923	**Zoom Link:**	https://us02web.zoom.us/j/83256137923

Minimal Fab Using Half-inch Wafers for Low-Volume Device Markets

Abstract: Minimal Fab which is a cleanroom-less compact device fabrication system using half-inch wafer and a localized clean wafer transfer system was developed. The investment costs of Minimal Fab are 1/100 at present and 1/1,000 in the future, compared to the cost of a conventional mega fab using 300 mm wafers. The production targets of Minimal Fab are device markets with wide-variety and low-volume. Another targets are research, development, and prototyping of devices. A prototyping fabrication speed of Minimal Fab is around 20 processes for 8 hours, which is one order faster than a mega fab. This is owing to almost zero waiting time before processes because of a single wafer transfer system, a fast wafer loading into a vacuum chamber within 15 seconds because of a very small air-lock chamber of ~ 1 cm3, full-automatic tool operation, and a small wafer size to decrease process times for scanning type processes, easy user maintenances for cartridge-type material sources and wastes, and a unified user operational interface for all the Minimal Fab tools, etc. This paper overviews the concept, features of Minimal Fab, and fabrication of devices.

Bio: Shiro Hara was born in Tokyo, Japan in 1961. He received his Ph.D in engineering from Waseda University in Japan. In 1989, he joined Waseda Univ. where he was an Assistant Professor. He was a special researcher, basic science program in Riken Institute since 1990. In 1993, he became a researcher of Electrotechnical Laboratory, MITI. He developed a localized clean research system to find elemental cause of variations of electronic device characteristics. In 2007, he proposed the Minimal Fab concept to reduce an investment cost of a semiconductor factory into 1/1000. He apply the localized clean technology to the minimal wafer transfer system. Using this transfer system as the core technology of the minimal fab, he has been developing the minimal fab with around 50 makers. During FY2012-2014, he promoted the national project on the development of Minimal Fab system as the project director. He is a Principal Research Scientist in AIST, METI. Also, he is the representative of Fab System Research Consortium of Minimal Fab Promoting Organization. In 2022, he established a company "Hundred Semiconductors, Inc." focusing only to Minimal Fab businesses and he is CTO of the company.