Master degree presentation
January 16th, 2023

Study on Incremental/ Delta-Sigma/ Folding ADCs, and Relaxation DAC

トリノ工科大学(伊)
からの発表の拡張

Division of Electronics & Informatics,
Faculty of Science and Technology

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Presenter
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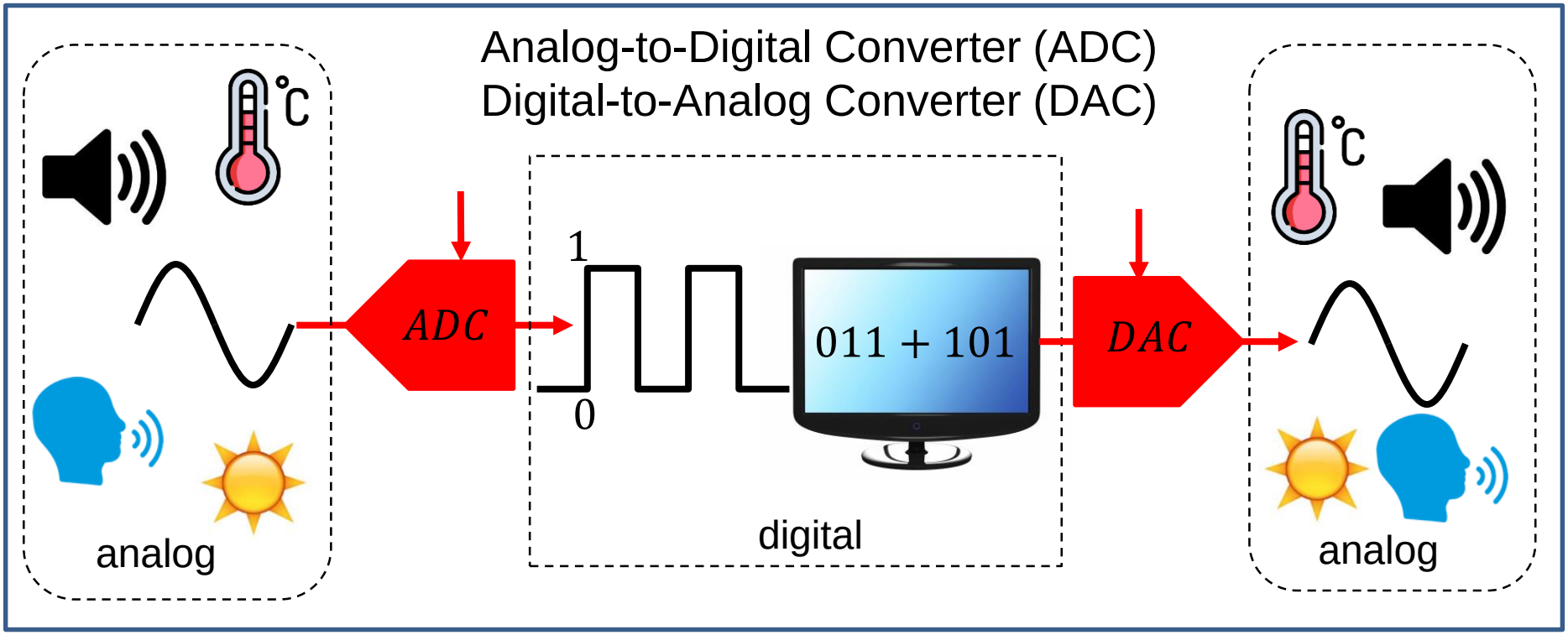
What's ADC and DAC ?

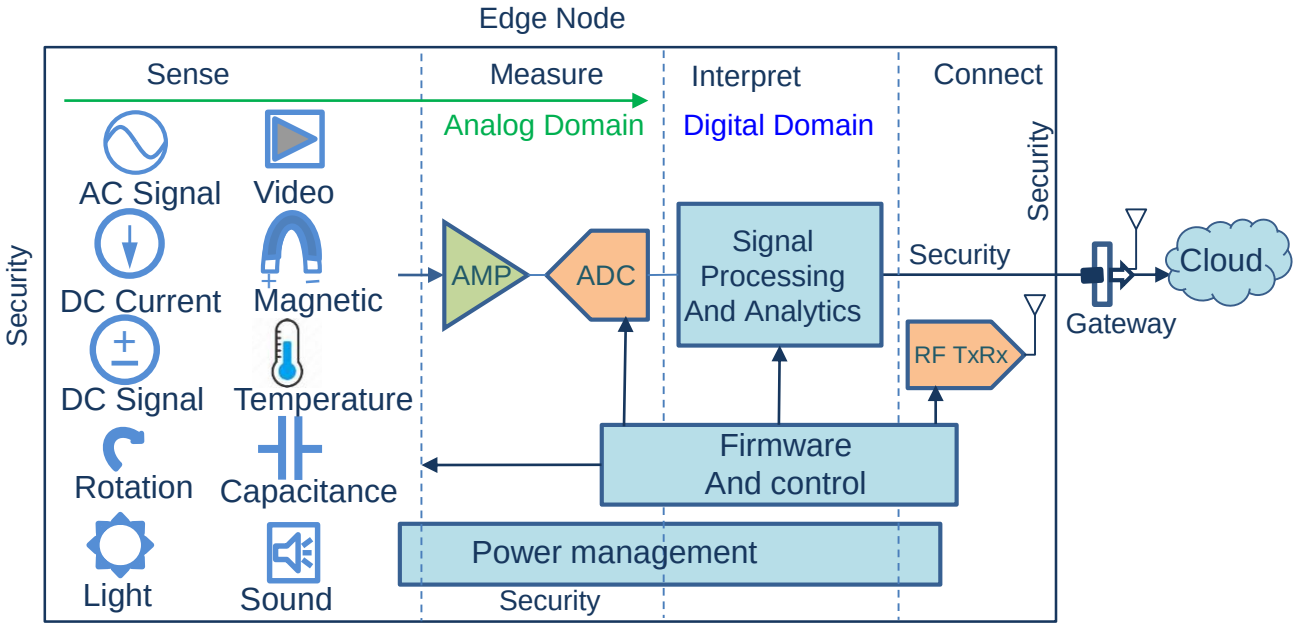


- Natural signals are analog signals
- Digital signals are suitable for signal processing

ADC and DAC interface circuits are important

Research Motivation

IoT node structure



Integrated circuits

ADCs and DACs are key elements in sensor interface circuits

Data converters which features with circuit simplicity, low power and high accuracy receive a lot of attention

Research Topics

1. **Self-Calibration of Two Reference Voltages Ratio for Two-step Incremental Delta-Sigma ADC**

2. **Extended Leslie-Singh Architecture of 1st order Delta-Sigma ADC Modulator with Multi-bit DAC**

3. **Relaxation DAC with Positive and Negative Polarity Output using High-Pass Filter**

OUTLINE

3-1. Conventional ReDAC with LPF

- Operation principle
- Simulation verification

3-2. Proposed ReDAC with HPF

- Operation principle
- Simulation verification

3-3. Conclusion

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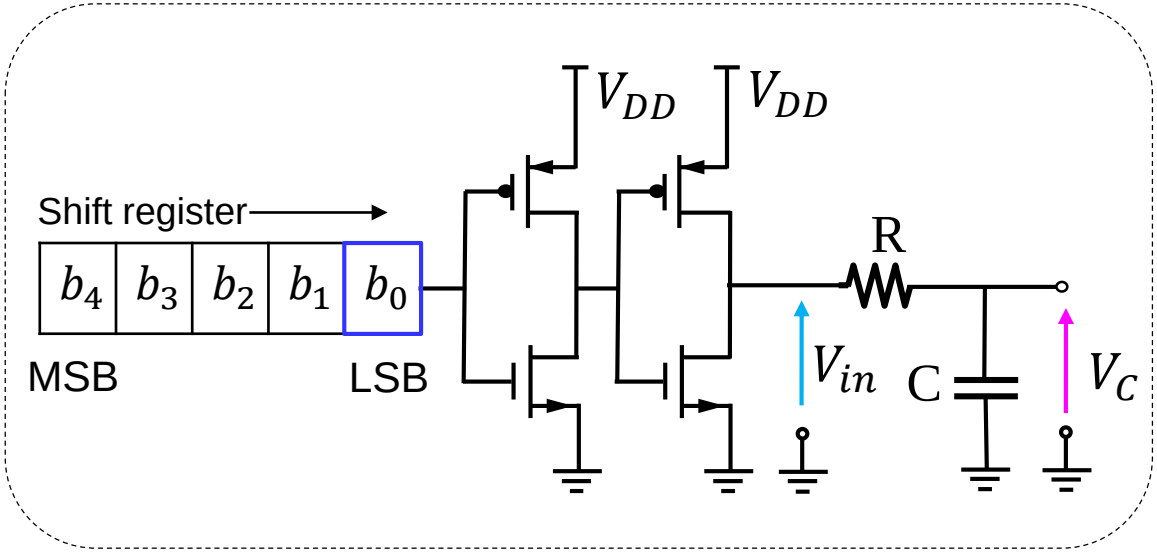
Operation principle

First order RC network

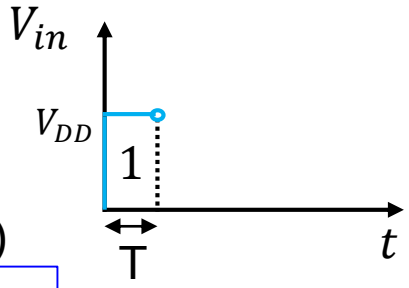
$\tau = RC$

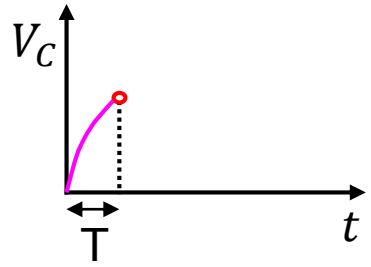


- 1st order RC network driven by digital stream
- Input bits $b_0 \dots b_{n-1}$ applied LSB-first to the RC
- After the MSB, the output buffer is put in high impedance

Input code

$$N = \sum_{i=0}^{n-1} b_i 2^i$$





Example: N=21 ($b_4 b_3 b_2 b_1 b_0$=10101 binary)

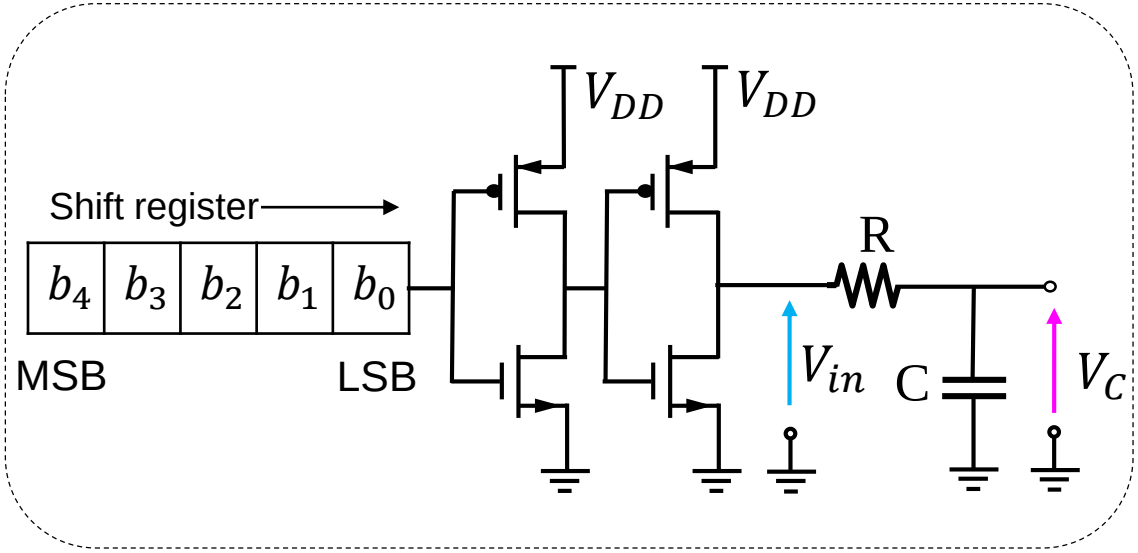
$N = 1 \cdot 2^0 + 0 \cdot 2^1 + 1 \cdot 2^2 + 0 \cdot 2^3 + 1 \cdot 2^4 = 21$

P. S. Crovetti, R. Rubino and F. Musolino, “Relaxation digital-to-analogue converter,” in Electr. Letters, 2019.
R. Rubino, et al. “Design of Relaxation digital-to-analogue Converters for IoT Applications in 40nm CMOS,” APCCAS 2019.

Operation principle

First order RC network

$\tau = RC$



- The final capacitor voltage is the result of the conversion:

$$V_C(nT) = V_{DD}\left(1 - e^{-\frac{T}{\tau}}\right) \cdot \sum_{i=0}^{n-1} b_i e^{-\frac{(n-i-1)T}{\tau}}$$

ReDAC condition

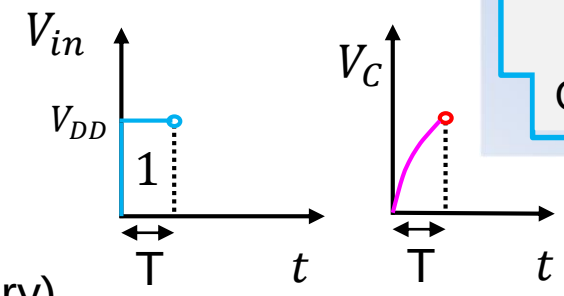
$$e^{-\frac{T}{\tau}} = \frac{1}{2} \Rightarrow T = \tau \cdot \log 2$$

$$V_C(nT) = \frac{V_{DD}}{2^n} \sum_{i=0}^{n-1} b_i 2^i = \frac{N}{2^n} \cdot V_{DD}$$

Output Voltage proportional to N

Input code

$$N = \sum_{i=0}^{n-1} b_i 2^i$$



Example: N=21 (10101 binary)

P. S. Crovetti, R. Rubino and F. Musolino, “Relaxation digital-to-analogue converter,” in Electr. Letters, 2019.
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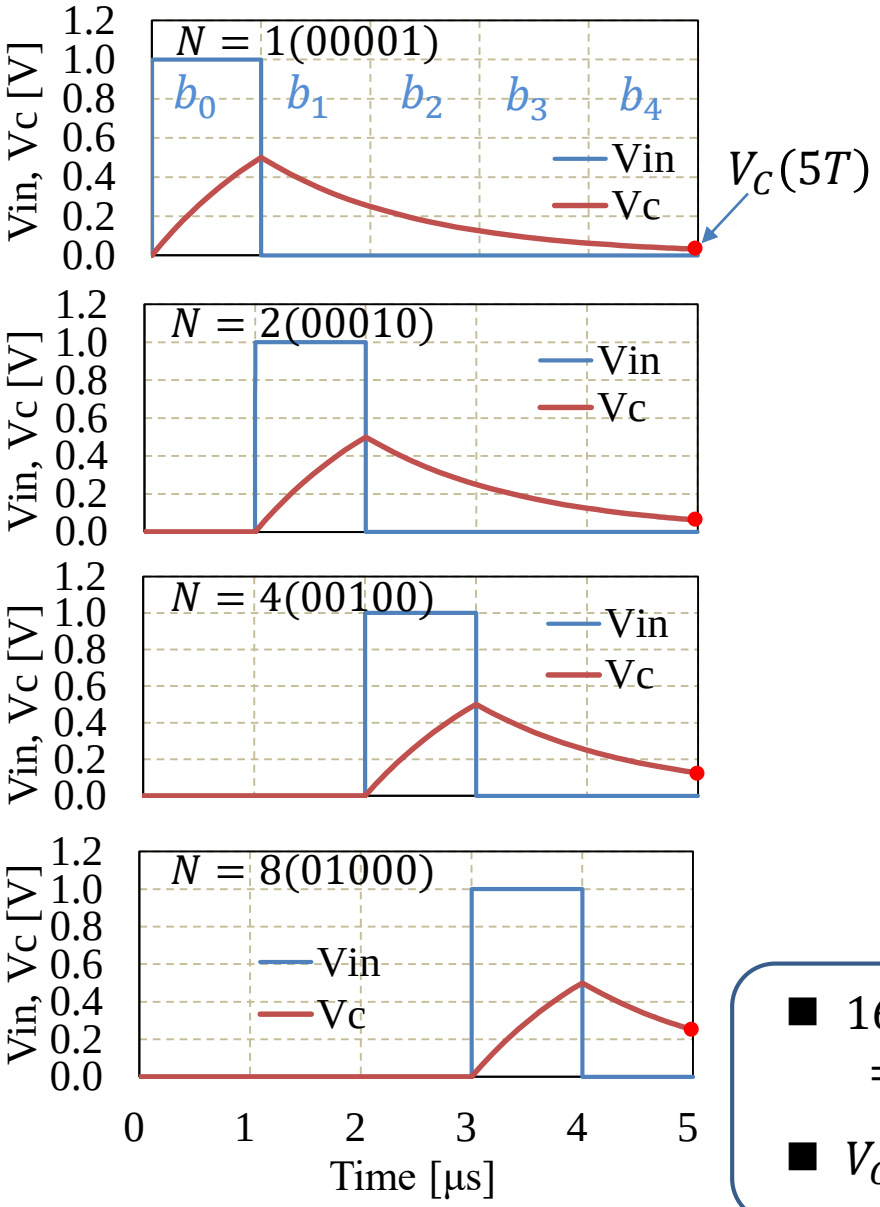
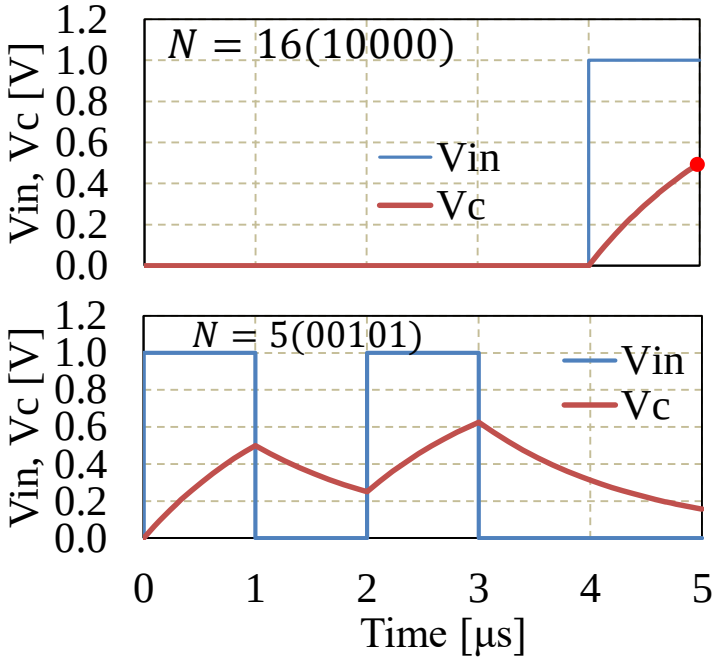
Simulation verification



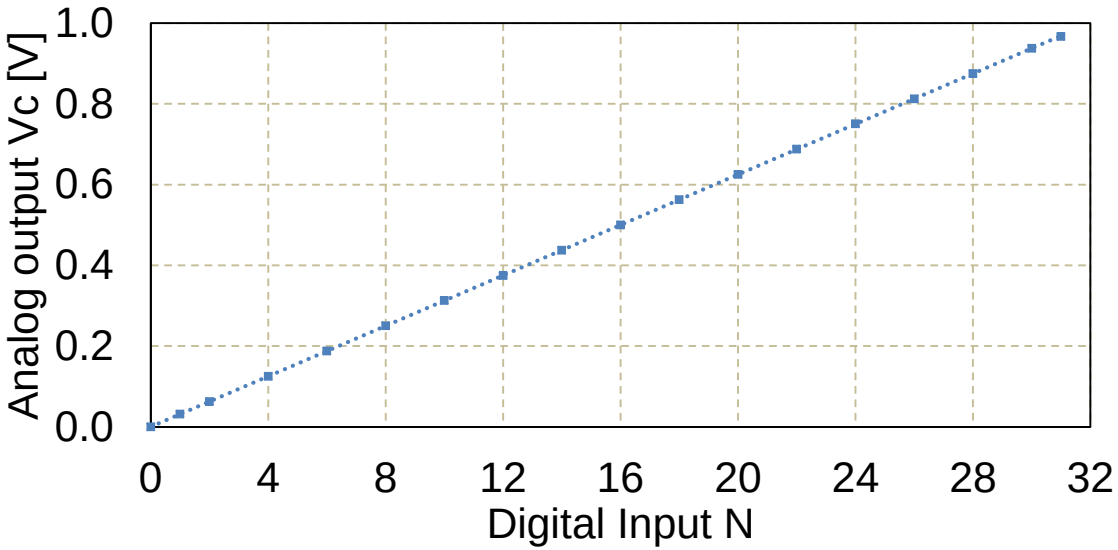
parameters	value
R	1 [kΩ]
C	1.443 [nF]
T	1 [μs]
V_{DD}	1 [V]



- $16V_C(5T)|_{N=1} = 8V_C(5T)|_{N=2} = 4V_C(5T)|_{N=4} = 2V_C(5T)|_{N=8} = V_C(5T)|_{N=16} = 0.5\ [V]$
- $V_C(5T)|_{N=5} = V_C(5T)|_{N=1} + V_C(5T)|_{N=4}$

Simulation verification

Digital input N		Analog output @
Decimal	Binary ($b_4b_3b_2b_1b_0$)	$V_C(5T)$ **[V]**
1	00001	0.03125
2	00010	0.06250
4	00100	0.12500
5	00101	0.15631
7	00111	0.21887
8	01000	0.25000
16	10000	0.50000



☑ Analog output is proportional to the digital input data N

✕ Analog output generates with only positive polarity

✕ Negative digital input data is not available

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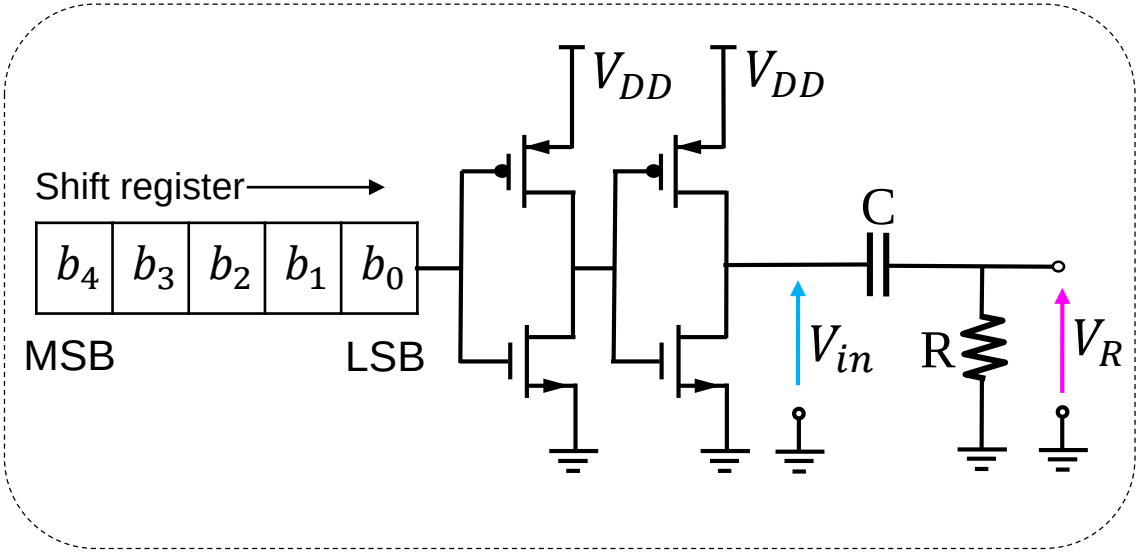
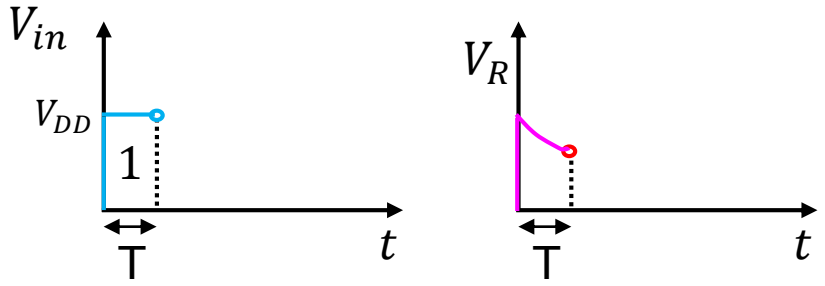


- 1st order RC network driven by digital stream
- Input bits $b_0 \ldots b_{n-1}$ applied LSB-first to the RC
- After the MSB, the output buffer is put in high impedance

Input code

$$N = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-1} b_i 2^i$$



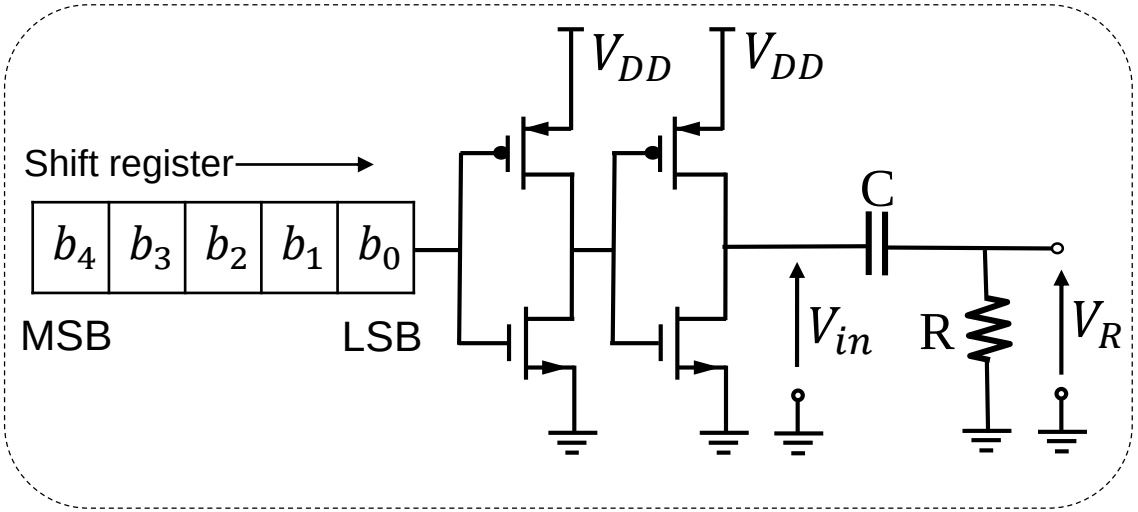
Example: N=-11 (10101 binary)

Operation principle

Input code

$$N = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i$$

Example: N=-11 (10101 binary)



- The final resistor voltage is the result of the conversion

$$V_R(nT) = -V_{DD}\left(-b_{n-1}e^{\frac{(n-1)T}{\tau}} + \sum_{i=0}^{n-2} b_i e^{-\frac{(n-i-1)T}{\tau}}\right)$$

ReDAC condition

$$e^{-\frac{T}{\tau}} = \frac{1}{2} \Rightarrow T = \tau \cdot \log 2$$

$$V_R(nT) = -\frac{V_{DD}}{2^n}\left(-b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i\right) = -\frac{N}{2^n} \cdot V_{DD}$$

Output Voltage proportional to N

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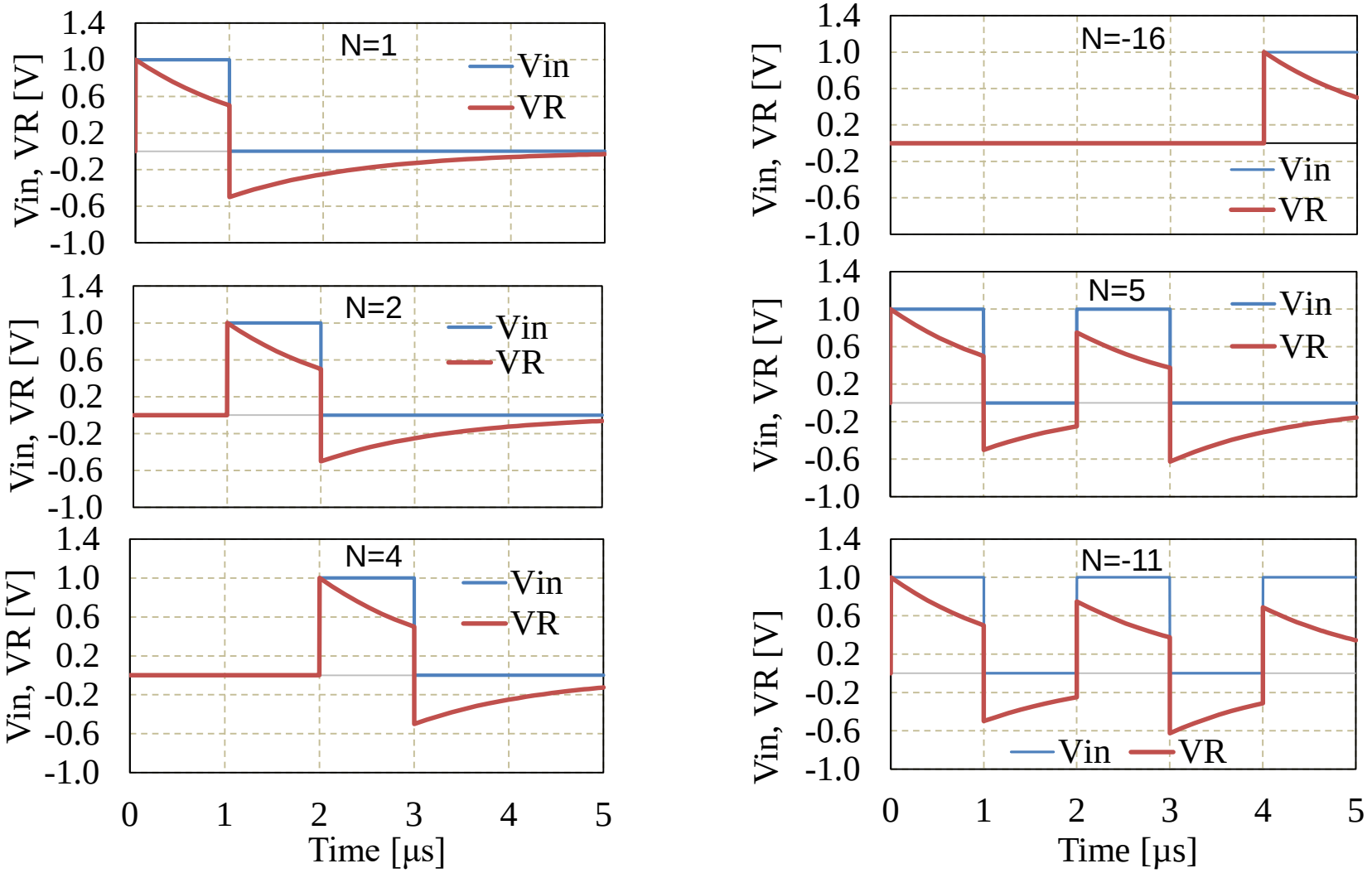
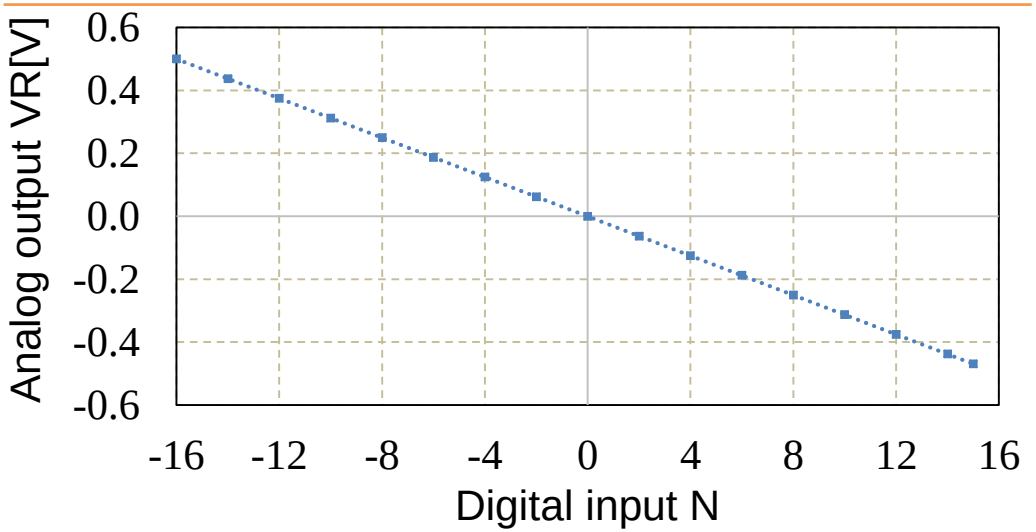


- $V_R(5T)|_{N=5} = V_R(5T)|_{N=1} + V_R(5T)|_{N=4}$
- $V_R(5T)|_{N=-11} = V_R(5T)|_{N=1} + V_R(5T)|_{N=4} + V_R(5T)|_{N=-16}$

Simulation Verification

Digital input N		Analog output @ $V_R(5T)$ [V]
Decimal	Binary ($b_4b_3b_2b_1b_0$)	
1	00001	-0.03125
2	00010	-0.06250
4	00100	-0.12500
5	00101	-0.15625
7	00111	-0.21875
8	01000	-0.25000
-16	10000	0.50000
-11	10101	0.34375
-9	10111	0.28125



- ☑ Analog output is proportional to the digital input data N
- ☑ Analog output generates with both positive and negative polarity
- ☑ Input data is available for two's implement format

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Conclusion

Proposed ReDAC with HPF

- ✓ Analog output is proportional to digital Input.
- ✓ Output generates both positive and negative polarity
- ✓ Two’s complement format is usable for input

Future work:

- ➢ Prototype implementation and performance evaluation

List of publications

Journal paper

1. Lengkhang Nengvang, Shogo Katayama, Anna Kuwana, Kazufumi Naganuma, Kiyoshi Sasai, Akihisa Iikura, Akira Asao, Takuya Watanabe, Katsuaki Morishita, Haruo Kobayashi, “Relaxation DAC with Positive and Negative Polarity Output using High-Pass Filter,” IEICE Electronics Express (Advance online publication: January 17, 2023)