Spread-Spectrum Clocking in Switching Regulators to Reduce EMI

H. Sadamura, T. Daimon, T. Shindo, H. Kobayashi, M. Kono
EE Dept. Gunma University, Japan

T. Myono, T. Suzuki, S. Kawai, T. Iijima
Sanyo Electric Co. Ltd., Japan
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- Research Background and Goal
- Principle of DC-DC Converters
- Proposal of Noise Power Spectrum Spread Method in DC-DC Converters
- Implementation and Measurement Results
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Research Background

- Mobile equipment prevails everywhere
- Mobile phone, Digital still camera, PDA

- Small size, High efficiency
- Multiple supply voltages
- Low-voltage supply
Features of Switching Regulator

**Merit**
- High efficiency
- Continuously varying output voltage
- Large output current

**Demerit**
- Coil is required. bulky and costly
- Switching noise
We focus on a big problem of switching regulator: “Switching and harmonic noises”

Proposal of EMI reduction technique
by spreading noise power spectrum
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Principle of DC-DC Converter(1)

In case Clk=ON

\[
\Delta I_{L1} = \frac{V_{dd} - V_{out}}{L} \times T_{on}
\]

In case Clk=OFF

\[
\Delta I_{L2} = -\frac{V_{out}}{L} \times T_{off}
\]

\[
V_{out} = \frac{T_{on}}{T} \cdot V_{dd}
\]

\[
\Delta I_{L1} = \Delta I_{L2}
\]

T; clock period

Output voltage $V_{out}$ is determined by the clock duty.
- **V<sub>dd</sub>**: Input voltage
- **CLK**: Switching clock
- **L, C**: Low pass filter for smoothing
- **V<sub>out</sub>**: Output voltage

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![Circuit Diagram]

**LPF**

- **10V**

- **CLK**

- **DUTY=25%**
  - **CLK**: 2.5V
  - **OUT**: 2.5V

- **DUTY=50%**
  - **CLK**: 5V
  - **OUT**: 5V

- **DUTY=75%**
  - **CLK**: 7.5V
  - **OUT**: 7.5V
DC-DC Converter with PWM Controller

Error amplifier output

Triangular wave

Comparator output

Error amplifier output

Vcc 3.3[V]
Features of PWM Control

**Advantage**
- ON/OFF switching
- High efficiency
- Negative feedback control
- Output is stable regardless of output load.

**Disadvantage**
- Synchronization with clock
- Harmonic noises in specific frequencies
EMI and Switching Regulator

Shield is required to meet EMI Regulations

Proposal of EMI reduction circuit
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Generated switching noise power spectrum are in specific frequencies.

By spreading the spectrum of switching noise power, EMI reduction is realized.
Principle of Pseudo-Random Digital Modulation (PRM)

- Effect of \( V = L \frac{di}{dt} \)
- Switching Control with Pulse

Driving Clock

Regulator Output

Normal Clock

PRM Clock

Phase Modulation

Switching Noise

Large Switching Noises

Large Harmonic Noises

Pseudo-Random Spread Spectrum of Noise Power
PRM Circuit Implementation

- 3bit LFSR case -

Reset

Input

Clock

LFSR

MUX

SEL1

SEL2

SEL3

in1

in2

in6

in7

Shift Register
DC-DC Converter with PRM

Proposed PRM Circuit

PWM Controller

Control Circuit

Conventional Circuit

(No need for modification)
Optimal Clock Phase Shift(1)

- When clock phase shift is too large, output ripple becomes too large.

- When clock phase shift is too small, noise spectrum are not spread sufficiently.

Normal clock (Conventional)

PRM clock (proposed)

Optimal phase shift is obtained by measurement.
Optimal value of maximum phase shift ($T_{shift}$)

$$T_{shift} = \frac{T_{pwm}}{2}$$

$T_{pwm} = $PWM clock period
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**Evaluation Board**

Technology: FLEX10K30EQC208 –3 (Altera)

<table>
<thead>
<tr>
<th>Item</th>
<th>Spec.</th>
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<tbody>
<tr>
<td>Spectrum Spread Method</td>
<td>Direct</td>
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<tr>
<td>Shift Register Clock</td>
<td>6MHz</td>
</tr>
<tr>
<td>PWM Input</td>
<td>187kHz</td>
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<tr>
<td>PN—code Control Clock</td>
<td>187kHz</td>
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<tr>
<td>Supply Voltage</td>
<td>3.3V</td>
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<tr>
<td>PN-code</td>
<td>M-Sequencer</td>
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<tr>
<td>Code Length</td>
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<tr>
<td>The Number of DFFs</td>
<td>37</td>
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Measurement Setup

Measurement Setup diagram showing the connection of a flex board, PWM control circuit, shift register, spectrum analyzer, and Buck converter. The diagram includes labeled components such as V_{dd}, PWMOUT, Driver Circuit, μPC1933(PWM), f_{data}, f_{clk}, Reset, Mux, and GPIB interface.
Measured Power Spectrum of Driving Clock

Power spectrum of PRM output clock with 5bit M-sequencer (Proposed)

Maximum peak reduction by 12.7dBm
Input voltage $V_{dd}=3.3\,\text{V}$, Clock duty = 50\%

Amplitude [V]  

Output waveform with normal clock  
(Conventional)

Output waveform with PRM clock.  
(Proposed)
Measured Output Power Spectrum of DC-DC Converter

Output power spectrum with normal clock (Conventional)

Output power spectrum with PRM clock (Proposed)

Maximum peak reduction by 12.3 dBm
Clock Duty vs. Output Voltage

Match to the theoretical output voltage.

The proposed method does not affect the (average) output voltage.
The proposed method does not affect efficiency.
Peak Noise Power Spectrum vs. the Number of M-Sequencer Bits

5-bit and 6-bit are reasonable trade-off.

Peak Noise Power Spectrum of Driving Clock

Peak Noise Power Spectrum of Switching Regulator Output
Summary

Proposal of Noise Power Spectrum Spread Technique
- Addition of simple digital circuitry can realize EMI reduction.
  - Low cost, Low power
  - Robust against temperature variation, aging
- No need for modification of the other parts.
- Applicable also for voltage-boosting converter.

Implementation with FPGA

Confirmation of its effectiveness by measurements

Reduction by

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<tbody>
<tr>
<td>Max. Peak</td>
<td>12.3dBm</td>
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<tr>
<td>Fundamental</td>
<td>5.7dBm</td>
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<tr>
<td>2nd-harmonics</td>
<td>15.6dBm</td>
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<tr>
<td>3rd-harmonics</td>
<td>12.8dBm</td>
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