SAR ADC Algorithm with Redundancy

Tomohiko Ogawa, Haruo Kobayashi, Masao Hotta† Yosuke Takahashi, Hao San and Nobukazu Takai
Dept. of Electronic Engineering, Gunma University, Email: m08e610@gs.eng.gunma-u.ac.jp
† Dept. of Information Network Eng., Musashi Institute of Technology

***Abstract*— This paper describes a redundant algorithm for a highly reliable Successive Approximation Register (SAR) ADC where mistakes of comparator decision can be digitally-corrected. We generalize a conventional non-binary search algorithm which requires more conversion steps in the SAR ADC than the binary search algorithm, and clarify which decision errors can be digitally-corrected with the derived redundant algorithm. We also shows that the sampling speed of the SAR ADC using the proposed algorithm can be faster when the incomplete settling effects of the DAC inside the SAR ADC are taken into account.**

Keywords: SAR ADC, Digital Error Correction, Non-binary, Redundancy

I. Introduction

The automotive electronics technology is the spotlight in recent years [1], and there an SAR ADC embedded in a micro-controller chip is widely used and high reliability, high speed, high accuracy, low power and low cost are demanded.

In this paper we investigate a generalized non-binary algorithm which uses one comparator and requires M steps for N-bit resolution where M > N or in other words the number of the steps is redundant. Non-binary algorithms are used in SAR ADC [4,5] with the radix of $2^{N/M}$, but here we avoid such radix restriction and generalize the non-binary algorithm. We present its design method and possible error correction range, and show that the SAR ADC with this algorithm can be faster than the one with the binary search algorithm or the conventional non-binary search algorithm when we consider the incomplete settling effects of the DAC inside the ADC.

II. SAR ADC

SAR ADC Characteristics : An SAR ADC is widely used for high resolution (10-14bit) and middle sampling speed applications, such as automotive, factory automation and pen digitizer [2]- [5]. It can be realized with small chip area and consumes only low power.

SAR ADC Configuration: An SAR ADC is composed of a sample hold circuit, a comparator, a DAC, SAR logic circuit and timing generator (Fig.1).

SAR ADC Operation: Operation of a basic SAR ADC is based on binary search algorithm or "principle of a balance"(Fig.2).

III. Binary search algorithm

This section explains the binary search algorithm which realizes N-bit resolution SAR ADC with N-step, and we assume that the analog input range is normalized from 0 to $2^N - 1$. The comparator compares the analog input (V_{in}) and the reference voltage (DAC output). The reference voltage in the first step($V_{ref}(1)$) is given by $V_{ref}(1) = 2^{N-1}$. If the output of the comparator in (k-1)-th step ($d(k-1)$) is "1", the reference voltage in k-th step($V_{ref}(k)$) is given by

$$V_{ref}(k) \quad = \quad V_{ref}(k-1) + 2^{N-k}.$$

If the output of the comparator in (k-1)-th step($d(k-1)$) is "0", $V_{ref}(k)$ is given by

$$V_{ref}(k) \quad = \quad V_{ref}(k-1) - 2^{N-k}.$$

$$\text{Thus} \qquad V_{ref}(k) \quad = \quad 2^N \cdot \big(2^{-1} + \sum_{i=2}^{k} d(i-1)2^{-i}\big).$$

Then, the ADC output D_{out} is given by

$$D_{out} = d(0)2^{N-1} + d(1)2^{N-2} + ... + d(N-2)2 + d(N-1).$$

We see that if comparator decision errors occur, D_{out} cannot be corrected because there is no redundancy.

IV. Conventional Non-binary Algorithm

This section explains a conventional non-binary search algorithm which realizes N-bit resolution SAR ADC in M steps (N ≤ M) using the radix of $2^{N/M}$. In this algorithm, the reference voltages (which is different from the one with the binary search algorithm) are given by

$$V_{ref}(k) \quad = \quad 2^N + \big(\sum_{i=2}^{k} d(i-1)\gamma^{-i}\big).$$

Here $\gamma = 2^{N/M}$. The SAR ADC digital output is given by

$$D_{out} \quad = \quad 2^N + \big(\sum_{i=2}^{M} d(i-1)\gamma^{-i}\big) + \frac{1}{2}d(M) - 0.5.$$

The conventional non-binary algorithm is restricted to the radix γ of $2^{N/M}$.

V. Generalized Non-binary Algorithm

In this section, we propose a generalized non-binary algorithm which realizes N-bit resolution SAR ADC in M steps (N ≤ M) but it is not restricted to the radix of $2^{N/M}$. We give the reference voltage in k-th step($V_{ref}(k)$) as follows:

$$V_{ref}(k) \quad = \quad \sum_{i=1}^{k} d(i-1)p(i), \ (k = 1, 2, .., M). \qquad (1)$$

Here $p(k)$ is the value for addition (or subtraction) to the reference voltage in the previous step. Then we have the following ADC digital output :

$$D_{out} \quad = \quad \sum_{i=1}^{M} d(i-1)p(i) + \frac{1}{2}d(M) - 0.5. \qquad (2)$$

We have derived that $p(i)$ must satisfy the following:

$$p(1) = 2^{N-1} \quad (3)$$

$$\sum_{i=1}^{M} p(i) = 2^N - 1 + 2 \cdot (\text{over-range}). \quad (4)$$

Note that

- if $N = M$ and $p(i) = 2^{N-i}$, it is equivalent to the binary search algorithm.
- if $p(i) = \gamma^{-i}$ ($\gamma = 2^{N/M}$ and $1 < \gamma < 2$), it is the conventional non-binary search algorithm with radix γ.

Here "over range (r)"is defined as follows: for example, the output range of an ordinary 5-bit resolution SAR ADC is from 0 to 31, but the one with the generalized non-binary algorithm of Fig.3 is from -3 to 34. We call here the range from -3 to -1 and also the one from 32 to 34 as over-range ($\pm$3LSB) and $r = 3LSB$.

Example 1: Fig.2 shows the reference voltages of a 5-bit resolution 5-step SAR ADC with the binary search algorithm, where $N = 5, M = 5, p(1) = 16, p(2) = 8, p(3) = 4, p(4) = 2, p(5) = 1$.

Example 2: Fig.3 shows the reference voltages of a 5-bit resolution 6-step SAR ADC using the proposed generalized non-binary algorithm with over-range $r = 2$, $N = 5, M = 6, p(1) = 16, p(2) = 7, p(3) = 5, p(4) = 3, p(5) = 2, p(6) = 1$.

Example 3: Fig.4 shows another case of reference voltages of a 5-bit resolution 6-step SAR ADC with the proposed algorithm, where over-range $r = 0$, $N = 5, M = 6, p(1) = 16, p(2) = 7, p(3) = 4, p(4) = 2, p(5) = 1, p(6) = 1$. Fig.5 explains this SAR ADC operation that the analog input is 23.5 and the output of comparator takes a mistake in second step, but we obtain correct ADC digital output.

Example 4: Fig.6 shows another case of reference voltages of a 5-bit resolution 6-step SAR ADC with the proposed algorithm where over-range $r = 0$, $N = 5, M = 6, p(1) = 16, p(2) = 4, p(3) = 4, p(4) = 4, p(5) = 2, p(6) = 1$.

VI. Non-binary Search Algorithm and Digital Error Correction

In the non-binary search algorithm using (2), we see that there are 2^M comparison patterns and 2^N output patterns, and since M is bigger than N, 2^M is bigger than 2^N. In other word, for a given output level D_{out}, there can be multiple comparison patters, which means that there is some redundancy. Thus even if a comparator decision takes a mistake at some stage, we may have correct ADC output.

VII. Analysis of redundancy in generalized non-binary search algorithm

We define "the redundancy in k-th step ($q(k)$)"as follows:

$$q(k) = -p(k+1) + 1 + \sum_{i=k+2}^{M} p(i). \quad (5)$$

$q(k)$ in (5) indicates the overlap range between output ranges of one comparison pattern and other pattern in k-th step. Comparator decision error can be corrected in this range.

Proposition 1: Even if a comparator take a mistake in k-th step, but if $|V_{in} - V_{ref}(k)| < q(k)$ is satisfied, we obtain correct ADC output.

Fig.5 shows one example, where the analog input (V_{in}) is 23.5. The input is compared with $V_{ref}(1) = 16$ in the first step, and the comparator decision is correct. In the second step the input is compared with $V_{ref}(2) = 23$, but the comparator is not correct. However we obtain the correct ADC output because $|V_{in} - V_{ref}(2)| < q(2), (q(2) = 1)$ is satisfied.

In case of an N-bit M-step SAR ADC with the generalized non-binary algorithm, we have derived the design method of error correction range or redundancy $q(k)$ $(k = 1, 2, ..., M)$, and the calculation method of $p(k)$ $(k = 1, 2..., M)$ as follows:

Proposition 2:

$$2^M - 2^N = (\sum_{i=1}^{M-1} 2^i q(i)) + 2 \cdot \text{over-range}. \quad (6)$$

Proof: It follows from eq.(5) that

$$p(k+1) = -q(k) + 1 + \sum_{i=k+2}^{M} p(i). \quad (7)$$

Then we have

$$p(k+1) = -q(k) + 2^{M-k-1} - \sum_{i=k+1}^{M-1} 2^{i-k-1} q(i). \quad (8)$$

We have the following for $k = 1$ from eq.(8):

$$p(2) = -q(1) + 2^{M-2} - \sum_{i=2}^{M-1} 2^{i-2} q(i) \quad (9)$$

$$2^{M-2} = p(2) + q(1) + (\sum_{i=2}^{M-1} 2^{i-2} q(i)) \quad (10)$$

$$2^M = 4p(2) + 4q(1) + \sum_{i=2}^{M-1} 2^i p(i). \quad (11)$$

Also we have the following for $k = 1$ from eq.(7):

$$p(2) = -q(1) + 1 + \sum_{i=3}^{m} p(i). \quad (12)$$

From eq.(12) we have

$$2p(2) = -q(1) + 1 + \sum_{i=2}^{M} p(i). \quad (13)$$

Also from eqs.(13) and (11) we have

$$2^M = 2[-q(1) + 1 + \sum_{i=2}^{M} p(i)] + 4q(1) + \sum_{i=2}^{M-1} 2^i q(i) \quad (14)$$

$$2^M = 2[1 + \sum_{i=2}^{M} p(i)] + \sum_{i=1}^{M-1} 2^i q(i). \quad (15)$$

In eq.(15), 2^M of the left side term is the number of the total comparison patterns and $2(1+\sum_{i=2}^{M} p(i))$ of the right side is that of the total output levels. In case N-bit resolution, the number of the necessary output levels is 2^N, and hence $2(1+\sum_{i=2}^{M} p(i)) = 2^N + 2 \cdot$ (over-range). Thus eq.(15) yields to

$$2^M - 2^N = \left(\sum_{i=1}^{M-1} 2^i q(i) \right) + 2 \cdot \text{(over-range)}.$$

(Q.E.D).

Example 1: Fig.2 shows the case that $N = 5, M = 5, p(1) = 16, p(2) = 8, p(3) = 4, p(4) = 2, p(5) = 1$, $q(1) = q(2) = q(3) = q(4) = q(5) = 0$.

Example 2: Fig.3 shows the case that over-range $r = 3$, $N = 5, M = 6, p(1) = 16, p(2) = 7, p(3) = 5, p(4) = 3, p(5) = 2, p(6) = 1$, $q(1) = 5, q(2) = 2, q(3) = 1, q(4) = 0, q(5) = 0$. The following are satisfied which agrees with eq.(11):

$$\begin{aligned} p(2) &= 16 - q_(1) - q(2) - 2q(3) - 4q(4) - 8q(5) = 7 \\ p(3) &= 8 - q(2) - q(3) - 2q(4) - 4q(5) = 5 \\ p(4) &= 4 - q(3) - q(4) - 2q(5) = 3 \\ p(5) &= 2 - q(4) - q(5) = 2 \\ p(6) &= 1 - q(5) = 1. \end{aligned}$$

As eq.(6) is satisfied,

$$2^6 - 2^5 = 2q(1) + 4q(2) + 8q(3) + 16q(4) + 32q(5) + 2r.$$

Example 3: Fig.4 shows the case that over-range $r = 0$, $N = 5, M = 6, p(1) = 16, p(2) = 7, p(3) = 4, p(4) = 2, p(5) = 1, p(6) = 1$, $q(1) = 2, q(2) = 1, q(3) = 1, q(4) = 1, q(5) = 0, q(6) = 0$.

Example 4: Fig.6 shows the case that over-range $r = 0$, $N = 5, M = 6, p(1) = 16, p(2) = 4, p(3) = 4, p(4) = 4, p(5) = 2, p(6) = 1$, $q(1) = 8, q(2) = 4, q(3) = 0, q(4) = 0, q(5) = 0, q(6) = 0$.

Remarks : (i) If an N-bit M-step SARADC with the proposed algorithm is designed to satisfy eq.(6) for redundancy of each steps $q(k)$ and over-range r, $p(k)$ that realize these values can be calculated with eq.(8).

(ii) $\sum_{i=1}^{M-1} 2^i q(i)$ is the total number of error correction patterns. Its reason is as follows: in eq.(6), $\sum_{i=1}^{M-1} 2^i q(i)$ is equal to (the number of the total comparison patterns) - (the number of the total output levels). Since the number of the total patterns when all comparator decisions are correct is equal to the number of the total output patterns, $\sum_{i=1}^{M-1} 2^i q(i)$ is the number of the total error correction patterns.

(iii) Coefficient of $q(i)$, "2^i", of $\sum_{i=1}^{M-1} 2^i q(i)$ in eq.(6) can be explained as follows: 2^{i-1} is the number of the total comparison patterns from the first step to i-th step, and 2 is the number of correction cases: one case is that "1"is error, and another case is that "0" is error. Therefore, the sum of length of all arrows of $q(i)$ in Fig.3 is equal to $\sum_{i=1}^{M-1} 2^i q(i)$.

(iv) The circuit complexity for the generalized non-binary algorithm implementation is almost the same as the one for the conventional non-binary one (we just need to change the data of coefficient ROMs [4], [5]).

VIII. DAC Incomplete Settling

We consider the incomplete settling effects of the DAC for generating the reference voltage inside the SAR ADC. We assume that the DAC is the first-order system with a time constant of τ. When the reference voltage changes from V_0 to V_{ref} during time t, the reference voltage (the DAC output) has error due to incomplete settling as below:

$$V_{ref,er}(t) = V_{ref} - (V_{ref} - V_0)e^{-\frac{t}{\tau}}.$$

When time slot "t" is long enough, the error becomes small. Also note that the error becomes smaller in later step because change of the reference voltage between steps becomes smaller. Note that the SAR ADC with the binary algorithm has to wait for the DAC to settle within 1/2 LSB in each step. Non-binary search algorithm can correct error due to the DAC incomplete settling at early step, and we do not have to wait for the DAC to settle within 1/2 LSB. Also we can do optimal design using the proposed non-binary algorithm. We have simulated and compared the speed (conversion time) the SAR ADCs with the following conditions:

- 14-bit resolution
- SAR ADC can has correct ADC output.
- Time slot of each step is the same.

Table 1 shows the simulated conversion time comparison among the SAR ADC with the binary algorithm, the conventional non-binary algorithm and the generalized non-binary algorithm. We see that the SAR ADC with the generalized non-binary algorithm the fastest. We also found from simulation that as the resolution (number of bits) of the SAR ADC increases, it is more effective.

TABLE I

SAR ADC CONVERSION SPEED COMPARISON

Algorithm	Binary	Conventional	Generalized
Time slot for each step	8.4τ	2.2τ	1.2τ
Number of steps	14	17	22
Total conversion time	109.2τ	35.2τ	25.2τ

IX. Conclusion

We have proposed and analyzed a generalized non-binary algorithm for a high reliability, high speed SAR ADC. We have developed its design method, and also shown that the SAR ADC with the proposed algorithm is faster than the one with the binary search or conventional non-binary algorithm when we takes the DAC incomplete settling effects into accounts.

References

[1] *ISSCC Short Course, Automotive Technology and Circuits* (Feb. 2005).

[2] M. Hotta, A. Hayakawa, N. Zhao, Y. Takahashi, H. Kobayashi, "SAR ADC Architecture with Digital Error Correction", *IEEJ International Analog VLSI Workshop*, Hangzhou, China (Nov. 2006).

[3] S. Shimokura, M. Hotta, Y. Takahashi, H. Kobayashi, "Conversion Rate Improvement of SAR ADC with Digital Error Correction," *IEEJ International Analog VLSI Workshop*, Limerick, Ireland (Nov. 2007).

[4] M. Hesener, T. Eichler, A. Hanneberg, D. Herbison, F. Kuttner, H. Wenske, "A 14b 40MS/s Redundant SAR ADC with 480MHz Clock in 0.13μm CMOS," *Tech. Digest of ISSCC* (Feb. 2007).

[5] F. Kuttner, "A 1.2V 10b 20MS/S Non-Binary Successive Approximation ADC in 0.13μm CMOS," *Tech. Digest of ISSCC* (Feb. 2002).

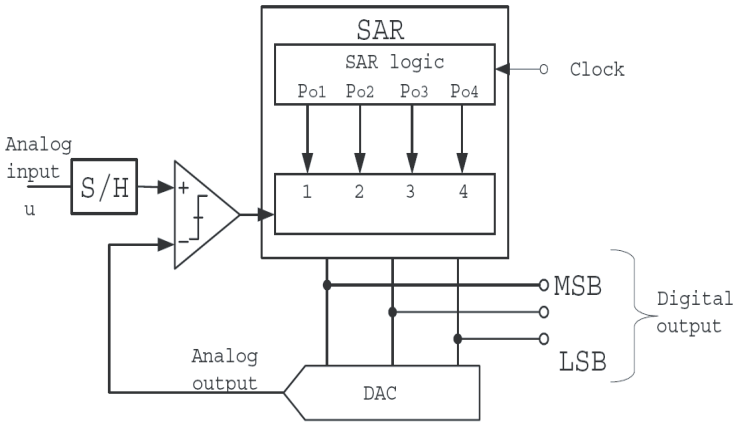

Fig. 1. Block diagram of an SAR ADC.

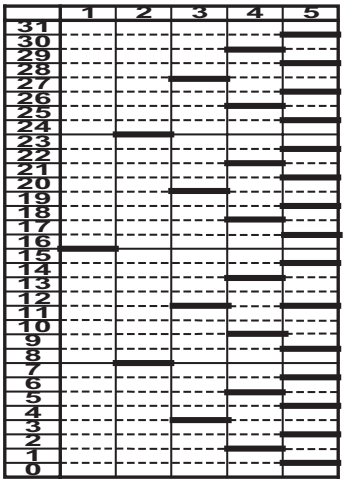

Fig. 2. Binary search algorithm of a 5-bit SAR ADC with 5 steps.

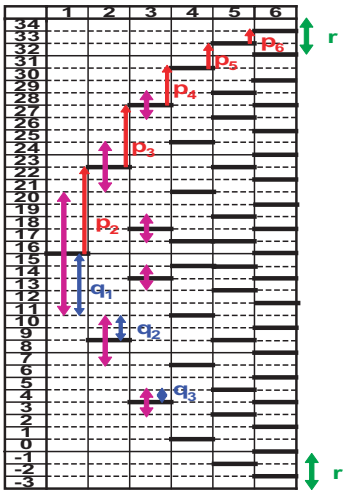

Fig. 3. Redundant search algorithm of a 5-bit SAR ADC with 6 steps (case 1).

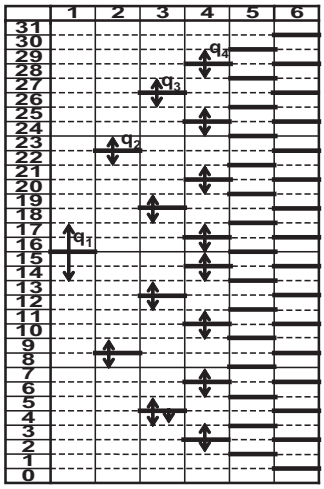

Fig. 4. Redundant search algorithm of a 5-bit SAR ADC with 6 steps (case 2).

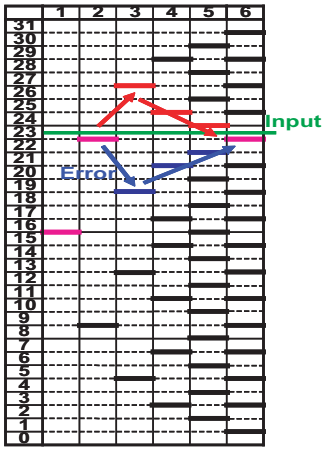

Fig. 5. Operation of the redundant search algorithm of a 5-bit SAR ADC with 6 steps (case 2).

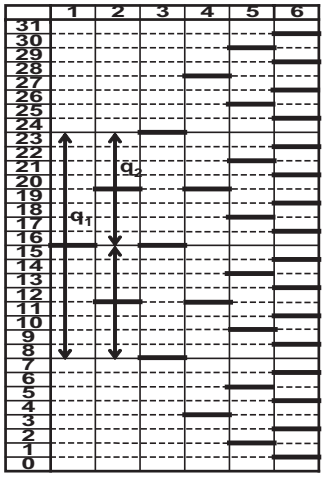

Fig. 6. Redundant search algorithm of a 5-bit SAR ADC with 6 steps (case 3).