High-Resolution DPWM Generator for Digitally Controlled DC-DC Converters

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***Abstract*— This paper describes a new architecture for high-resolution digital PWM (DPWM) generator used in digitally-controlled DC-DC converters, PWM time resolution is determined by the difference between two (or more) gate delays, while that of conventional DPWM circuits is determined by gate delay itself. The proposed DPWM circuit can achieve fine time resolution with small circuits, and has low power consumption. We have also developed a systematic design method for this DPWM circuit based on the extended Euclidean algorithm. A design example that achieves 10ps time resolution for 80ns cycle time (i.e. 13-bit resolution) is shown to demonstrate the effectiveness of the proposed DPWM architecture.**

I. INTRODUCTION

In recent years, demand for power converters that operate in high switching speed, low voltage with high power efficiency has become very high. One of the solutions that fill these difficult demand characteristics is a one-chip fabricated digitally controlled DC-DC power converter. By applying the digital power converter, complicated control algorithms that are difficult to realize in the conventional analog power converter, change of parameter function, malfunction diagnosis and life estimation, communication with peripheral equipment can be easily realized. As results, ripple-reduction and faster response that increase the circuit efficiency, unnecessary circuit change and part addition that increase the custom correspondence performance, low cost and small area circuit realization can be expected. Although digital control power converter has a high cost characteristics compared to analog control power converter, with the low cost of power management ICs and complicated algorithm that only can be realized in digital control power converter, high cost issue is not going to be a problem and it can increase the possibility of additional value creation.

In this paper, high-resolution $DPWM$ (Digital Pulse Width Modulation) generator methods, a key point in the digital power converter, are proposed. The proposed methods have higher resolution compared to the conventional method. In section 2, we describe the proposed high-resolution Digital PWM generator circuit. In sections 3 and 4, we describe the proposed 2-stage buffer configuration fine DTC and design of proposed fine DTC using an extended Euclid algorithm. Finally, conclusions and future works are described in section 5.

II. PROPOSED HIGH-RESOLUTION DIGITAL PWM GENERATOR

A. Target Specification

We show the target specification of this design. As for currently assumed ADC, the sampling frequency is 12.5MHz. The clocks which can be used are $100MHz$ and $12.5MHz$. Thus, 1 cycle is $\frac{1}{12.5MHz} = 80ns$ and the target resolution is 13bit.

$$\frac{80ns}{2^{13}} = \frac{80ns}{8192} = 10ps. \tag{1}$$

Therefore, time resolution is 10 ps. Conventionally, time resolution of digital control IC (UCD9K, 2005) of the U.S. TI company is 150 ps.

B. DPWM Circuit Configuration

The digital PWM circuit configuration used widely is shown in Fig.1. The digital signal of 13 bits is considered as an input and CLK_{out} is the PWM output signal. It consists of Coarse DTC and Fine DTC. The digital input signal of 13 bits is divided into high 3bits and low 10bits, and high bits are input into Coarse DTC and low bits are input into Fine DTC. Coarse DTC consists of a digital counter of 3 bits which operates with a standard clock of 100MHz, and its output CLKin is fed into Fine DTC. A 10-bit timing signal is generated using both analog and digital circuits. DTC stands for Digital-to-Time Converter, where a time output is obtained from a digital input. Unlike the conventional ways where their designs are centering on the voltage, it treats time and it is based on the idea of a time-domain analog circuit design.

13 bits of digital signals are divided into high 3 bits and 10 bits of low ranks, and the form processes by Coarse DTC and Fine DTC are taken respectively.

C. Coarse DTC and Fine DTC Specifications

The specification of Coarse DTC is decided by the ADC sampling frequency of the DPWM generator circuit and standard clock of 100MHz.

$$CLKin = \frac{1}{100MHz} = 10ns \tag{2}$$

Therefore, high bits are decided by the following equation:

$$\frac{\frac{1}{12.5MHz}}{\frac{1}{100MHz}} = \frac{80ns}{10ns} = 8 = 2^3 = 3bit \tag{3}$$

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In Coarse DTC, it is a one-cycle waveform of 80ns that will resolve into 3bits. In Fine DTC, 10-bit becomes PWM resolution and time resolution is 10ps.

D. Configuration and Operation of Coarse DTC

Fig.2 shows a block diagram of Coarse DTC. It consists of a 3-bit digital counter, a digital comparator and a flip-flop for retiming. The digital comparator compares the higher 3-bits of the digital input with the counter output.
The digital counter operates with a standard clock of 100MHz. When the counter output and higher 3-bits digital input are equal, CLKin is set to high from low. The time resolution here is $1/fclk = 10ns$.

E. Conventional Fine DTC

Conventional Fine DTC is shown in Fig.3. The output CLK_{in} from Coarse DTC is considered as its input, and a signal is delayed through the buffer delay line. The delay signal is chosen corresponding to the 10bit digital input to the multiplexer, and it outputs as CLK_{out}. Time resolution here is the buffer delay τ. At the conventional Fine DTC (Fig.3), the buffer delay (gate delay) minimum time resolution τ is dependent on the performance of a CMOS process, therefore, it becomes difficult to make it very small. With this configuration, when low bit digital Din is "2", A_2 is chosen as output CLK_{out}. In order to obtain fine time resolution, it is necessary to make gate delay minimum. Also, in order to realize 10bit resolution, $2^{10} - 1 = 1023$ buffers are needed, and therefore the circuit scale becomes large. Moreover, since amount of [power consumption x gate delay] is fixed, therefore, the power consumption of fine DTC also becomes very large. However, the proposed method can attain smaller time resolution than one gate delay τ. Also the proposed fine DTC can reduce the number of buffers significantly.

III. PROPOSED 2-STAGE BUFFER CONFIGURATION FINE DTC

Fine DTC is newly proposed as the response for the current structure and its problems. Its time resolution is defined not as [gate delay (τ)], but as [the difference between 2 gates delay($\tau_1 - \tau_2$)]. The objective of the proposed method is to achieve fine PWM circuit time resolution with small hardware and power. The proposed Fine DTC circuit uses [the difference between 2 gates delay] and as shown on Fig.4, and signal selecting algorithm of the buffer delay line is formed by decoder circuit part. The decoder circuit part consists of 2 multiplexers. The point in designing the multiplexers is to put cautions on long wired system layout so that the timing skew of each pass inside the multiplexers will not occur. This is required for the proposed Fine DTC to be able to use delay difference in each buffer more accurately.

A. Configuration of the Proposed Fine DTC

Configuration of the proposed Fine DTC is shown in Fig.4. Its characteristics are the addition of another stage in the buffer delay line. Standard clock and DLL (Delay locked loop) based self-delay-amount-control/setting are applied to each gate delay value τ_1, τ_2 of buffer delay line 1, 2. Fine PWM circuit time resolution (compared to the current method) can be achieved by adjusting the parameter of gate delay amount τ_1, τ_2. Path selection is performed by 2 multiplexers according to the lower digital input bits; [the difference between 2 gates delay] is realized. Selection algorithm is determined by the decoder circuit. For example, the buffer circuit here is a bias controlled inverter circuit. The buffer delay line inside DLL is also structured by buffers. When the DLL frequency is locked at a specific value of fclk, the output delay is exactly (1/fckl) compared with the input signal. The buffer delay can be calculated as follow:

$$\tau = \frac{1}{K \cdot f_{clk}} \tag{4}$$

At this moment, bias voltage of the bias controlled inverter will have certain value which satisfies eq.(4) when supplying either buffer delay line 1 or 2.

B. Operation of the Proposed Fine DTC

The proposed Fine DTC uses gate delay τ_1 of the buffer delay line 1 and gate delay τ_2 of the buffer delay line 2. The relation between the 2 parameters is kept as $\tau_1 > \tau_2$, and the buffers are selected so that the overall Fine DTC time resolution satisfies $\Delta\tau(= \tau_1 - \tau_2)$. The selection method and timing chart are shown in Figs.5, 6, 7.

This continuous operation will eventually creates PWM time resolution of $\Delta\tau(= \tau_1 - \tau_2)$. In Fig. 6, if the number of the total buffers in delay line 2 is defined as N (in Fig,5, N=3), then the relation between $\tau 1$, $\tau 2$ is shown as follow:

$$\tau_1 = (N+1)\Delta\tau, \Delta\tau = \tau_1 - \tau_2 \tag{5}$$

$$\tau_2 = \frac{N}{N+1}\tau_1. \tag{6}$$

The overall time resolution can be preserved in high level, even if the delay amount in a single buffer is very large by preparing multistage buffer.

The relation between $\tau 1$, $\tau 2$ can be fixed by DLL and each buffer circuit is controlled by bias control. Furthermore, the relation shown below can be obtained from eq.(4) and eq.(6) by previously defining total buffer number inside $DLL1$ used to create buffer delay $\tau 1$ as $K1$, and total buffer number inside $DLL2$ used to create buffer delay $\tau 2$ as $K2$.

$$\frac{K_1}{K_2} = \frac{N}{N+1}. \tag{7}$$

IV. SYSTEMATIC DESIGN OF FINE DTC USING EXTENDED EUCLID ALGORITHM

We investigate a systematic design method in the proposed Fine DTC section of high-resolution DPWM. The following section describes how this is applied, and how improvements of circuit scale, power consumption, and time-resolution from conventional way are achieved.

A. Application of Extended Euclid Algorithm

x and y are natural numbers (which are not 0), and it is referred to as $l = GCD(x, y)$. At this time,

$$ax + by = l \tag{8}$$

the integers "a" and "b" exist which satisfiy eq.(8). For example, in calculation of GCD (13, 5), the result becomes:

$$2 \times 13 - 5 \times 5 = 1 \tag{9}$$

This technique is called as an extended Euclid algorithm. Here, l=GCD (x, y) expresses the greatest common denominator of x and y. We apply this algorithm to the gate delays τ_1 and τ_2 in the proposed 2-stage buffer configuration fine DTC. Using the measured gate delays and this algorithm, the required total amount of delay can be calculated. When l=1, the amount of delay is 1τ, when l=2 the amount of delay is 2τ. When τ represents the time-resolution, and $x = \frac{\tau_1}{\tau}$,$y = \frac{\tau_2}{\tau}$, using extended Euclid algorithm eq.(8) values of "a" and "b" can be calculated. "a" expresses the number buffers at top-stage, and "b" expresses the number of buffers at bottom-stage. From the standard point which determines "a" and "b" , we can choose both of right and left buffer signal wires. This method enables the proposed 2-stage buffer configuration to constitute the circuit automatically, and design fine DTC with minimum number of buffers using the absolute values of minimum "a" and "b". The minimum solutions of a and b are obtained using a C language program.

B. Design of 2-stage Buffer Configuration Fine DTC

We apply the extended Euclid algorithm to design the proposed Fine DTC for small circuit area, and relatively large gate delay $\tau 1$ and $\tau 2$. Since the target resolution specification of this Fine DTC design is 10bit, l in eq.(8) is set to l= 0-1023. Here we set $\tau 1/\tau 2 = 1.8$ as an optimal value obtained from simulation.

V. DESIGN RESULT OF PROPOSED FINE DTC

A. Design of 2-stage Buffer Fine DTC

By using the extended Euclid algorithm, the proposed Fine DTC reduces the number of buffers from 93 to 82,and also it reduces power consumption from 540mW to 216mW. Furthermore it changes amount of gate delay from 10ps to 160ps and 290ps. Small scale design, reduction of amount of gate delays on a buffer, and high precision resolution characteristics are possible to realize using the proposed Fine DTC architecture.

B. Design Result of Whole DPWM Generator

We consider a Fine DTC with multi-stage configuration of buffers. As a result, comparing 2-stage, 3-stage and 4-stage, and taking account of the increase of DLL and MUX, we found that the 3-stage buffer configuration is the most efficient. The design result of the whole DPWM generator circuit is shown in Fig.9. In 10ps time-resolution, comparing 3-stage to 2-stage buffer configuration, the number of buffers is reduced from 82 to 37. Applying the extended Euclid algorithm, when designing a DTC, can provide a possible optimal parameter program extraction method. It is a very effective method to the design of DPWM generating circuit.

VI. CONCLUSIONS AND FUTURE WORK

A fine time resolution PWM generator for digitally controlled power converter is proposed. From the time resolution which is decided by "gate delay" in the conventional way, time-resolution which is decided by "difference of two or more gate delay" new method was devised. Therefore, the semiconductor process dependability of time resolution becomes less compared to the conventional way. Improvements of resolution, circuit scale, and power consumption were verified with a design example.We would like thank K. Wilkinson for valuable discussions.

REFERENCES

[1] K. Wang, et.al, "All Digital DPWM/DPFM Controller for Low Power DC-DC Converters," IEEE Applied Power Electronics Conference and Exposition (APEC), Dallas, TX (Mar. 2006).
[2] J. Chen, et.al., "DPWM Time Resolution Requirements for Digitally Controlled DC-DC Converters," IEEE APEC, Dallas, TX (Mar 2006).
[3] K. Leung, et.al., "Design and Implementation of a Practical Digital PWM Controller", IEEE APEC, Dallas, TX (Mar. 2006).
[4] T. Komuro, J. Rivoir, K. Simizu, M. Kono, H. Kobayashi, "ADC Architecture Using Time-to-Digital Converter", IEICE Wabun-C vol. J90-C, no.2, pp.125-133 (Feb 2007).
[5] K. Simizu, A. Motozawa, K. Lin, T. Komuro, H. Kobayashi, "Nonuniform-Sampling ADC Using Time-to-Digital Converter and its Signal Processing", IEICE the 19th Circuit and System (Karuizawa)Workshop(April 2006).
[6] M. Kono, K. Kimura, I. Mori, Y. Yamada, H. Kobayashi, Y. Kobori, K. Shimizu, K. San, High-Resolution DPWM Generator for Digitally Controlled DC-DC Converters, IEICE Vol.J91-C, no.8, pp.418-427 (Aug. 2008).

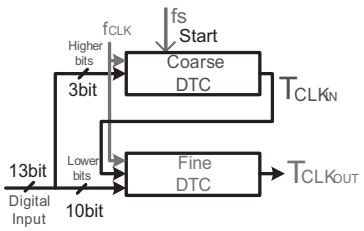

Fig. 1. Block daigram of the whole DPWM circuit.

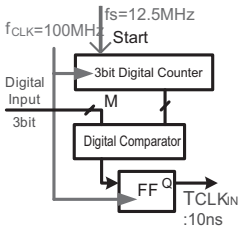

Fig. 2. Coarse DTC configuration.

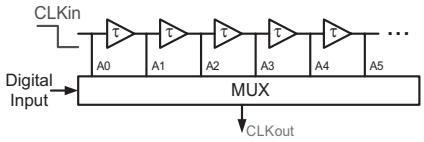

Fig. 3. Conventional fine DTC circuit. When digital input D_{in} is 2, then $A2$ is selected as the output signal CLK_{out}.

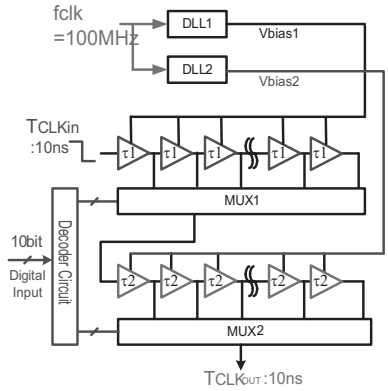

Fig. 4. Proposed two-delay-line fine DTC circuit.

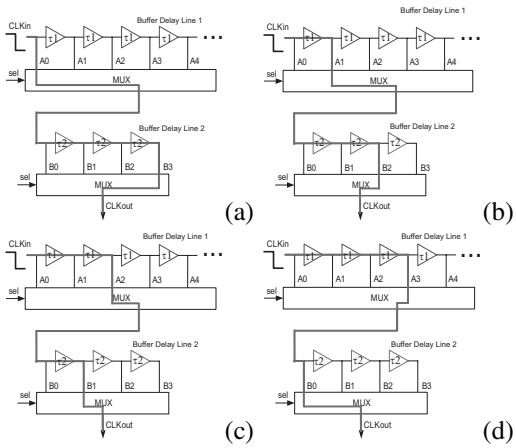

Fig. 5. Operation of the proposed two-delay-line fine DTC.

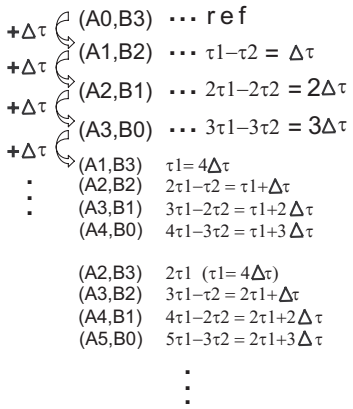

Fig. 6. Algorithm of the proposed two-delay-line fine DTC.

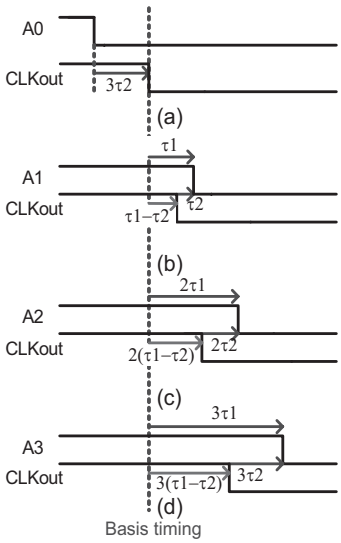

Fig. 7. Timing chart of the proposed two-delay-line fine DTC.

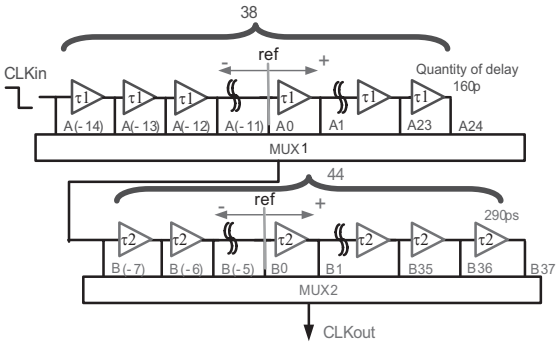

Fig. 8. Two-delay-line fine DTC which is designed using the extended Euclidean algorithm.

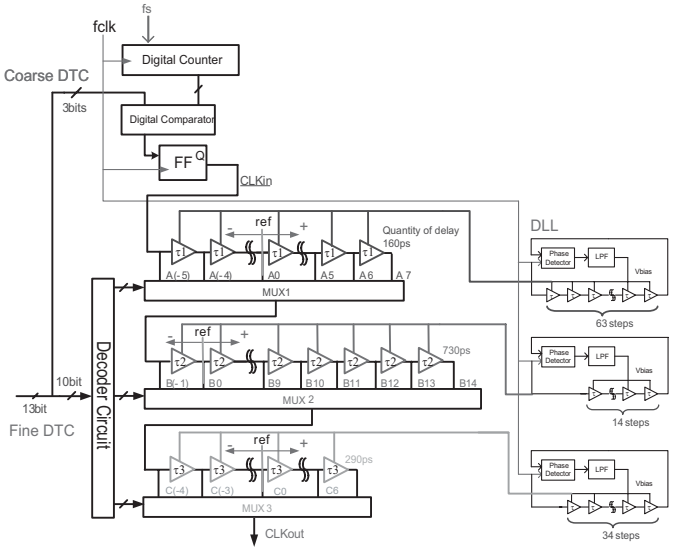

Fig. 9. Proposed DPWM generator with three-delay-line fine DTC.