$\Delta\Sigma$AD Modulator for Low Power Application

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***Abstract*— This paper proposes a new architecture of the feedforward multibit $\Delta\Sigma$AD modulator for low power application. The SQNDR (Signal to Quantization Noise and Distortion Ratio) of $\Delta\Sigma$AD modulator is limited by the dynamic range of the input signal and non-idealities of circuit building blocks, particularly by the harmonic distortion in amplifier circuits. In a full feedforward $\Delta\Sigma$AD modulator structure, the signal swings through the loop filter is smaller than a feedback $\Delta\Sigma$AD modulator. Therefore, the harmonic distortion generated inside the loop filter of the feedforward structure can be significantly reduced because the effect of non-idealities in amplifiers can be suppressed when signal swing is small. However, in conventional feedforward $\Delta\Sigma$AD modulator, an analog adder is needed before the quantizer, and especially in a multibit modulator, an additional amplifier is necessary to realize the summation of feedforward signals, which leads to extra chip area and power dissipation. In this paper, firstly, we propose a new architecture of a feedforward $\Delta\Sigma$AD modulator which realizes the summation of feedforward signals without additional amplifier. The proposed architecture is functionally equivalent to the conventional one but with smaller chip area and lower power dissipation. Furthermore, we extend the architecture with noise-shaping enhancement, the modulator contains a second-order loop filter can deliver a third-order noise-shaping. We conducted MATLAB simulations to validate the proposed architecture.**

I. Introduction

As an interface between the analog world and the digital domain, the Analog-to-Digital Converter (ADC) is widely used in mixed-signal circuits. However, in nano-meter CMOS technology, the device characteristics degradation (such as matching, r_{ds}) and the low supply voltage evidently reduce the accuracy of ADC. $\Delta\Sigma$AD modulators realize high resolution by oversampling and noise-shaping techniques, which are suitable for high resolution application in the nano-meter CMOS technology. The performance of $\Delta\Sigma$AD modulators is limited by dynamic range of input signal and non-idealities of circuit building blocks. In nano-meter CMOS technology, the performance of analog circuits is significantly degraded and non-idealities of circuit building blocks, especially non-linearities of amplifiers generate more harmonic distortion. Furthermore, since allowable signal swings are reduced due to lower supply voltage, the dynamic range will be decreased and the performance of the modulator would be degraded. In this paper, we propose a new feedforward architecture of the $\Delta\Sigma$AD modulator with noise-shaping enhancement. The order of the modulator will be effectively raised. just by adding some passive capacitors and switches, the additional active circuits are not necessary. Therefore, it can achieve higher SQNDR with low power dissipation.

II. Feedback & feedforward $\Delta\Sigma$AD modulators

Fig.1 shows a second-order feedback $\Delta\Sigma$AD modulator and Fig.2 shows a second-order feedforward $\Delta\Sigma$AD modulator. They have similar structure with two integrators, one ADC and one or two DACs, but their signal paths are different.

- **Feedback $\Delta\Sigma$AD modulator**

The feedback structure shown in Fig.1 is a commonly used in a $\Delta\Sigma$AD modulator, and its transfer function can be expressed as

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2 E(z). \quad (1)$$

Here X(z) is the input signal, Y(z) is the output signal and E(z) is the quantization noise of the modulator. The signal transfer function (STF) and noise transfer function (NTF) are given by

$$STF(z) = z^{-2} \quad (2)$$
$$NTF(z) = (1-z^{-1})^2. \quad (3)$$

NTF provides a second-order noise-shaping function for the quantization noise E(z). The output signals of the first and second integrators (y_1 and y_2) are given as follows:

$$y_1 = z^{-1}(1+z^{-1})X(z) - z^{-1}(1-z^{-1})E(z) \quad (4)$$
$$y_2 = z^{-2}X(z) - z^{-1}(2-z^{-1})E(z). \quad (5)$$

From Eqs.(4) and (5), we see that output signals of two integrators (y_1 and y_2) are the functions of the input signal $X(z)$. Then the signal swings at the amplifier outputs become large which creates complexity for their implementation with the low supply voltage. The harmonics generated by the amplifier non-linearities also depends on the signal swing of integrator, which would reduce SQNDR of the modulator.

- **Feedforward $\Delta\Sigma$AD modulator**

The transfer function of the feedforward $\Delta\Sigma$AD modulator shown in Fig.2 can be expressed as

$$Y(z) = X(z) + (1-z^{-1})^2 E(z) \quad (6)$$
$$STF(z) = 1 \quad (7)$$
$$NTF(z) = (1-z^{-1})^2. \quad (8)$$

Compared with feedback $\Delta\Sigma$AD modulator (Fig.1), NTF given by Eq.(8) is the same as Eq.(3). However note that STF is unity and not delayed under ideal circumstances. The output signals of the first and second integrators (y_1 and y_2) are given

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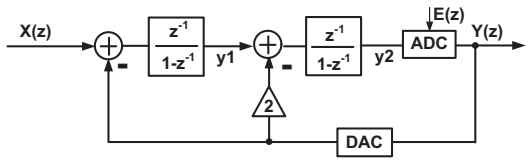

Fig. 1. Second-order feedback ΔΣAD modulator.

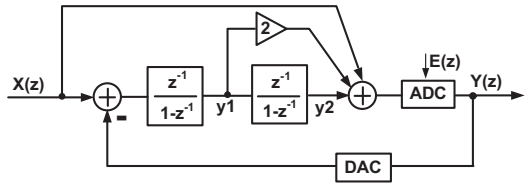

Fig. 2. Conventional second-order feedforward ΔΣAD modulator.

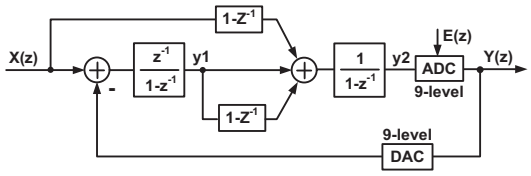

Fig. 3. Opamp shared second-order feedforward ΔΣAD modulator.

as follows:

$$y_1 = -z^{-1}(1-z^{-1})E(z) \quad (9)$$

$$y_2 = -z^{-2}E(z). \quad (10)$$

From Eqs.(9) and (10), we can see that the y_1 and y_2 are free of the input signal $X(z)$, which means that the first and second integrators of the feedforward ΔΣAD modulator processes quantization error only [1]. Therefore, the signal swings passing through the integrators are smaller and the distortion generated by the amplifiers would be input-signal-independent and reduced. Furthermore, in this topology, the signal amplitudes of the amplifiers are reduced which eases implementation of amplifier design with low power supply.

III. Opamp Shared Feedforward ΔΣAD modulator

Note the summation point of feedforward paths in the front of the quantizer in Fig.2, an analog adder circuit is necessary to realize all the feedforward signals summed together. In a multibit implementation of the full feedforward ΔΣAD modulators, the switched-capacitor adder has to be used and a weighted summation amplifier is required before the quantizer [2], that leads to extra chip area and power dissipation. Some ideas have been proposed to solve this problem in [3],[4]. However, they require a distributed DAC-feedback or a high-order(≥third-order) loop filter which would increase complexity of modulator circuits.

We have proposed an opamp shared architecture of feedforward ΔΣAD modulator [5]. It is a single DAC-feedback, second-order ΔΣAD modulator without an additional amplifier and its circuit implementation with low supply voltage would be simple. Fig.3 shows the simplified structure of proposed feedforward ΔΣAD modulator in 3-bit ADC and DAC case, and it has the following features:

- **One-amplifier saving**

In the proposed architecture, we moved the summation point of feedforward path from input node of the quantizer to the input node of the second-stage loop filter. (See the conventional modulator in Fig.2 for comparison.) The feedforward signals are merged into the output of the first-stage integrator, and then are fed to the second stage. By this way, the amplifier in the second stage can be shared to realize signal summation and integration. As such, circuit complexity is reduced by not requiring an additional weighted summation amplifier before the quantizer. In the modulator implementation of [2], the summation amplifier in the front of the quantizer consumes 8% of total power, and we estimate that this amount of power reduction would be possible in the modulator topology of [2] with our proposed amplifier-saving technique.

- **Lower-order loop filter and multibit architecture**

Higher SQNDR can be realized by a higher-order modulator which, however, needs more hardware and consumes more power. A second-order loop filter can be implemented simply rather than a high-order one, which reduces analog circuit complexity and power dissipation. Multibit quantizer not only reduces quantization noise, but also relaxes the required slew rate of input amplifier of the filter. Therefore, the modulator becomes more linear, its stability is improved and power dissipation is lower [6].

- **Single DAC-feedback and single-loop topology**

Furthermore, with a single DAC-feedback and a single-loop topology, (rather than a distributed DAC-feedback or a cascaded architecture [6]), requirements for analog circuit and DAC linearization in the modulator are reduced, because the modulator circuits can be much insensitive to the finite DC gains of the amplifiers. Normally DAC circuits are realized by switched-capacitor circuits, and simple DAC implementation can reduce the power dissipation for charge and discharge of capacitors, which are more suitable for low-power dissipation.

The input and output transfer function of the proposed modulator are the same as the conventional feedforward ΔΣAD modulator, but the output signal of the second integrator contains a input signal component. However, non-idealities of the second integrator can be noise-shaped by the feedback loop in the modulator, and their effects are not dominant for the second order modulator. It should also be noted that the $(1-z^{-1})$ term in the feedforward path of the proposed modulator can be implemented just by a simple capacitor.

We have made the performance comparison of feedback ΔΣAD modulator with our proposed ΔΣAD modulator, including a finite gain amplifier model and a nonlinear amplifier model with harmonic distortion. We assumed that all amplifiers in the modulators have DC gain of 40dB and third-order distortion corresponding to 1% for a full scale signal.

Fig.4 shows the output spectrum of a feedback ΔΣAD modulator in Fig.1 including a finite gain and a nonlinear amplifier model. We observe that the gain non-linearities of amplifiers cause large harmonic distortion and it appears at the output of the feedback ΔΣAD modulator. When this modulator samples a sinusoidal input signal of F_{in}=1.94kHz

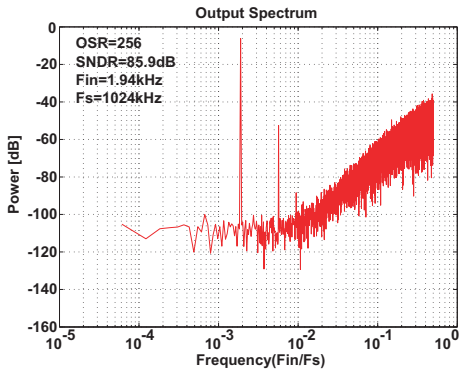

Fig. 4. Simulated output power spectrum of the second-order feedback ΔΣAD modulator in Fig.1 with harmonic distortions.

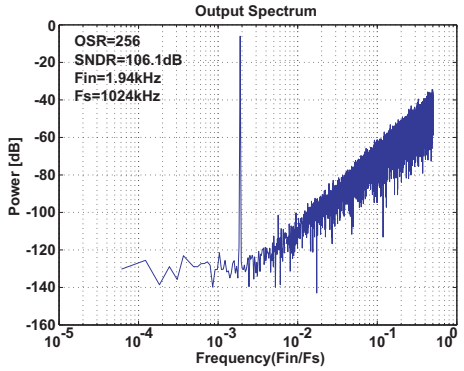

Fig. 5. Simulated output power spectrum of the opamp shared second-order feedforward ΔΣAD modulator in Fig.3 with harmonic distortions.

at F_s=1024kHz sampling rate, its SQNDR reaches 85.9dB in case of OSR=256. Fig.5 shows the output spectrum of the opamp shared feedforward ΔΣAD modulator in Fig.3. It includes a finite gain and nonlinear amplifier models that are the same as feedback modulator ones. The same nonlinear gain coefficients are used as the case of Fig.4, however, in the feedforward modulator the harmonic distortion is suppressed, and the SQNDR can reach 106.1dB in the case of OSR=256 with the same input signal frequency and sampling rate. From the above discussion we can see that the proposed modulator can realize equivalent noise-shaping function to the conventional one and is less sensitive to non-idealities of amplifier.

IV. Opamp Shared Feedforward ΔΣAD Modulator with Noise-shaping Enhancement

Fig.6 shows a ΔΣAD modulator with self-coupled noise injection [7], which is a full feedforward ΔΣAD modulator with an additional error-feedback structure of quantization noise. Notice the additional self-coupled noise injection structure surrounded by the dotted line, the quantization noise $E(z)$ is obtained by subtracting the internal ADC's input from the DAC output. After through a filter z^{-1}, the delayed replica of quantization error $E(z)$ is fed back into the input node of ADC again. It is similar to an error-feedback structure in ΔΣ modulator [6]. While the noise transfer function of conventional ΔΣAD modulator is NTF(z), the transfer function of ΔΣAD modulator with self-coupled noise injection shown in Fig.6 can be written as following:

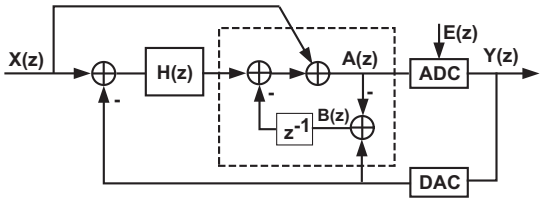

Fig. 6. Noise-shaping enhancement architecture of ΔΣAD modulator.

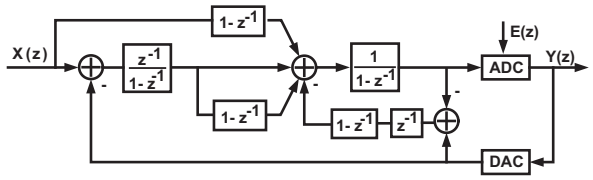

Fig. 7. Proposed ΔΣAD modulator with noise-shaping enhancement.

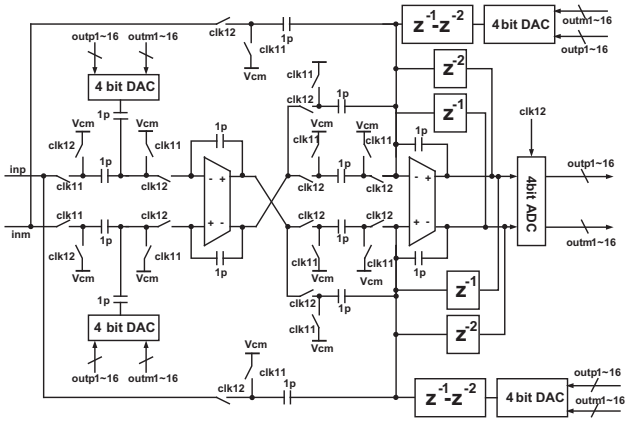

Fig. 8. Switched-capacitor implementation of the proposed modulator.

$$\begin{aligned} Y(z) &= X(z) + NTF'(z)E(z) \\ NTF'(z) &= NTF(z)(1 - z^{-1}) \end{aligned} \quad (11)$$

As shown in Eq.(11), the $NTF'(z)$ of ΔΣAD modulator increments the NTF(z) by an extra $(1 - z^{-1})$ factor, the order of the modulator is increased by one, which is equivalent to obtaining more noise shaping in low frequency signal band, and achieving higher SQNDR of modulator.

We propose an extended ΔΣAD modulator architecture with noise-shaping enhancement shown in Fig.7. Compared with the ΔΣAD modulator shown in Fig.6, we moved the summation point for feedforward and noise injection paths from input node of the quantizer to the input node of the second-stage integrator, which is similar to the ΔΣAD modulator shown in Fig.3 with an additional self-coupled noise injection structure. The input and output of extended ΔΣAD modulator architecture can be expressed as

$$Y(z) = X(z) + (1 - z^{-1})^2(1 - z^{-1})E(z) \quad (12)$$

$$= X(z) + (1 - z^{-1})^3 E(z) \quad (13)$$

From Eqs.(12) and (13), we can see that the noise-shaping of the proposed modulator is enhanced to third-order only use two integrators. Therefore, proposed modulator is an equivalent structure to the modulator shown in Fig.6.

Figure 8 shows the fully differential switched-capacitor circuit implementation of the proposed ΔΣAD modulator. Parasitic-insensitive switched-capacitors structures are used for integrators. Negative capacitors in the modulator are easily implemented by changing the polarity of input signals in the fully differential circuit. Feedforward signals and injected quantization noise are summed at input node of the second stage integrator, and no more additional summation amplifier is necessary. The coefficients in Fig.7 are realized by the ratios of capacitors around the amplifiers. In our proposed modulator, all coefficients are 1 which is easily implemented with the same capacitor size.

V. Simulation Results and Conclusion

We have conducted MATLAB simulations to evaluate the effectiveness of the proposed ΔΣAD modulator with noise-shaping enhancement architecture. We made comparison of behavioral models which are shown in Fig.2, Fig.3 and Fig.7. In the behavioral model of Fig.2, a conventional feedforward ΔΣAD modulator is used; in the behavioral model of Fig.3, opamp shared feedforward ΔΣAD modulator is used; and in the behavioral model of the proposed modulator shown in Fig.7, we just add the noise-shaping enhancement structure to Fig.3. Fig.9 shows simulation result comparison of output power spectrum for behavioral models of of above modulators. Around the input signal band of low frequency, the signal power of the proposed modulator is the same as others, but the noise floor is lower than the others architecture, which means that the noise power can be suppressed well in the proposed modulator. Fig.10 shows simulation result comparison of SQNDR vs OSR which are calculated from above of their output power spectrum of the behavioral models. For the conventional feedforward modulator and opamp shared modulator, the SQNDR increases by 15dB/Oct while OSR is increased, which shows second-order characteristic of ΔΣAD modulator. On the other hand, for the proposed noise-shaping enhancement ΔΣAD modulator with self-coupled noise injection architecture shown in Fig.7, the SQNDR increases by 21dB/Oct while OSR is increased, which shows third-order characteristic of ΔΣAD modulator. It suggests that the proposed modulator realizes high order of noise shaping by noise-coupled architecture, it can effectively raise the order of the modulator, and suppress the noise power of interest band. Therefore, the SQNDR of the proposed ΔΣAD modulator can be higher than the conventional structures.

As a result, by the techniques of quantization noise injection and amplifier-saving, the proposed modulator provides a higher-order NTF using a lower-order loop filter, the additional integrator circuit which consists of an operational amplifier is not necessary, and the performance of the ΔΣAD modulator can be effectively raised without more power dissipation. The MATLAB simulation results with behavioral model show that

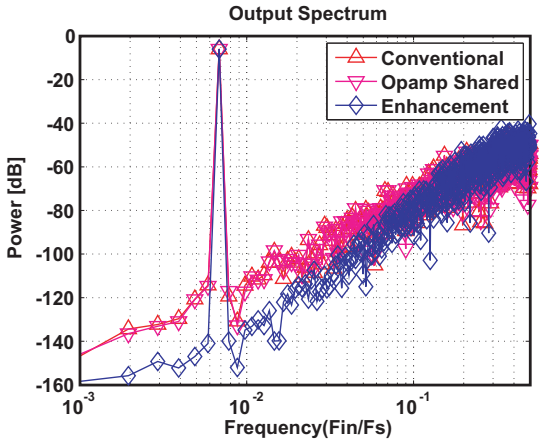

Fig. 9. Simulattion results comparison of output power spectrum

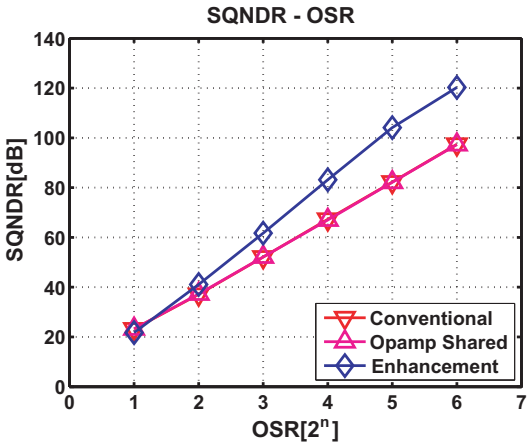

Fig. 10. Simulation results comparison of SQNDR-OSR.

the proposed architecture can effectively raise the order of the modulator, and improve the SQNDR of a ΔΣAD modulator.

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