Non-Uniform Sampling A/D Converter Using Time-to-Digital Converter
And Its Signal Processing

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I. Introduction

In a deep-submicron CMOS process,
○ Time-domain resolution of a digital signal edge transition
× Voltage resolution of an analog signal
□ - Analog part ⇒ minimum
□ - Mostly digital circuits

This ADC is suitable for implementation with fine-line-width semiconductor

II. Proposed A/D Converter Architecture

Fig. 2 Proposed A/D Converter.

• The reference cosine wave generator circuit
  ⇒ delta-sigma D/A modulation

• The unclocked comparator
  ⇒ simple low-voltage supply circuit.

Fig. 3 Time-to-Digital Converter.

• TDC ⇒ The resolution of several picoseconds order

TDC measures the time from the rising edge of the reference clock CLK to the time when the comparator output toggles.

Reference cosine: \( y(t) = \cos(2\pi ft) \)

TDC output: \( t_{ADC} = T \tan^{-1}(\frac{y_{ref}}{2V_{ref}}) \)

ADC output digital value: \( D_{ADC} = \frac{t_{ADC}}{2} \times \frac{V_{ref}}{T} \)

⇒ Non-uniform sampling

III. Signal Processing (Non-uniform Sampling Data)

Fig. 6 Uniform Sampling A/D Converter.

• The circuit composition in an analog part is simpler and achievement is easier than the subranging ADC.

⇒ Uniform sampling (by using the T/H circuit)

Fig. 7 Non-Uniform Sampling A/D Converter.

• The TDC measures the time from the rising edge of the reference clock CLK to the time when the comparator output toggles.

⇒ Non-uniform sampling

IV. Summary

• Automatic Test Equipment (ATE)
  • Power spectrum
  • Minimum calculation time.

□ The reference cosine wave generation circuit ⇒ delta-sigma D/A modulation (which is mostly digital)
□ The unclocked comparator circuit ⇔ simple analog filter.
□ The TDC circuits
  • Vernier delay Line TDC (high time resolution)

The power of the Spurious element can be dropped by interpolating the non-uniform sampling data.

However, a further examination of a high-speed, highly accurate signal processing of the non-uniform sampling data is necessary.