Non-Uniform Sampling A/D Converter Using Time-to-Digital Converter And Its Signal Processing

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I. Introduction

New A/D Converter Architecture

Voltage domain ⇒ Time domain

In a deep-submicron CMOS process,

- ○ Time-domain resolution of a digital signal edge transition
- × Voltage resolution of an analog signal

⇒ ・**Analog part ⇒ minimum**
・**Mostly digital circuits**

This ADC is suitable for implementation with fine-line-width semiconductor process.

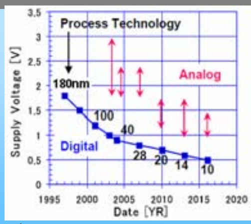


Fig.1 Trend of process technology and supply voltage.

II. Proposed A/D Converter Architecture

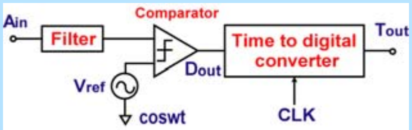


Fig.2 Proposed A/D Converter.

・The reference cosine wave generator circuit
⇒ delta-sigma D/A modulator

・The unclocked comparator
⇒ simple low-voltage supply circuit.

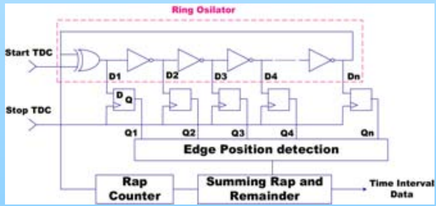
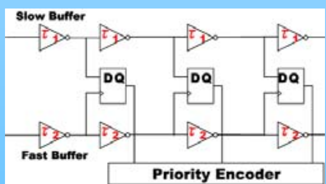


Fig.3 Time-to-Digital Converter.

・TDC ⇒ The resolution of several pico second order



・$\tau 1 > \tau 2$
⇓
Time Resolution $\Delta\tau = \tau 1 - \tau 2$

Fig.4 Vernier Delay Line Time-to-Digital Converter.

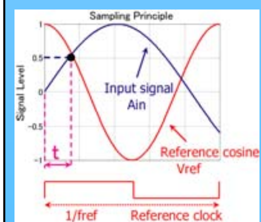


Fig.5 Operation of Proposed ADC.

TDC measures the time from the rising edge of the reference clock CLK to the time when the comparator output toggles.

Reference cosine: $V_{ref}(t) = A\cos\left(2\pi\frac{t}{T}\right)$

TDC output: $t_n = T\arccos\left(\frac{A_{in}(t_n)}{A}\right)$

TDC output digital value: $T_{out}(n)$

ADC output: $D_{out}(n) = A\cos\left(2\pi\frac{T_{out}(n)}{T}\right)$

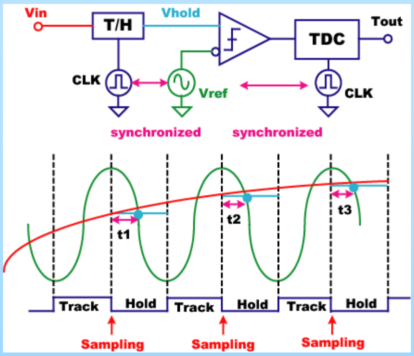


Fig.6 Uniform Sampling A/D Converter.

・The circuit composition in an analog part is simpler and achievement is easier than the subranging ADC.

⇒ Uniform sampling (by using the T/H circuit)

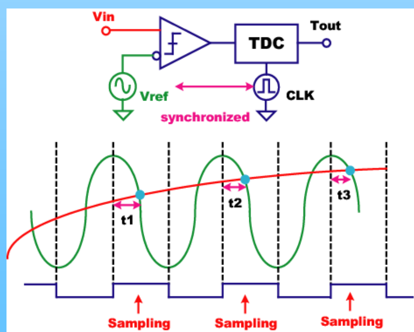


Fig.7 Non-Uniform Sampling A/D Converter.

・The TDC measures the time from the rising edge of the reference clock *CLK* to the time when the comparator output toggles.

⇓

・The amplitude of the input signal at that timing can be calculated from the measured time *Tout*(*n*).

⇒ Non-uniform sampling

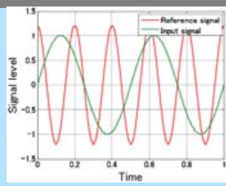


Fig.8.Input signal and reference signal

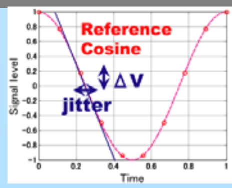


Fig.9.TDC's Jiiter

Vin/Vref=1.0/1.2

Reference cosine

$y = 1.2\cos(2\pi \cdot fs \cdot t)$

Gradient

$y' = -1.2 \cdot 2\pi \cdot fs \cdot \sin(2\pi \cdot fs \cdot t)$

Gradient_Max

$y'_{max} = 1.2 \cdot 2\pi \cdot fs$

$\Delta V_{max} = y'_{max} \cdot \text{jitter}\ [V_{rms}]$

$V_{input} = 2V_{pp} / \sqrt{2} / 2 = 0.707\ [V_{rms}]$

$SNR = 20\log_{10}\left(\frac{V_{input}}{\Delta V_{max}}\right)$ [dB]

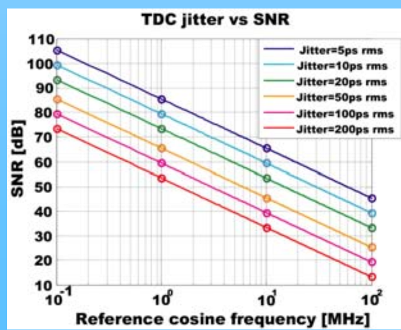


Fig.6 TDC Jitter vs SNR.

III. Signal Processing (Non-uniform Sampling Data)

■ Automatic Test Equipment (ATE)

・Power spectrum

・Minimum calculation time.

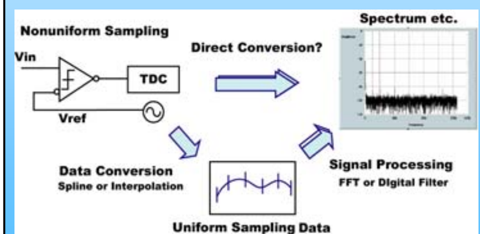
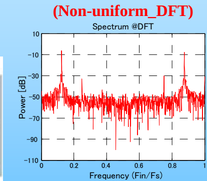


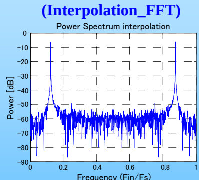
Fig.8 Signal processing.

Power Spectrum (Non-uniform_DFT)



-32.8[dB] @ fin/fs=0.248

Power Spectrum (Interpolation_FFT)



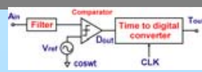
-49.04[dB] @ fin/fs=0.248

Spurious

The power of the Spurious element can be dropped by interpolating the non-uniform sampling data.

However, a further examination of a high-speed, highly accurate signal processing of the non-uniform sampling data is necessary.

IV. Summary



・**We proposed new ADC architecture.**

⇒ ADC handles the signal in time domain.

→ Mostly digital circuits
→ analog part is minimum.

☐ The reference cosine wave generation circuit
・delta-sigma D/A modulator (which is mostly digital)
・simple analog filter.

☐ The *unclocked* comparator circuit
・simple circuit (such as an differential amplifier)

☐ The TDC circuits
・Vernier delay Line TDC (high time resolution)

The measurement of the signal of DC, the audio band, and the video band is possible with one circuit (proposed ADC).