ASP-DAC 2009 University LSI Design Contest 1D-10

A Time-to-Digital Converter with Small Circuitry

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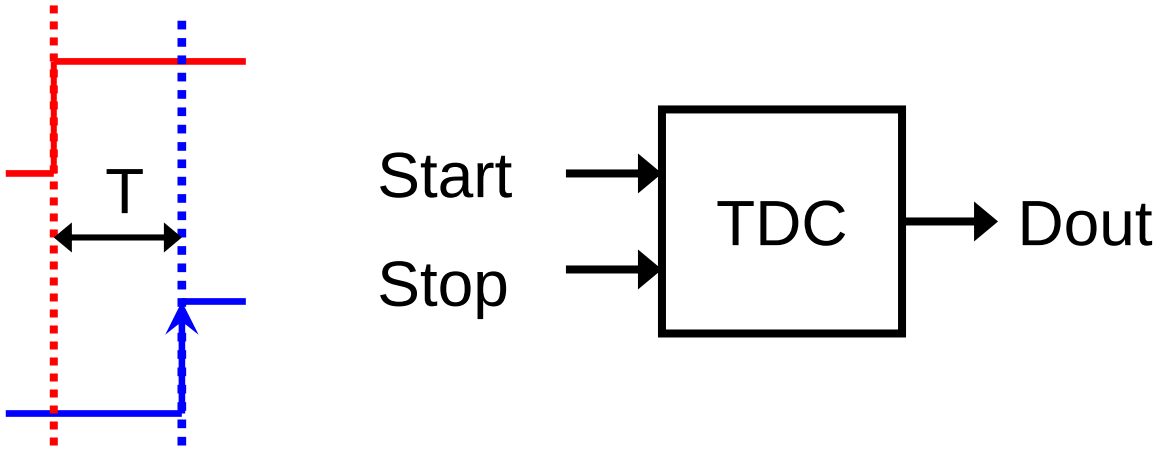
Research Goal

Development of new architecture
for a time-to-digital converter
with

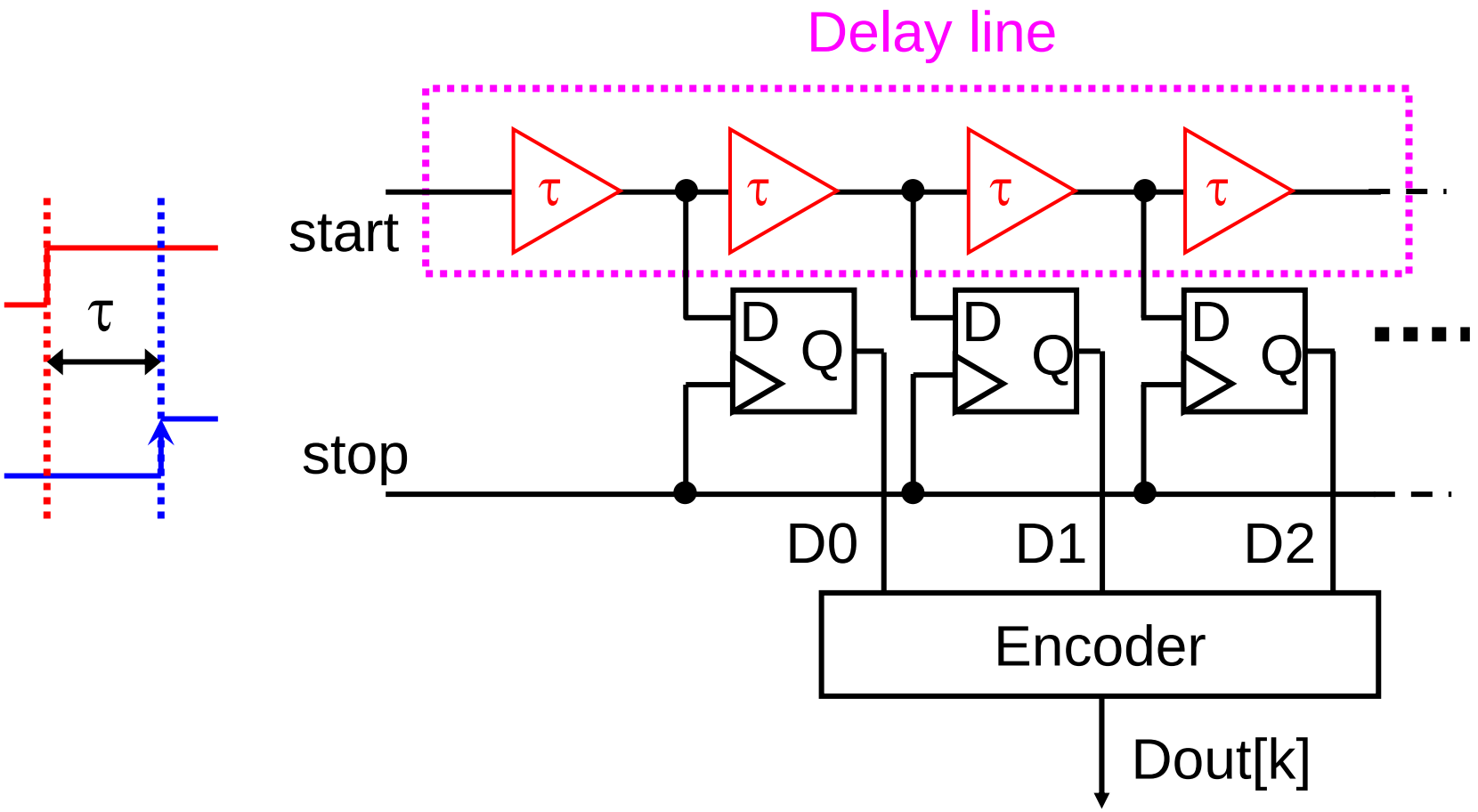
- fine time resolution
- high linearity
- small circuitry
- low power.

TDC (Time-to-Digital-Converter)

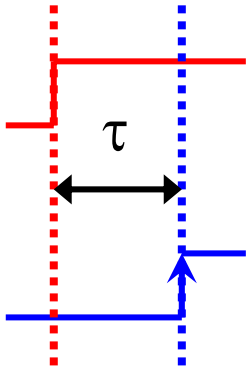
- Time interval measurement → Digital output

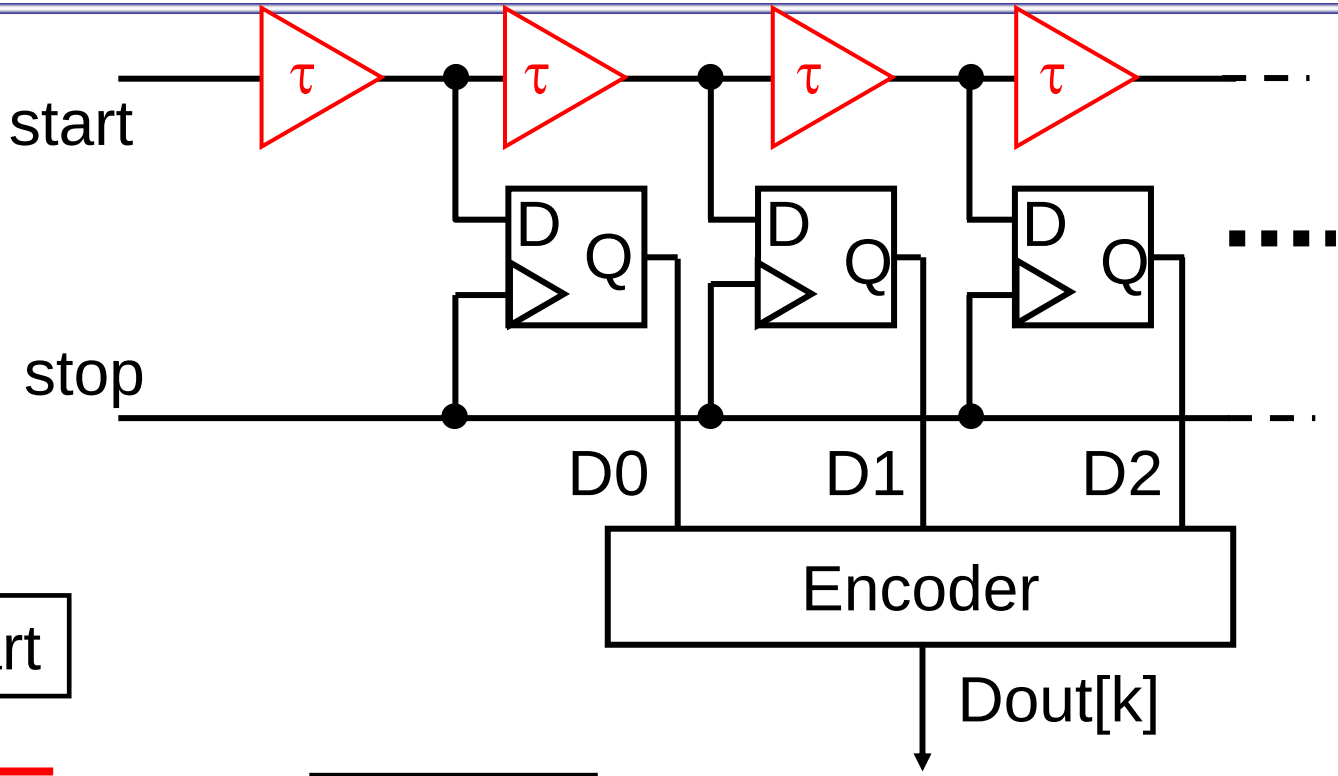


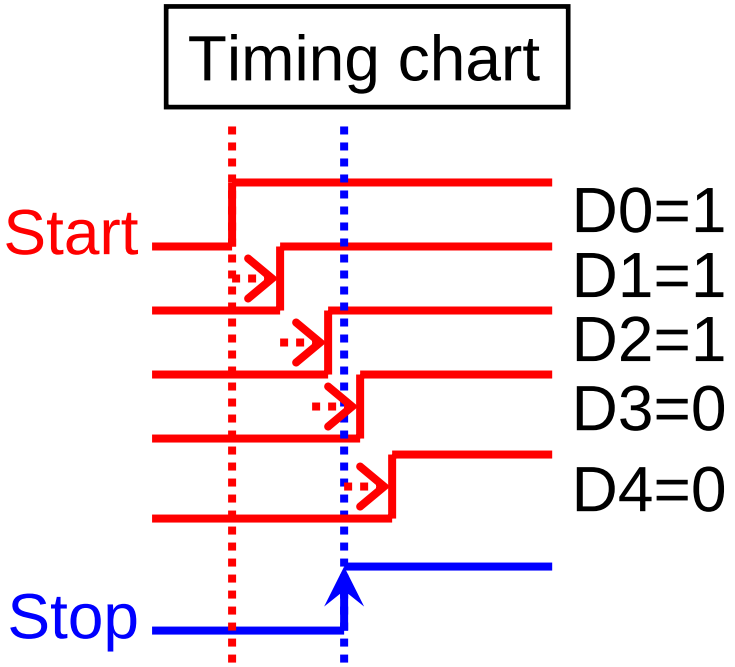
Structure of Basic TDC



Operation of Basic TDC







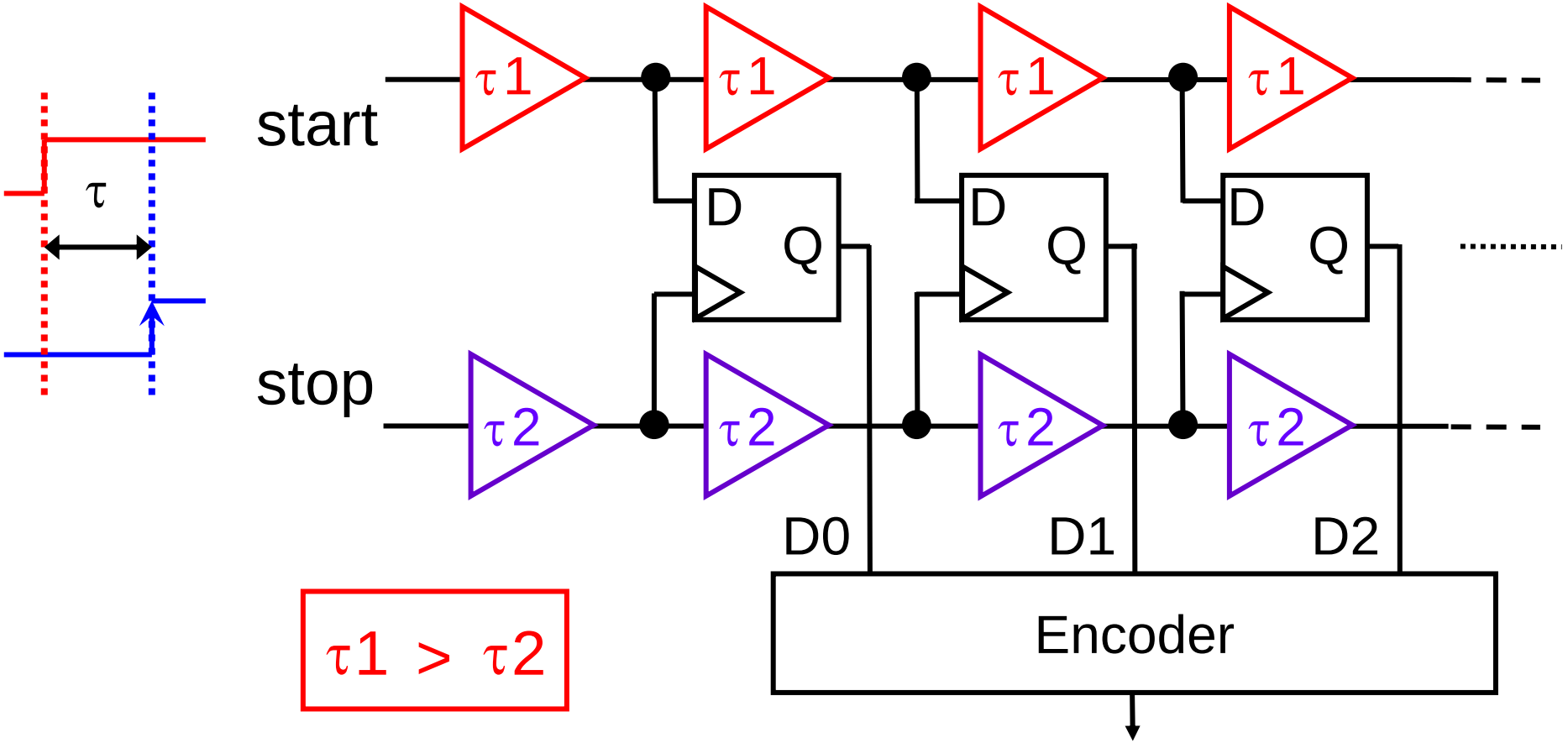
Encoder

Thermometer code → binary code

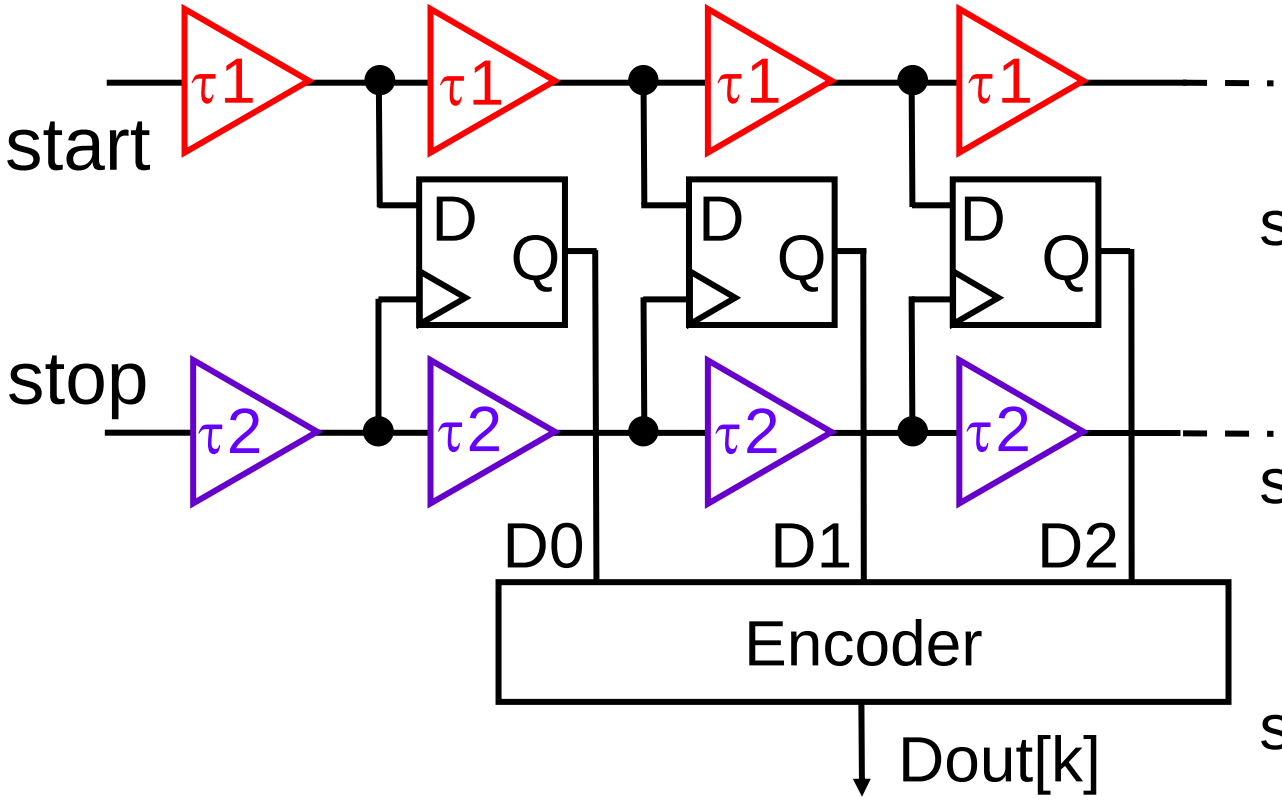
1LSB = tau1

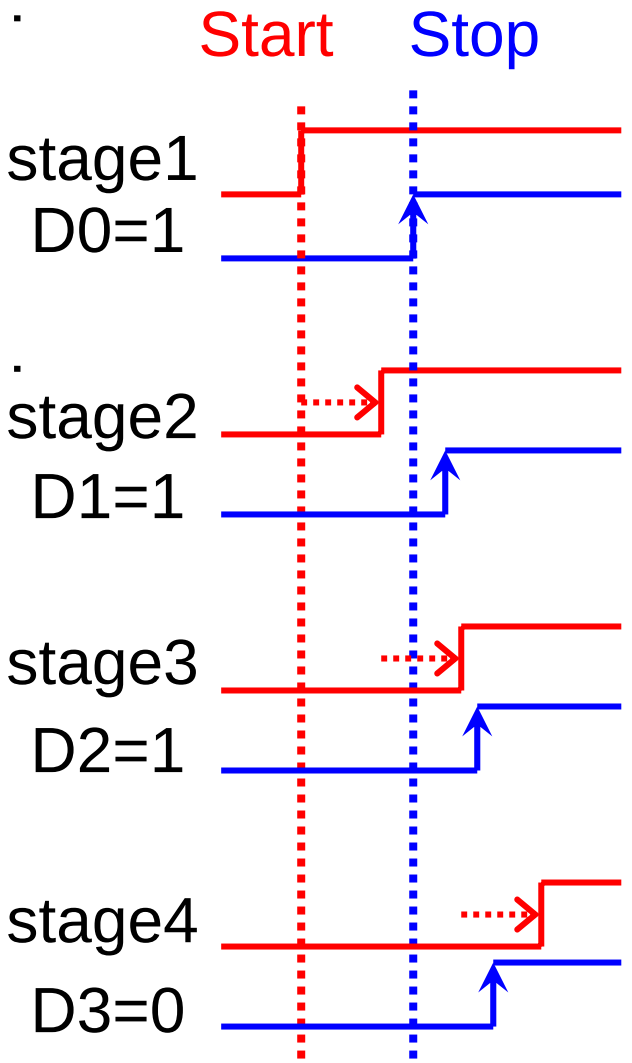
(Minimum value depends on CMOS process rule)

Structure of Vernia Delay Line TDC



Operation of Vernia Delay Line TDC



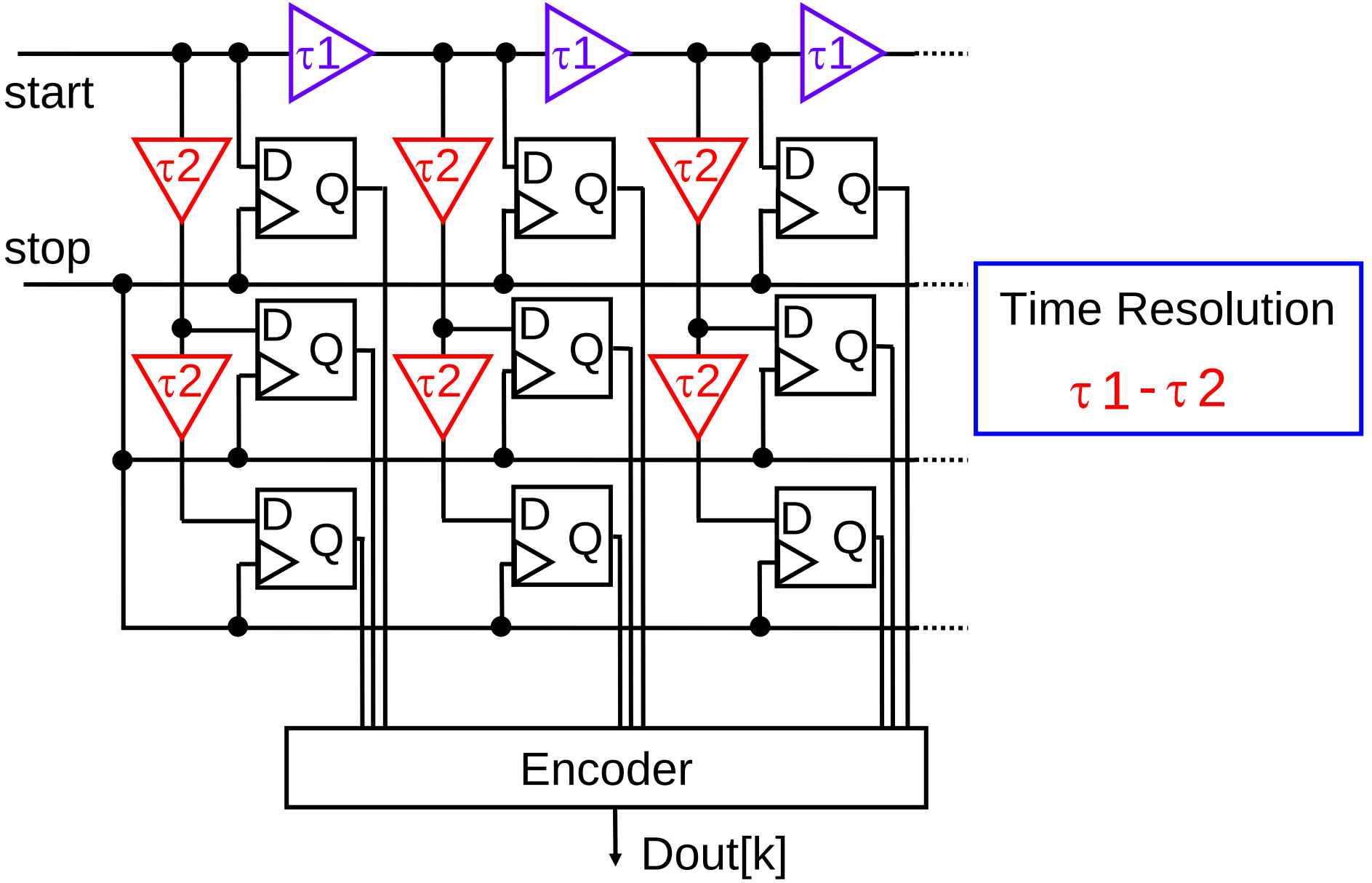


$\tau = (\tau 1 - \tau 2) \times M$

1LSB = $\tau 1 - \tau 2$ fine time resolution

→ buffer delay difference

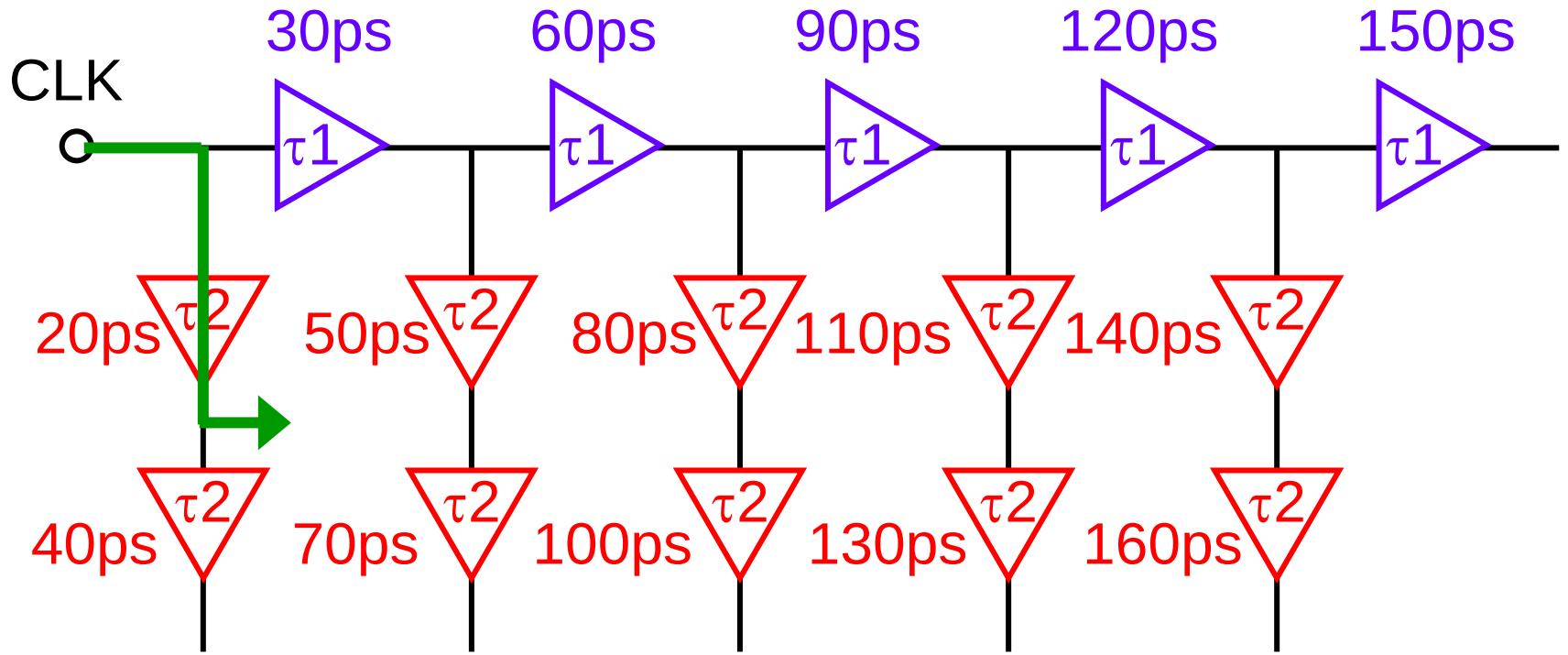
Structure of Proposed TDC



Operation of Proposed TDC

- In case of 20ps delay

Time resolution：10ps



τ1 = 30ps

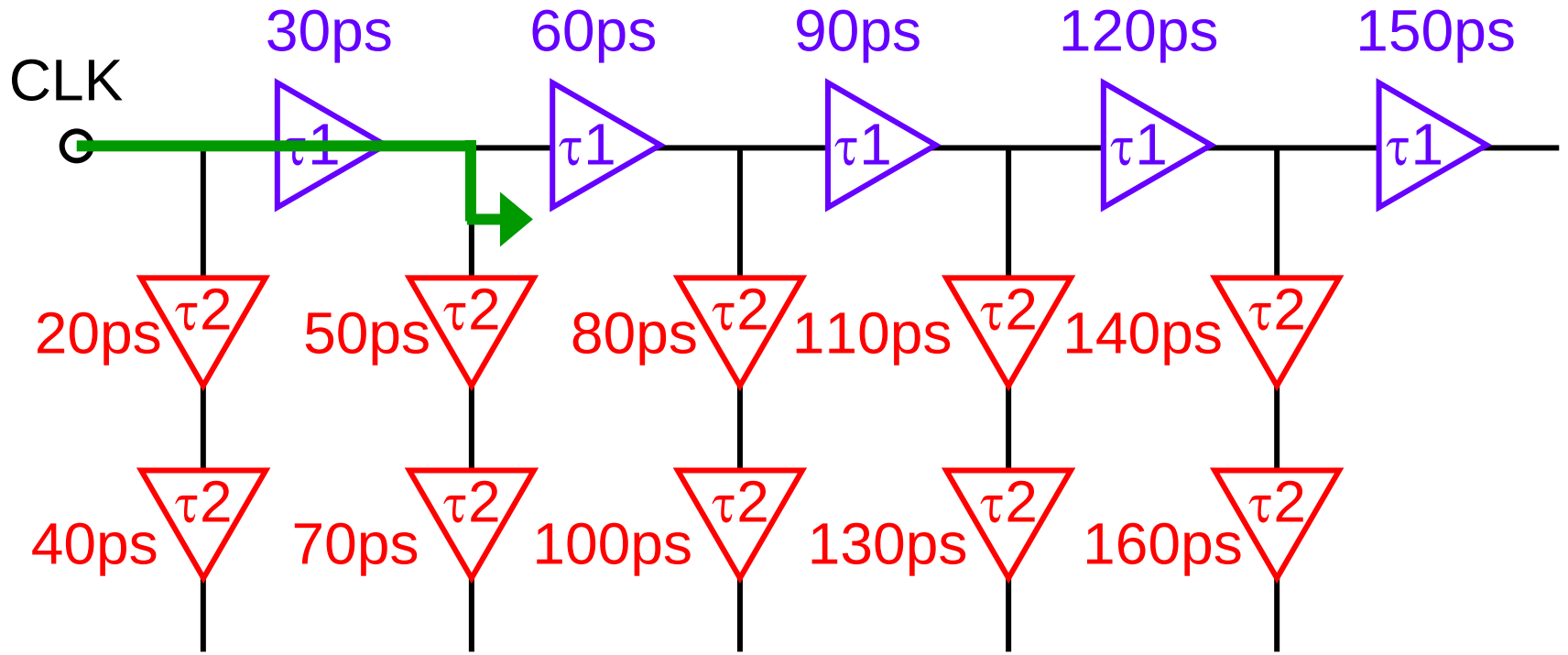
τ2 = 20ps

(90nm CMOS)

Operation of Proposed TDC

- In case of 30ps delay

Time resolution：10ps



τ1 = 30ps

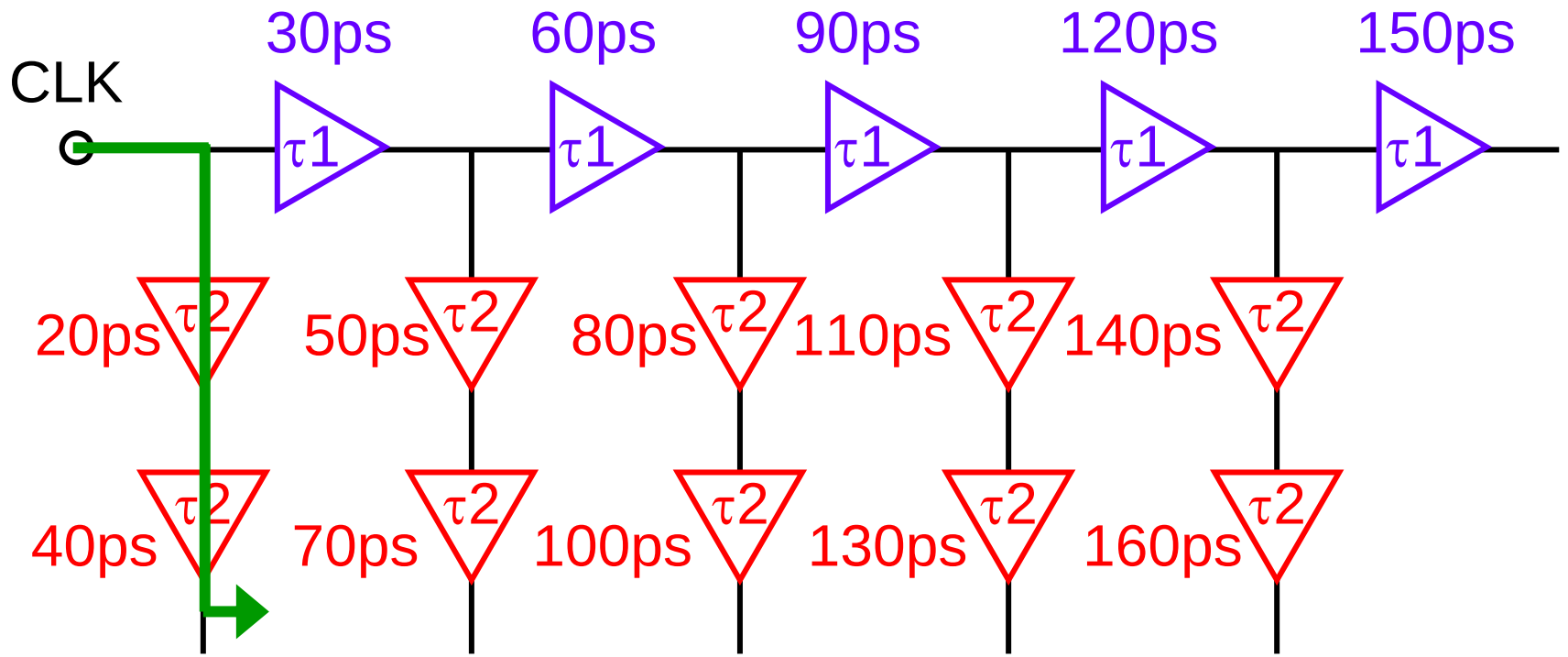
τ2 = 20ps

(90nm CMOS)

Operation of Proposed TDC

- In case of 40ps delay

Time resolution：10ps



τ1 = 30ps

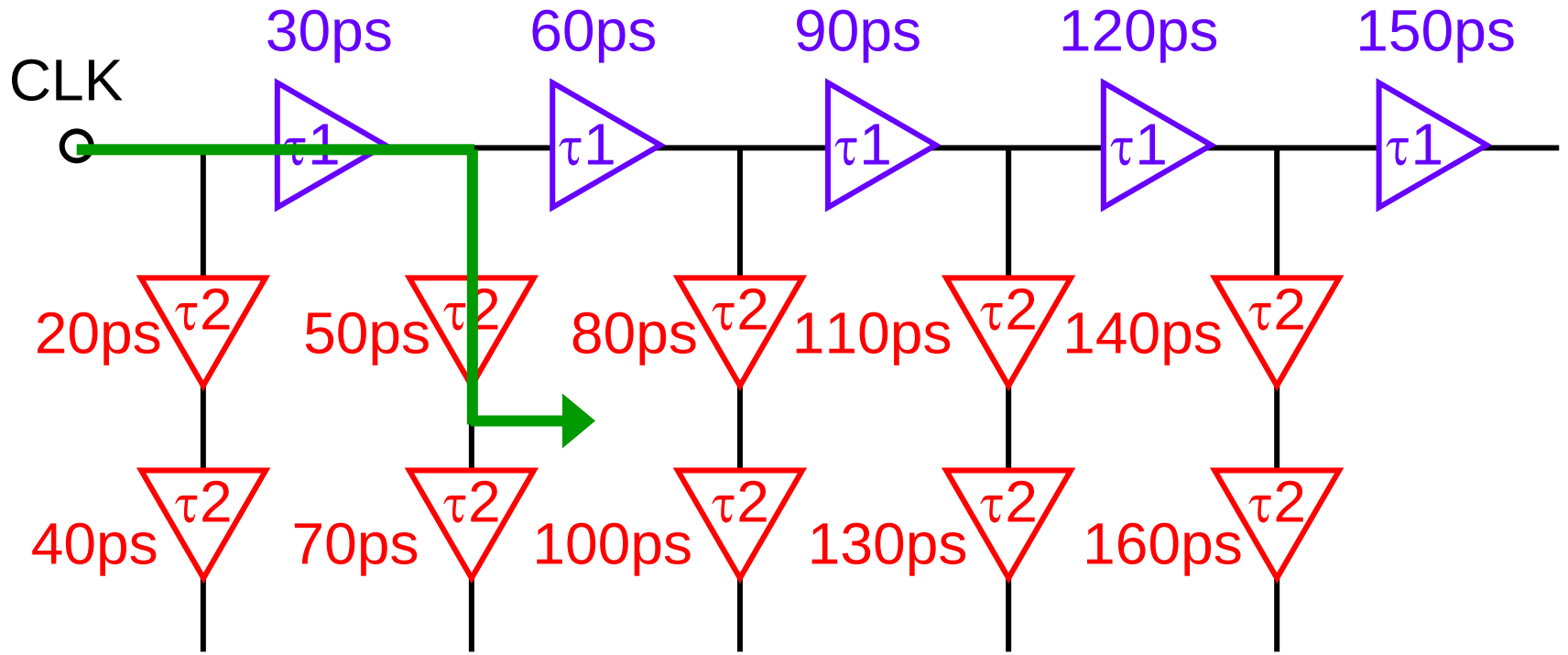
τ2 = 20ps

(90nm CMOS)

Operation of Proposed TDC

- In case of 50ps delay

Time resolution：10ps



τ1 = 30ps

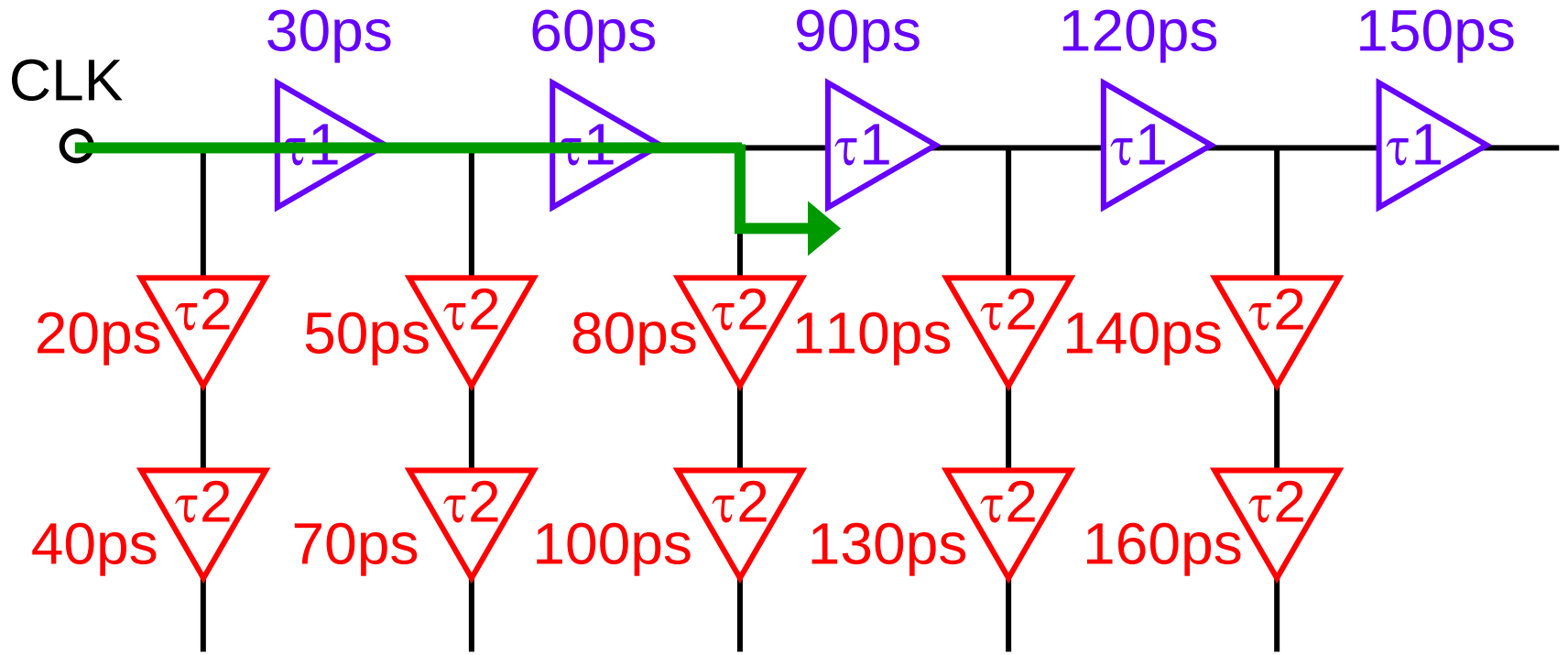
τ2 = 20ps

(90nm CMOS)

Operation of Proposed TDC

- In case of 60ps delay

Time resolution：10ps



τ1 = 30ps

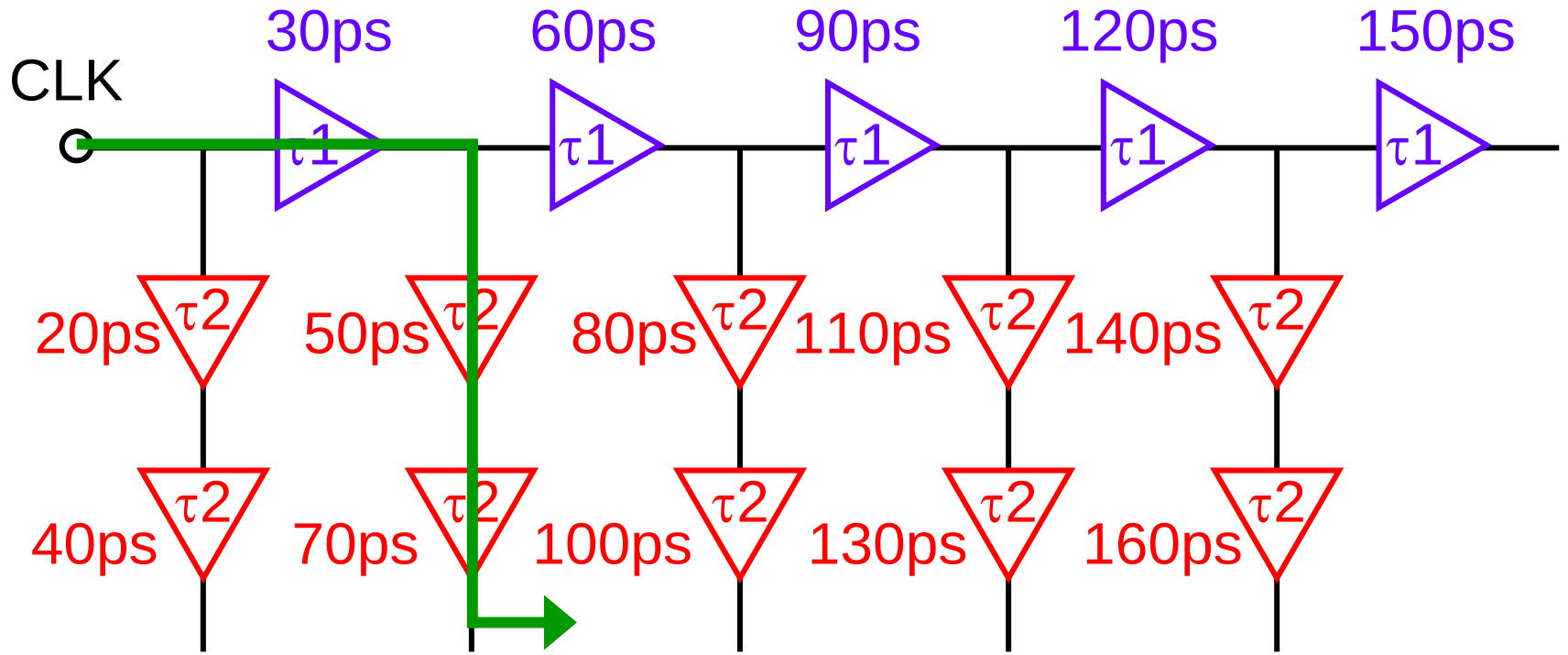
τ2 = 20ps

(90nm CMOS)

Operation of Proposed TDC

- In case of 70ps delay

Time resolution：10ps



τ1 = 30ps

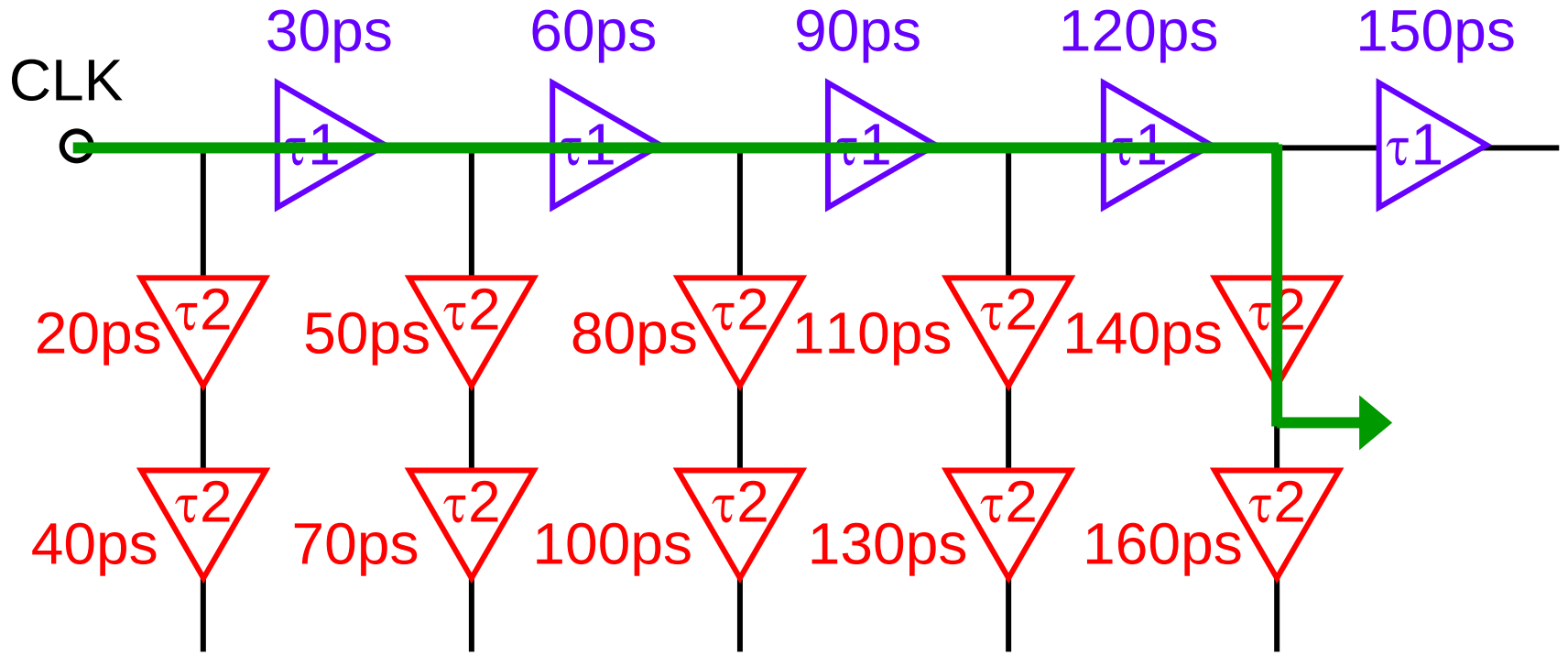
τ2 = 20ps

(90nm CMOS)

Operation of Proposed TDC

- In case of 140ps delay

Time resolution：10ps



τ1 = 30ps

τ2 = 20ps

(90nm CMOS)

Comparison among TDC Architectures

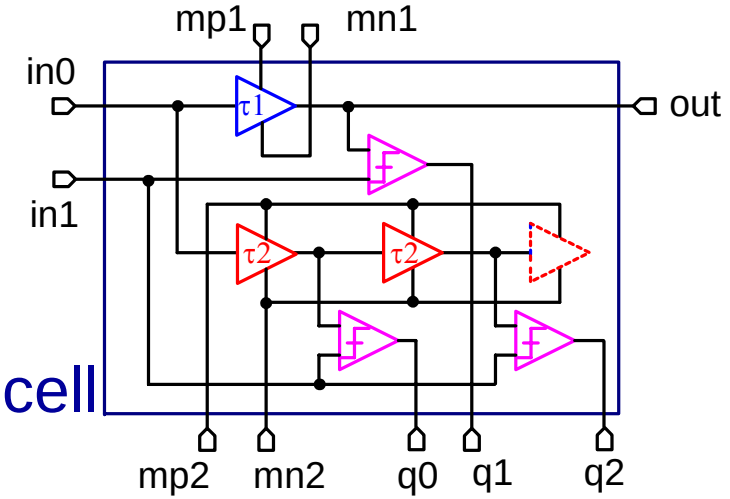
	Basic TDC	Vernier Delay Line TDC	Proposed TDC
Time resolution	$\tau 2$ 20ps	$\tau 1$-$\tau 2$ 10ps	$\tau 1$-$\tau 2$ 10ps
# of delay buffers	19	38	19

$\tau 1$: 30ps $\tau 2$: 20ps
Input range : 0 - 200ps

Proposed TDC Circuit Design

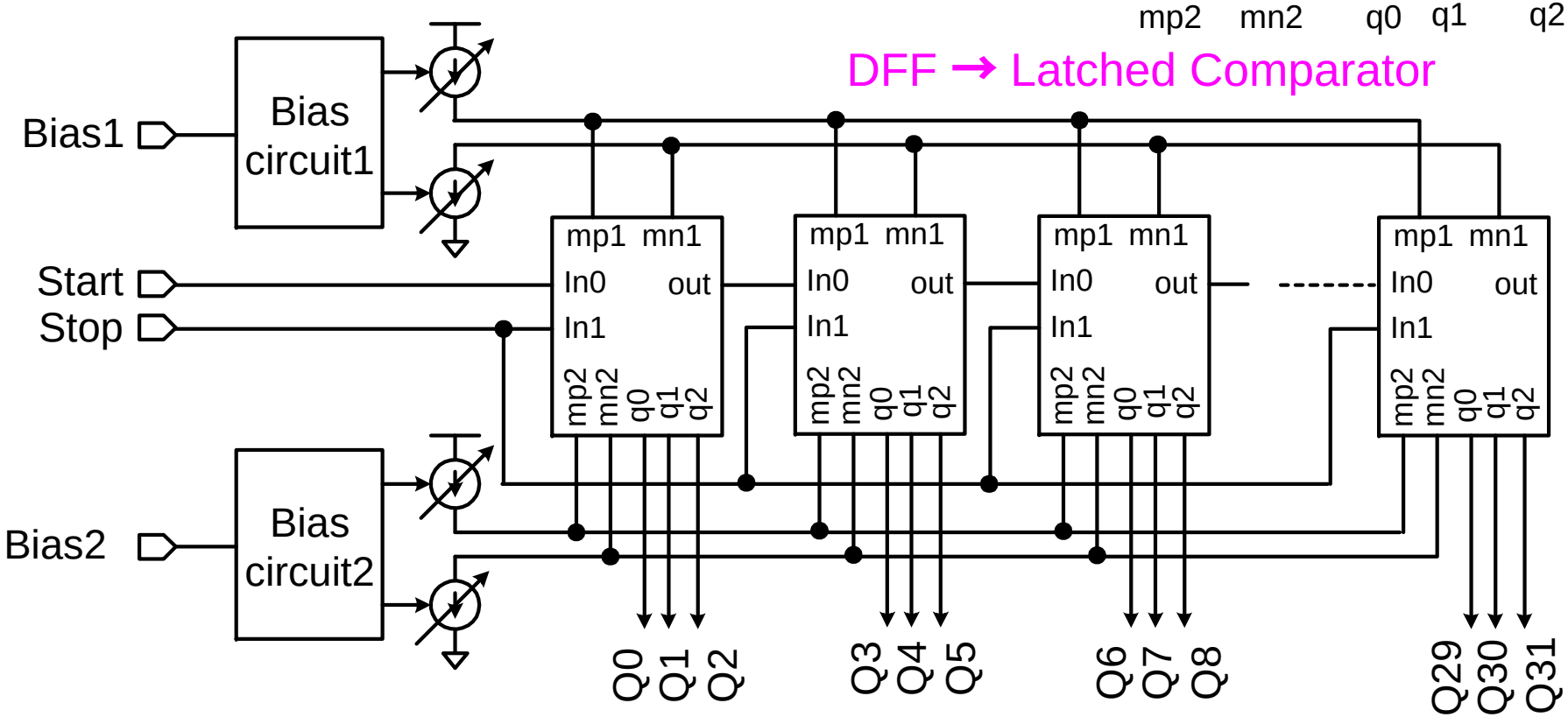
Specification

Vdd:1.8V
Time resolution:100ps
5bit output
TSMC 0.18um CMOS process

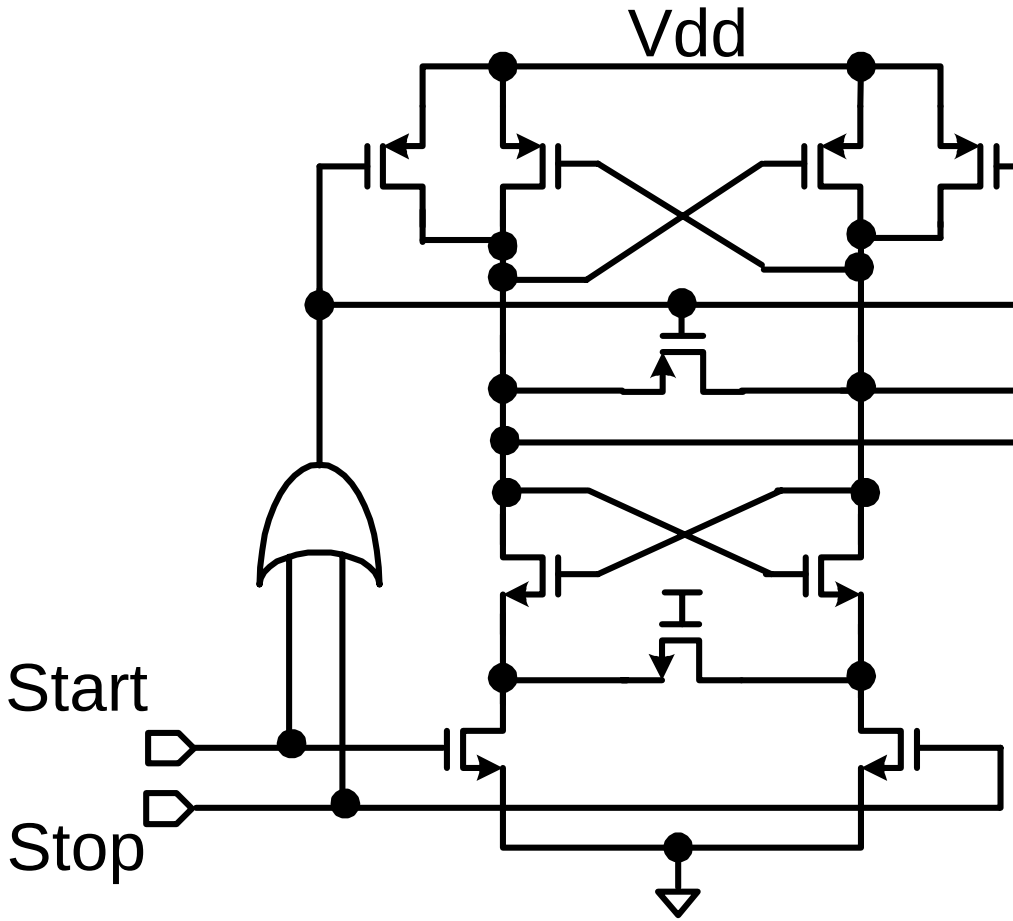


Unit cell

DFF → Latched Comparator



Latched Comparator Circuit



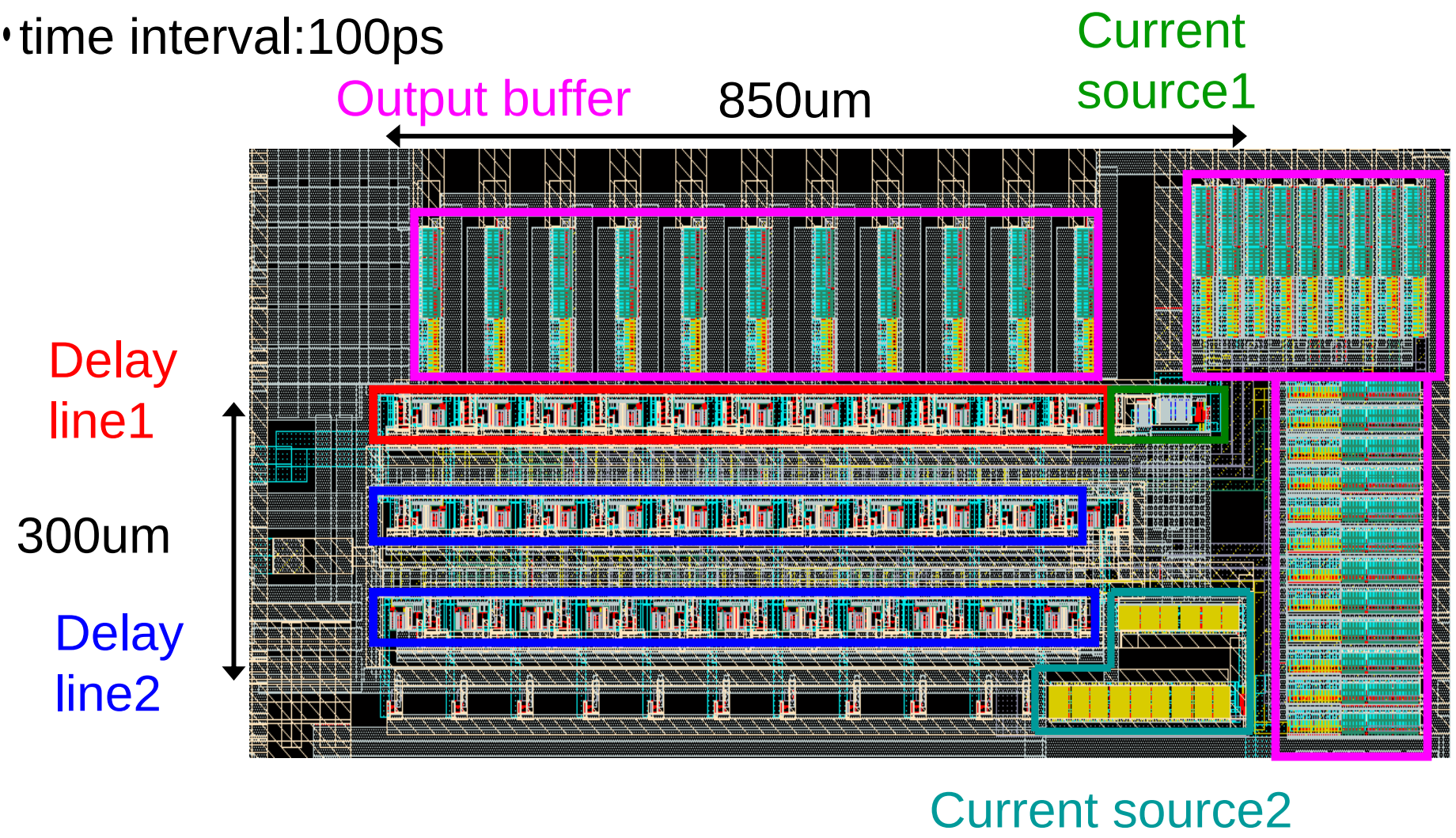
Latched Comparator
Truth Table

start	stop	out	$\overline{\text{out}}$
L	L	H	H
L	H	L	H
H	L	H	L
H	H	Hold	Hold

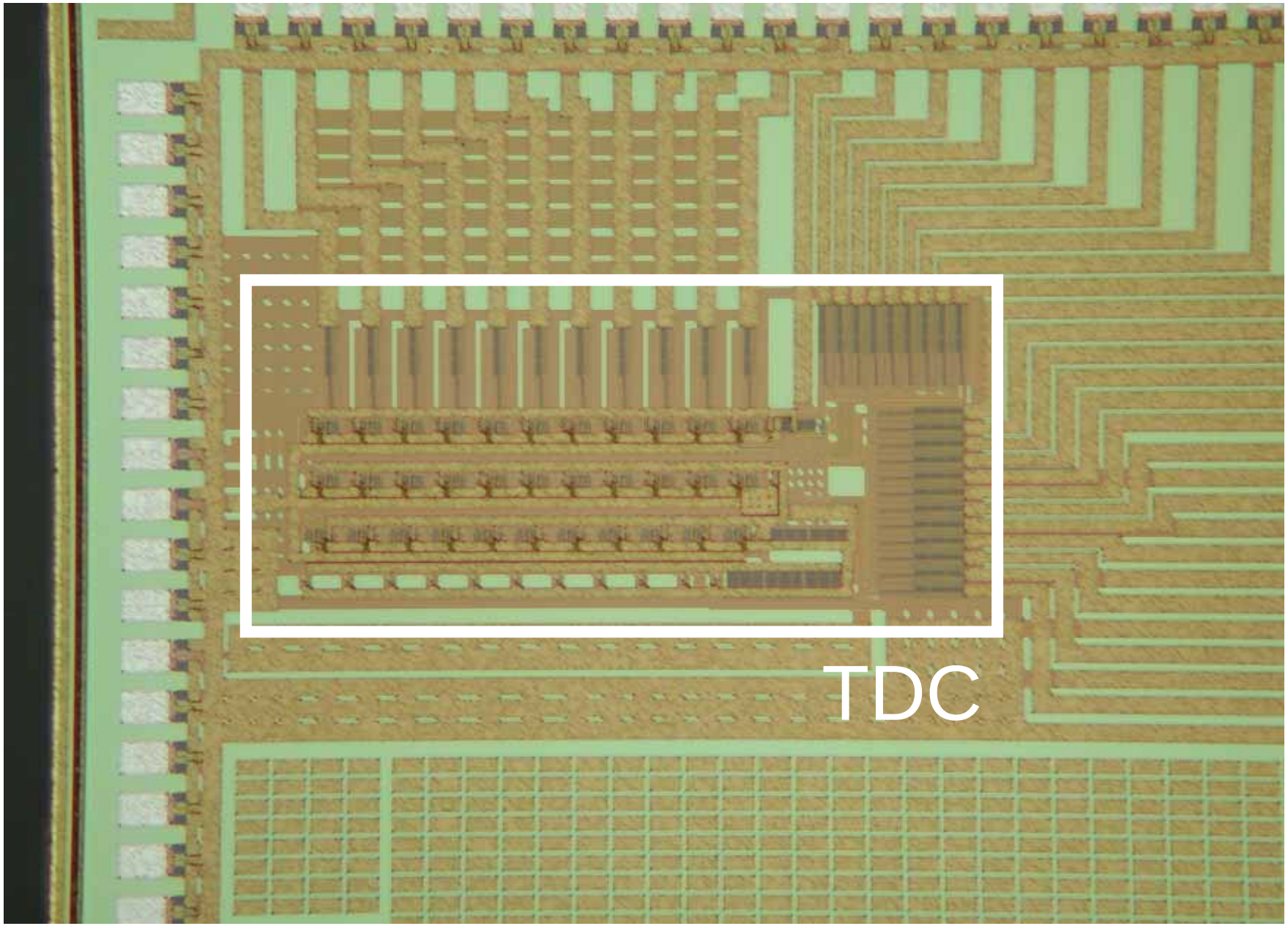
Proposed TDC Layout

Process: TSMC 0.18um CMOS (1P6M)

- Vdd:1.8[V]
- time interval:100ps
- 5bit output

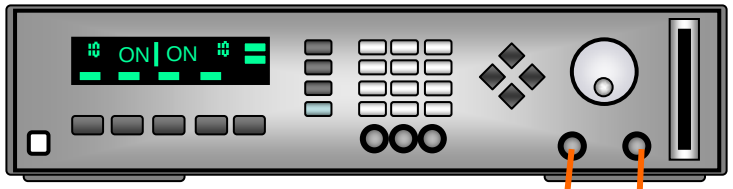


Proposed TDC Chip Photo

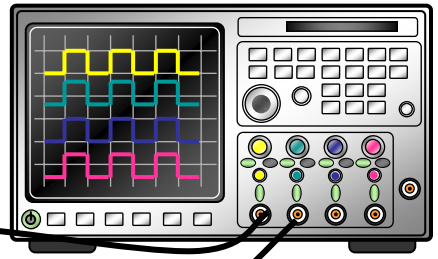


Measurement Set up

Pulse generator
Hewlett Packard 8110A



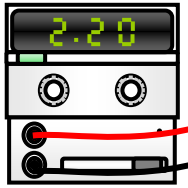
Oscilloscope
Infinium
1.5GHz 8Gsanp/s

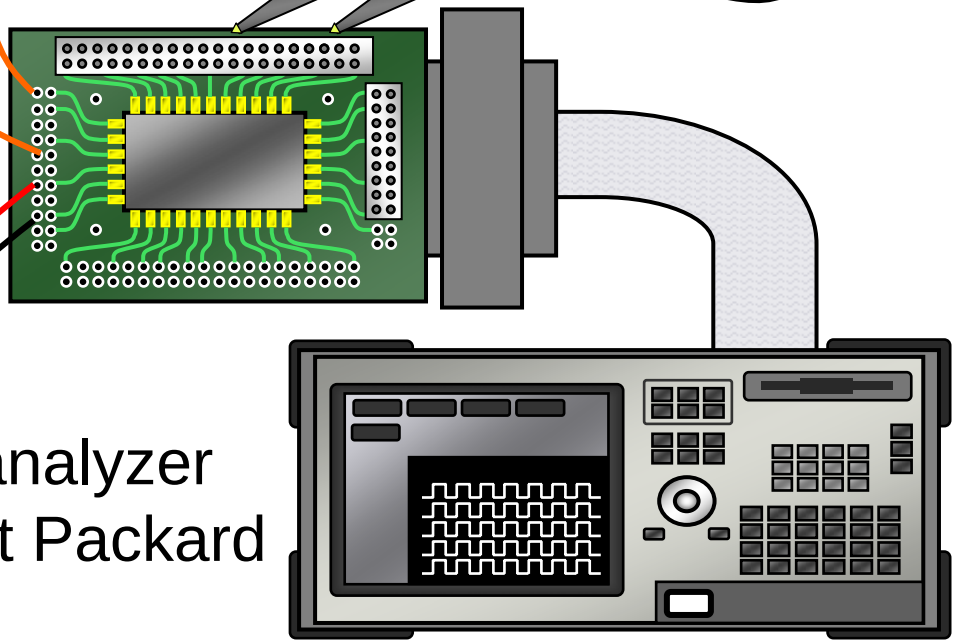


Stop
signal

Start
signal

Power supply
KIKUSUI
PMC18-5A 2.2V





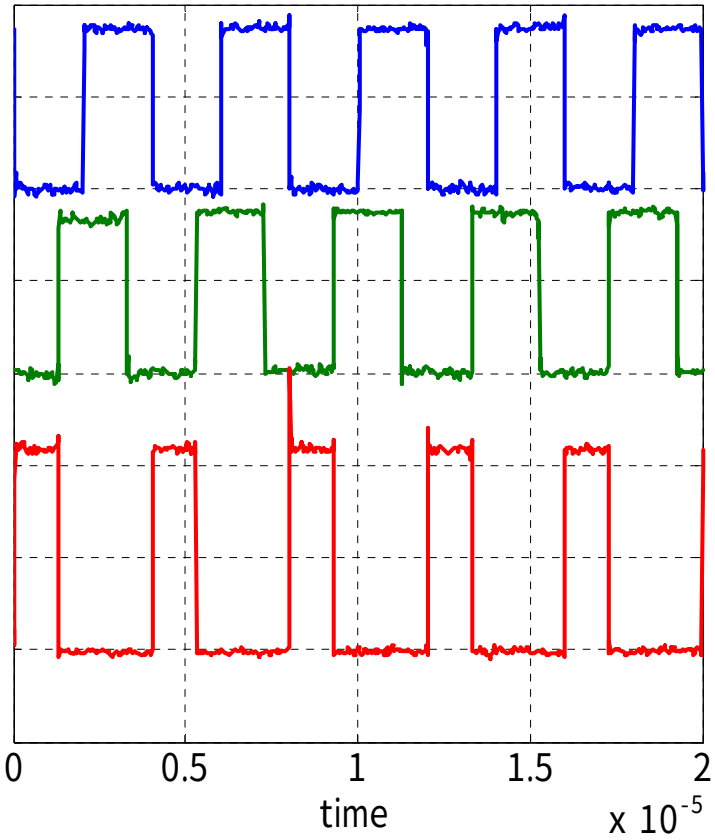
Logic analyzer
Hewlett Packard
1663C

Latched Comparator Output Waveform

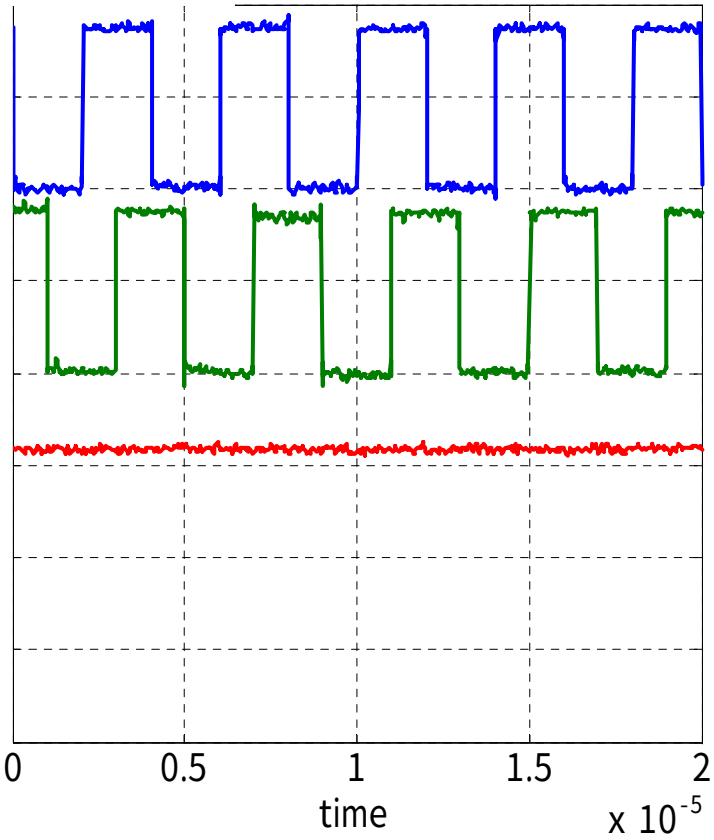
Latched Comparator
Truth Table

start	stop	out	$\overline{out}$
L	L	H	H
L	H	L	H
H	L	H	L
H	H	Hold	Hold

Faster
Stop

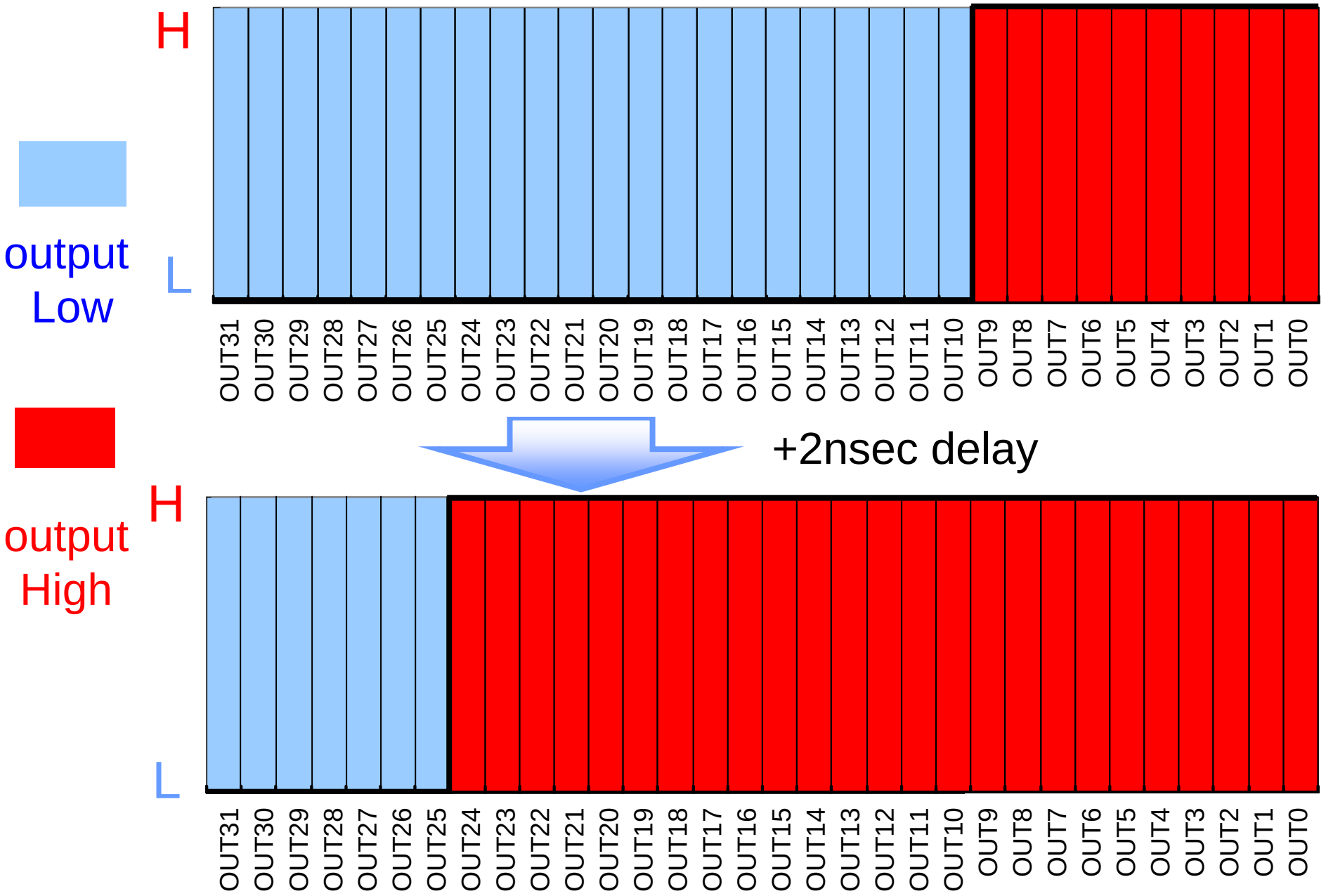


Faster
Start



Start
Stop
CMP Out

Whole TDC Measurement Results



Conclusion

- We have proposed a TDC architecture with small circuitry.
- We have designed and laid out a prototype TDC.
- We have measured the prototype TDC

⇒ Its principle is confirmed.